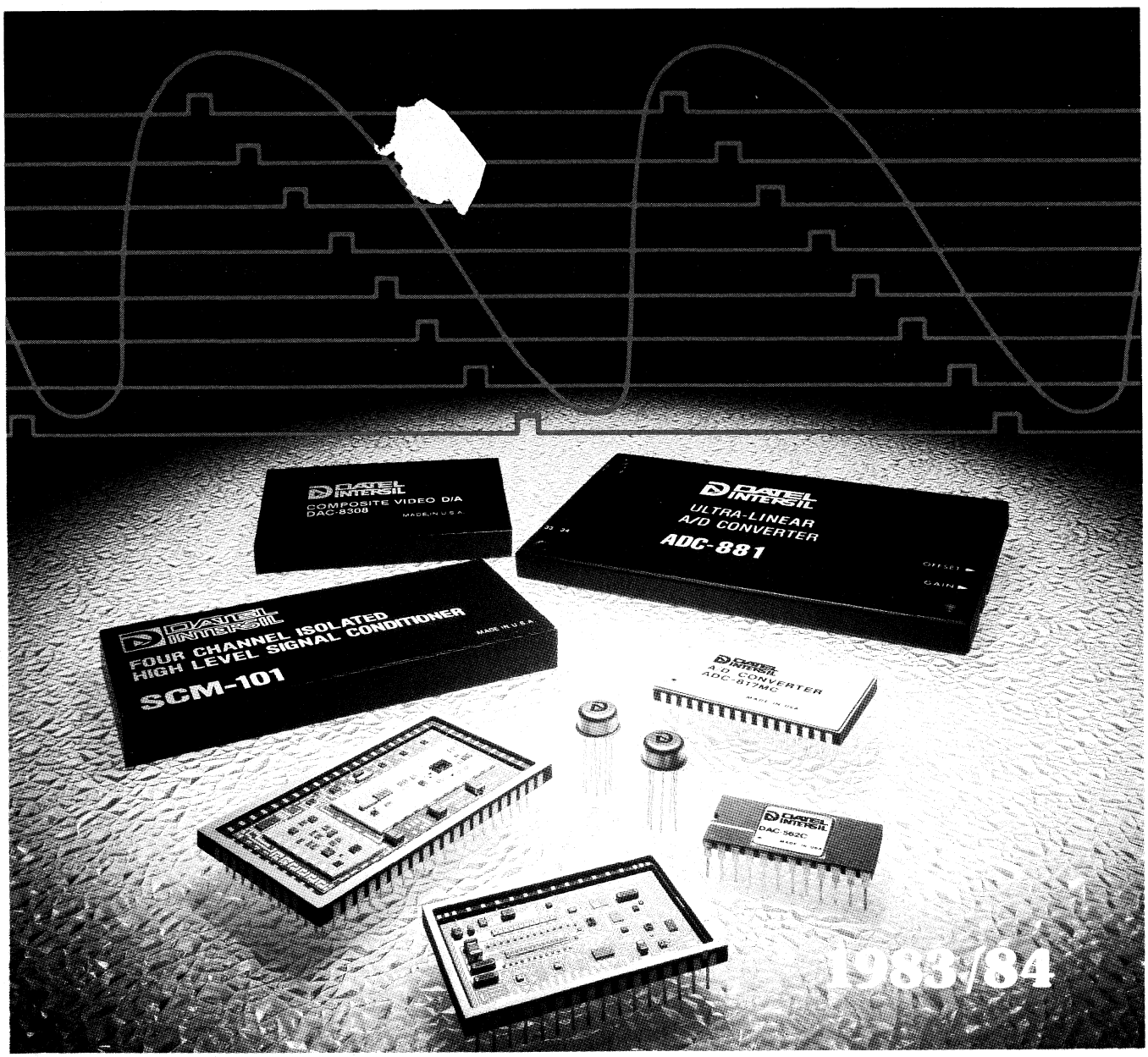
DATEL

Data Conversion Components



PRODUCT INDEX

About DATEL-INTERSIL

DATEL-INTERSIL is an established international leader in all phases of data conversion technology. To meet the rapidly growing need for data acquisition components and systems to interface with computers in industrial, commercial, scientific and military applications, DATEL-INTERSIL offers one of the broadest lines of products in the industry.

These products employ five basic technologies: monolithic CMOS, monolithic bipolar, thin-film hybrid thick-film hybrid and discrete component circuits. Many products employ a combination of these technologies to achieve higher levels of performance and complexity.

The present data acquisition product lines of DATEL-INTERSIL include: A/D and D/A converters, sample-hold amplifiers, analog multiplexers, operational and instrumentation amplifiers, V/F and F/V converters, voltage references, active filters, data loggers and readers, data acquisition subsystems, computer analog I/O boards, digital panel meters, digital panel printers, digital voltage calibrators, linear and switching power supplies and DC-DC converters.

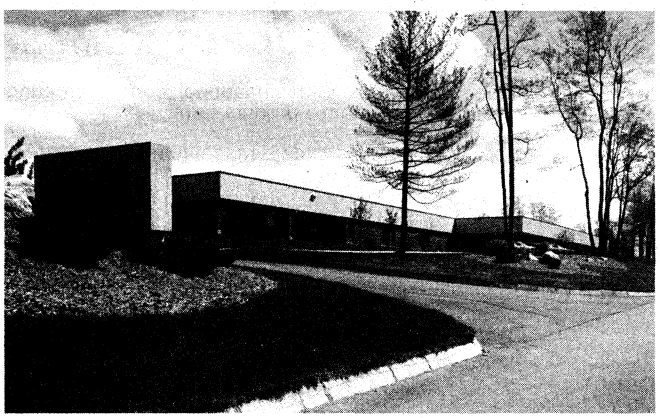
DATEL-INTERSIL's modern 120,000 square-foot manufacturing facility in Mansfield, Massachusetts, just 40 minutes from Boston's Logan Airport, houses all DATEL-INTERSIL operations. This new headquarters is dedicated to continuing our leadership position by supplying a steady stream of significant new products designed to meet the continuing demand for high performance data acquisition devices.

About This Catalog

This handbook is written for the design engineer who requires detailed technical information about products in order to select and apply a product appropriate to a particular application.

Products in this handbook are categorized by function. Each category is organized into quick selection tables followed by detailed data sheets for our most popular products. Data Sheets not included in this catalog may be obtained by contacting Datel-Intersil's nearest sales office.

DATEL-INTERSIL also maintains an experienced Application Engineering Department to answer any questions that may arise concerning the application of our products.



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DATEL INTERSIL

11 CABOT BOULEVARD
MANSFIELD, MA 02048
TEL. (617) 339-9341
TWX 710-346-9341/TLX 951340

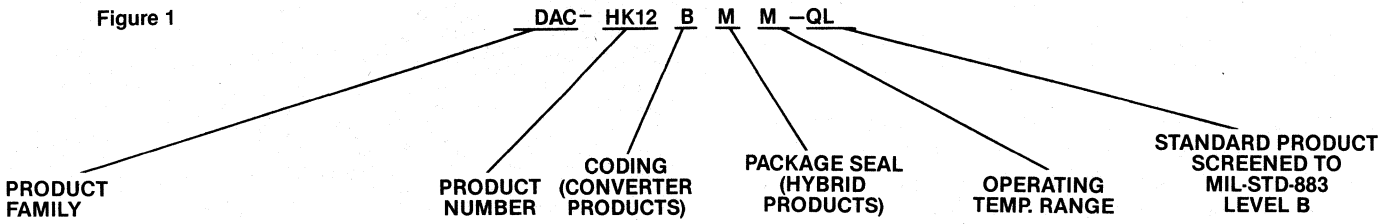
SANTA ANA, CA (714) 835-2751 • SUNNYVALE, CA (408) 733-2424 • Los Angeles, CA (213) 933-7256 OVERSEAS: INTERSIL DATEL (UK) LTD / TEL: BASINGSTOKE (0256) 57361 • INTERSIL DATEL SARL 601-57-11 • INTERSIL DATEL GmbH / (089) 77-60-95 • DATEL KK TOKYO 793-1031

PRODUCT NUMBERING INFORMATION

All data sheets contained in this handbook contain ordering guides which give the specific information needed for model differentiation within a product family.

Figure 1 below gives the standard model numbering system used by DATEL-INTERSIL for its proprietary component products.

Figure 1



ADC—Analog to Digital Converter
AM—Operational Amplifier
DAC—Digital to Analog Converter
DAS—Data Acquisition System (monolithic)
FLT—Active Filter
HDAS—Data Acquisition System (Hybrid)
MDAS—Data Acquisition System (Module)
MV/MX—Analog Multiplexer
SCM—Signal Conditioning Module
SHM—Sample-Hold Amplifier
VFQ/VFV—Voltage to Frequency Converter
VI—Voltage Inverter
VR—Voltage Reference

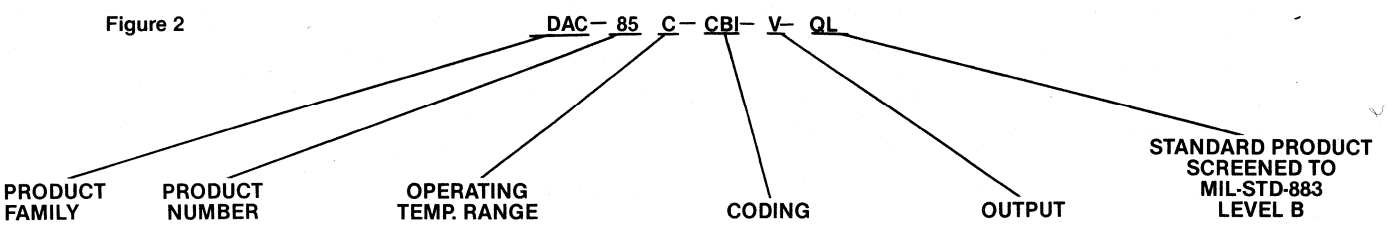
B Binary
D BCD

G Epoxy
M Hermetic

C 0°C to +70°C
R –25° to +85°C
M –55°C to +125°C

Figure 2 and figure 3 give examples of selected second source devices available from DATEL-INTERSIL where established, industry-standard product numbering has been used.

Figure 2



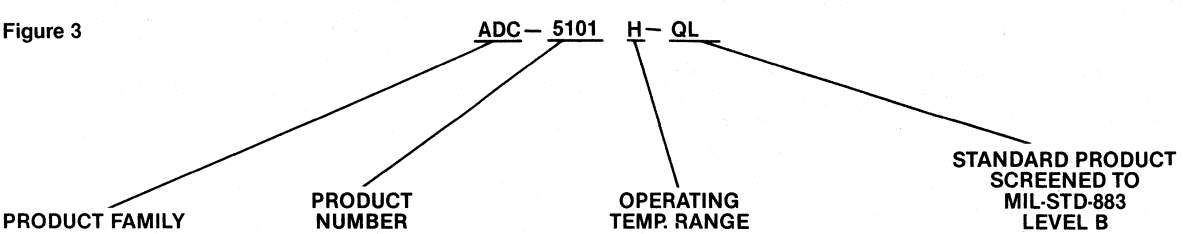
See Figure 1

C 0°C to +70°C
Blank –25°C to +85°C

CBI Straight Binary
COB Offset Binary
CCD BCD

V Voltage
I Current

Figure 3



See Figure 1

Blank 0°C to +70°C
E –25° to +85°C
H –55°C to +125°C

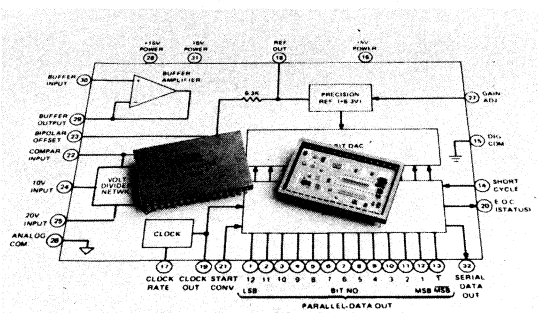
PRODUCT AVAILABILITY

The following table lists DATEL-INTERSIL products which are not recommended as being economical for "design-in" situations.

Since these products are "designed into" a great number of existing applications, DATEL-INTERSIL will continue to make them available. However, special ordering conditions may be required, so please contact your nearest DATEL-INTERSIL sales office before ordering.

MODEL Number/Series	NEAREST EQUIVALENT
ADC- ECONOVERTER	ADC-856
ADC-E Series	ADC-ET Series
ADC-G8B	ADC-815
ADC-G10B	ADC-816
ADC-HU	ADC-833
ADC-L Series	ADC-HX12B
ADC-M Series	ADC-HZ12B
ADC-MA10	ADC-HX12B
ADC-SH4B	ADC-HS12B
ADC-UH Series	ADC-833
ADC-89 Series	ADC-856
DAC-HI Series	DAC-HF Series
DAC-I Series	DAC-HF Series
DAC-V Series	DAC-HZ12/DAC-85C
DAC-VR Series	DAC-HK12
DAC-98 Series	DAC-IC8B
DAC-198 Series	DAC-HZ12/DAC-85C
DAC-298 Series	DAC-HZ12/DAC-85C
DAC-4910/12 Series	DAC-HZ12/DAC-85C
DAC-6912 Series	DAC-HZ12/DAC-85C
SHM-1	SHM-IC-1
SHM-2	SHM-7
SHM-UH	SHM-7
AM-100 Series	AM-411
AM-201 Series	AM-542

New Products from Datel Intersil



ADC-810, ADC-811
Ultra-fast, 12-bit Hybrid Analog to Digital Converters

The ADC-810 and ADC-811 are ultra-fast, hybrid, successive approximation, 12-bit analog to digital converters. The ADC-810 achieves a maximum conversion time of 2 μsec. Conversion time for the ADC-811 is 4 μsec maximum, which is the only difference between the two. Both models are pin-compatible with industry-standard ADC-85/87 converters, offering increased speed, high accuracy and reliability. Models are available subjected to 100% screening to MIL-STD-883B.

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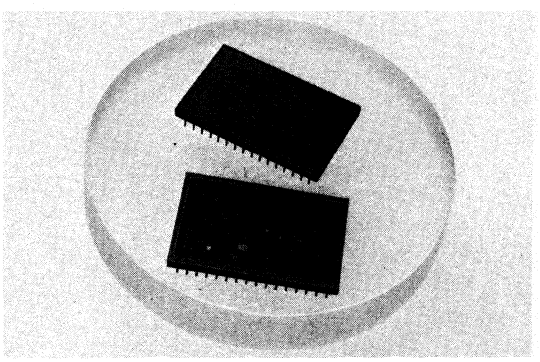

ADC-84, 85, 87 new, industry standard military and industrial 12-bit A/D converters

DATEL-INTERSIL's ADC-84, ADC-85, and ADC-87 series devices are high-performance, low-cost 10 and 12-bit successive approximation analog to digital converters. Direct replacements for industry standard ADC-84/85/87 converters, these devices offer improved performance and reliability. Each converter is available in two performance grades; 12 bits of resolution at a maximum conversion speed of 10 μs, or 10 bits of resolution at a conversion speed of 6 μs maximum. The ADC-87 is specified for operation over the full military operating temperature range of $-55°C$ to $+125°C$. Versions of this model are availabel screened to MIL-STD-883B.

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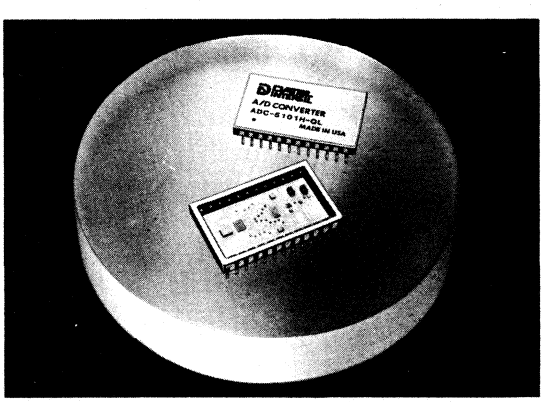

ADC-5101 high speed, 8-bit A/D offers high temperature operation at low cost

The ADC-5101 is a high speed, adjustment-free, 8-bit A/D converter. Pin compatible with standard ADC-5101 converters, these devices offer high accuracy and high speed over the full military operating temperature range of $-55°C$ to $+125°C$. Designed for operation without external adjustment circuits, the ADC-5101 accomplishes an 8-bit conversion in only 900 ns maximum. Models are available subjected to 100% screening to MIL-STD-883 Class B.

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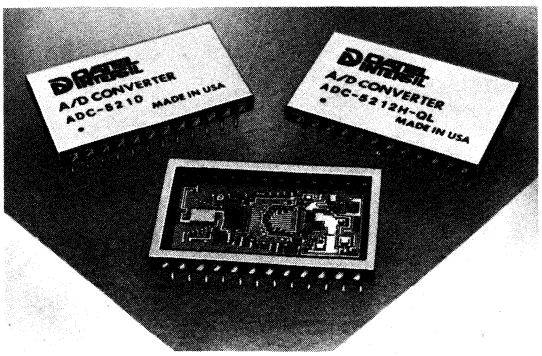

ADC-5210 series adjustment-free 12-bit A/D features high accuracy over military temperature range

The ADC-5210 series are high performance, 12-bit successive approximation A/D converters. Completely pin and function compatible with standard ADC-5210 devices, these models offer significantly improved high-temperature operation at lower cost. Full scale absolute accuracy error is a maximum of ±0.05% FSR at +25°C and only ±0.2% FSR over the full military operating temperature range of −55°C to +125°C; an improvement of 10 LSBs over the error specified on competing devices. MIL-STD-883 screening is available.

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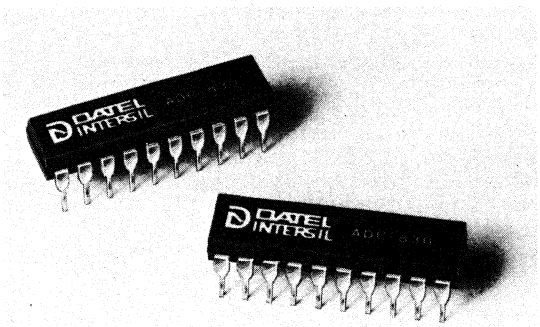

ADC-830 microprocessor compatible 8-bit A/D converter

DATEL-INTERSIL's ADC-830 is a low-cost, monolithic 8-bit A/D converter designed to operate directly with the 8080A control bus via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic. Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8-bit conversion in 100 μs with a maximum total adjusted error of only ± ½ LSB. Its combination of low cost, small size, and interface versatility make the ADC-830 an ideal choice for many process control and instrumentation applications.

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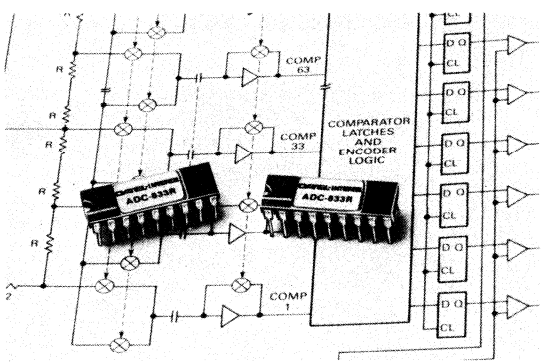

ADC-833 6-bit A/D features video speed at low power

The ADC-833 is a low-power, video-speed, 6-bit flash A/D manufactured with CMOS/SOS technology. The device is capable of digitizing an analog input signal at conversion rates up to 15MHz while its power consumption is only 200mW. The analog input voltage range is +2.5V to +10V, and typical differential linearity error is only ± ½ LSB. Outputs are buffered three-state and include an overflow output which allows the user to cascade two units to achieve 7-bit resolution.

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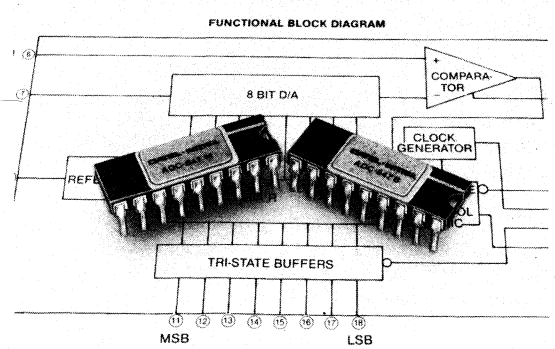

ADC-847 Microprocessor Compatible, 8-Bit A/D Converter

The ADC-847 is a low cost, monolithic, 8-bit A/D converter designed to interface directly to a microprocessor via three-state outputs. Utilizing the successive approximation technique, the ADC-847 completes an 8-bit conversion in 9 μS with a maximum linearity error as low as ± ¼ LSB. The ADC-847 includes, an internal clock generator, reference circuit, successive approximation register, comparator, three-state buffers, 8 bit D/A converter and interface and control logic, making it an ideal choice for many process control and instrumentation applications. The ADC-847 is available for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges and is packaged in either an 18 pin plastic or ceramic DIP.

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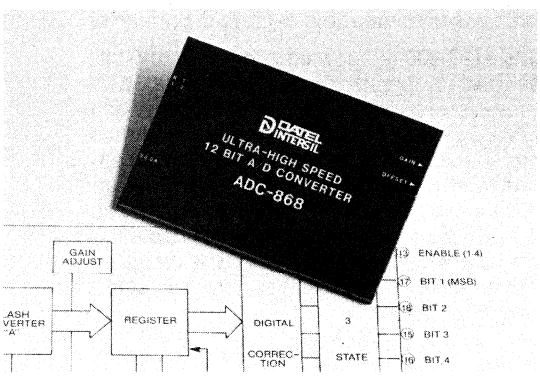
New Products from Datel Intersil



ADC-868, DATEL-INTERSIL's new Ultra High Speed, 12 Bit Modular A/D Converter Features 500 nsec Conversion Time

The ADC-868 is an ultra-high speed, 12 bit, modular A/D converter. A conversion time of 500 nsec (max) with no missing codes is guaranteed over the 0°C to +70°C temperature range. Standard input ranges are 0V to 5V for unipolar operation and ±2.5V for bipolar operation using straight binary and offset binary coding respectively. Extended input ranges of 0V to 10V (unipolar) and ±5V (bipolar) can be implemented by the addition of 2 external resistors. Zero (offset) and gain are adjustable with two on board potentiometers, no external components are required. The packaging is a 4″ × 6″ × 0.375″ CR steel casing with a 34 pin male connector at one end.

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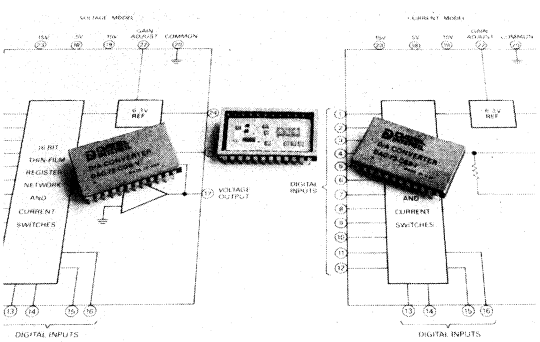

DAC-72 industry standard, high resolution microelectronic D/A converter

The DAC-71/72 series is a comprehensive family of high performance 16-bit D/A converters offering voltage or current outputs with either complementary binary or 4-digit BCD, TTL compatible, input coding. Linearity error is ±0.003% FSR maximum and settling time for an output voltage step of 20V to ±0.003%, is only 10 μs. Current output settling time, 2 mA to ±0.003%, is only 1 μs. All models are cased in miniature, 24-pin packages and are completely pin and function compatible with industry-standard DAC-71/72 converters.

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DAC-85, DAC-87 new, industry standard military and industrial 12-bit D/A converter

The DAC-85 and DAC-87 are industry standard high-performance, 12-bit D/A converters. This comprehensive line of D/As allows a choice of voltage or current output models with either 12-bit binary or 3-digit BCD coding. The DAC-87 is specified for operation over the −55°C to +125°C military temperature range, and is available with 100% screening in accordance with MIL-STD-883B. This family of units has been specifically designed to be pin and function compatible with industry standard DAC-85/87 converters while offering substantially improved performance.

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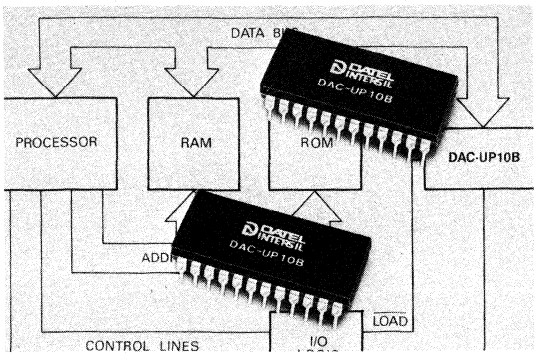

DAC-UP10B new 10-bit D/A with input registers

The DAC-UP10B is a low cost, monolithic, 10-bit D/A converter with internal registers. The device also includes a high-speed output amplifier, stable internal reference, and an input buffer amplifier. Low loading latches, adjustable logic thresholds and addressing capability allow the DAC-UP10B to directly interface with many microprocessor and logic controlled systems. The output voltage range is 0 to + 10V for unipolar mode, ± 5V for bipolar. A full scale output change settles to within 0.05% FSR in 5 μs.

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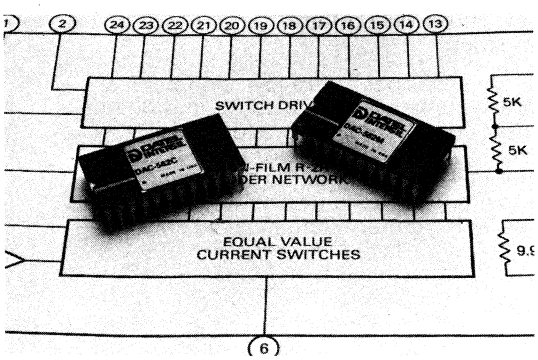

DAC-562 High Performance 12 Bit D/A Converter

The DAC-562 is a high performance monolithic 12 bit D/A converter fabricated with advanced bipolar technology. It consists of a control amplifier, 12 switched current sources, an R-2R resistor ladder network, and 12 level shifters and switch drivers. The DAC-562 features an output current of 2 mA which can also be connected to give a ± 1 mA output. Linearity for the DAC-562C and DAC-562M is ± ½ and ± ¼ respectively, with monotonicity guaranteed over the operating temperature range. Both models are packaged in a 24 pin hermetically sealed ceramic DIP.

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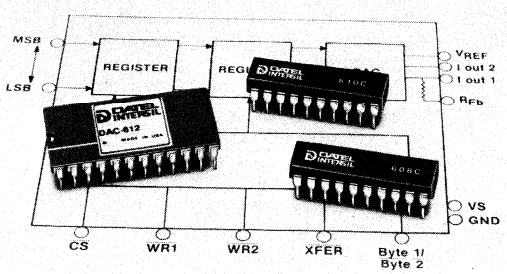

DAC-608/610/612 Low Cost, Double-Buffered Microprocessor Compatible D/A Converters

The DAC-608, DAC-610 and DAC-612 are low cost monolithic 8, 10 and 12 bit multiplying D/A converters, designed to interface directly with most popular microprocessors. Double-Buffered inputs allow the converters to output an analog voltage corresponding to one digital word while holding the next. The converters consist of an input register, a D/A register, control logic and D/A converter. Settling time is 1 μS for the DAC-608 and DAC-612 and 500 nS for the DAC-610. The reference input of these converters is selectable over a range of ±10V and may also be used as the analog input for four quadrant multiplication applications.

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DAC-8308, DAC-8318
Ultra-fast, 8-bit Digital to Analog Converter Modules

DATEL-INTERSIL's DAC-8308 and DAC-8318 are high performance, ultra-fast 8-bit digital to analog converters. The DAC-8308 accepts 8-bits at throughput rates up to 40 MHz and produces a composite video output signal with 256 gray scale levels including setup, blanking and sync., all derived from separate digital inputs. The output will directly drive a terminated 75Ω coaxial cable giving a 0 to − 1.054V output that is in general conformance with EIA standards RS170 and RS343A. The DAC-8318 is the same converter without the composite video inputs.

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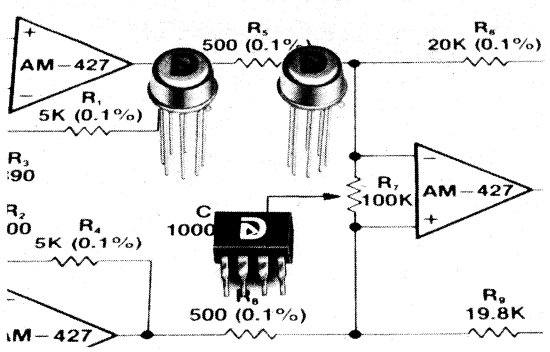
New Products from Datel Intersil



AM-427 Ultra-Low Noise Monolithic Operational Amplifier

The AM-427 is a low cost, ultra-low noise operational amplifier which is designed for instrumentation grade signal conditioning where low noise, low offset voltage and low offset voltage drift are required. The AM-427 combines exceptional DC performance with ultra-low noise operation. Maximum input noise voltage density and input noise current density at 10 Hz are 5.5 nV/$\sqrt{\text{Hz}}$ and 0.4 pA/$\sqrt{\text{Hz}}$ respectively. The AM-427 is available for operation over the industrial, −25°C to +85°C and military, −55°C to +125°C temperature ranges and is packaged in either an 8 pin TO-99 or an 8 pin ceramic DIP.

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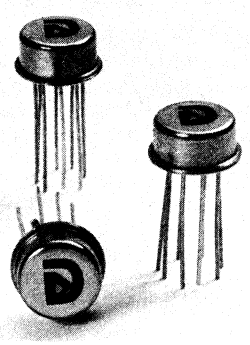

AM-430 Ultra-Low Drift, Monolithic Operational Amplifier

The AM-430 is a chopperless ultra-low drift monolithic operational amplifier. Featuring a 25 μV maximum input offset voltage, the AM-430 requires no external zeroing in most applications. Maximum input offset voltage drift is only 0.6 μV/°C. The amplifier has low input noise characteristics of 9 nV/$\sqrt{\text{Hz}}$ voltage noise density and 0.2 pA/$\sqrt{\text{Hz}}$ current noise density. Output voltage range is ±10V minimum at ±25 mA load current with a short circuit protected output. Its unique combination of specifications make the AM-430 ideal for accurate low level signal amplification, and biomedical, or precision integrator applications where low drift, low noise, and precise closed loop gain are required.

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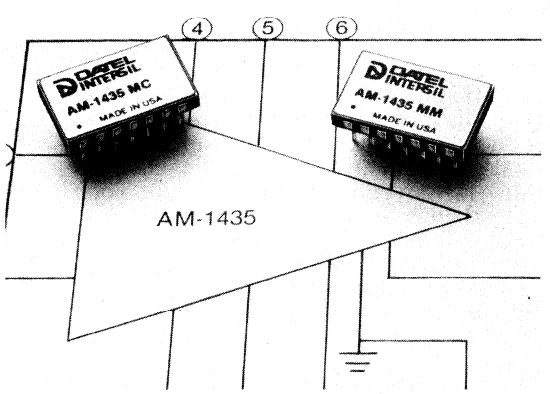

AM-1435
Ultra High Speed, Wideband, Hybrid Operational Amplifier

DATEL-INTERSIL's AM-1435 is an ultra-fast settling, wide-band operational amplifier. The AM-1435 achieves a settling time of only 70 nsec for a 10V step to 0.01% accuracy. High speed performance is optimized with high open loop gain, flat frequency response beyond 10 kHz and a roll-off of 6 dB/octave to beyond 100 MHz. Gain bandwidth product is typically 1GHz and slew rate is 300V/μsec. All models are packaged in hermetically sealed ceramic cases, with full screening to MIL-STD-883 level B available.

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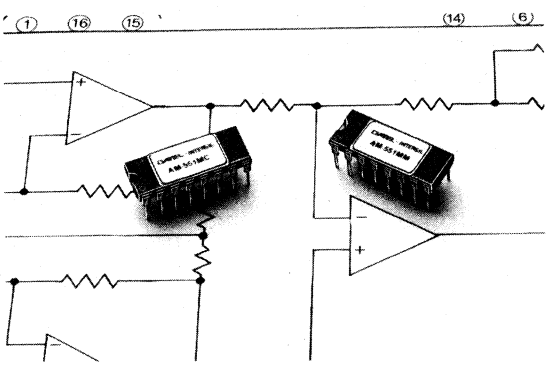

AM-551 Low Cost, Hybrid Programmable Instrumentation Amplifier

DATEL-INTERSIL's AM-551 is a low cost, high performance, programmable gain instrumentation amplifier manufactured with hybrid thin-film technology. Gain range is 1 to 1000 and is set externally by a single resistor and simple pin-strapping. Settling time is 2 μsec for a 20V output step to 0.01% accuracy, with a slew rate of 23V/μsec and a small signal bandwidth of 400 kHz. Applications include remote amplification of low-level signals produced by thermocouples, strain gages and RTD's, high performance data acquisition systems and remote instrumentation systems.

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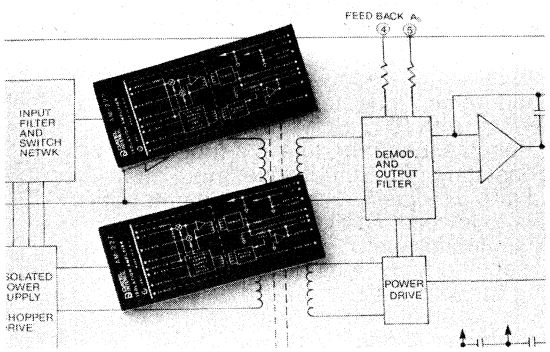

AM-227
New, Low Cost, Ultra-Stable, Modular Isolation Amplifier

The AM-227 is a precision, low-cost, modular isolation amplifier designed specifically for applications involving the amplification of low-level, low frequency signals in the presence of high common mode interference. The ultra-low drift, high accuracy and high CMRR make it possible to accurately amplify microvolt level signals with a user selectable gain range of 10 to 1000. Common mode rejection is 166 dB minimum and common mode isolation voltage is 1000 VDC. The AM-227 is packaged in a compact 2.8 × 1.2 × 0.45 inch, fully encapsulated module.

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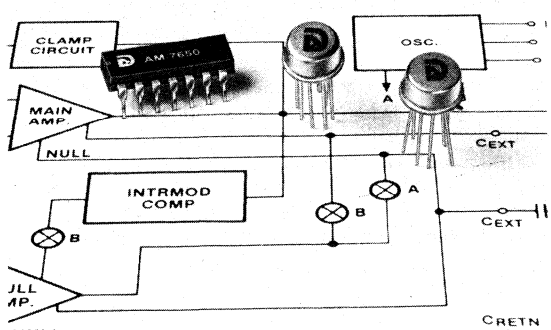

AM-7650 new, low cost chopper stabilized operational amplifier features ultra-low offset voltage and drift

DATEL-INTERSIL's AM-7650 is a low cost, high performance chopper stabilized amplifier featuring exceptionally low offset voltage and input bias specifications combined with excellent bandwidth and speed characteristics. Input offset voltage is typically ±0.7 μV with an input offset voltage drift as low as 0.01 μV/°C. The AM-7650 achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, which is nulled by alternate clock phases from the internal clock oscillator. The 14 pin DIP version also includes a provision for the use of an external clock if an application requires. These devices are internally compensated for unity-gain operation.

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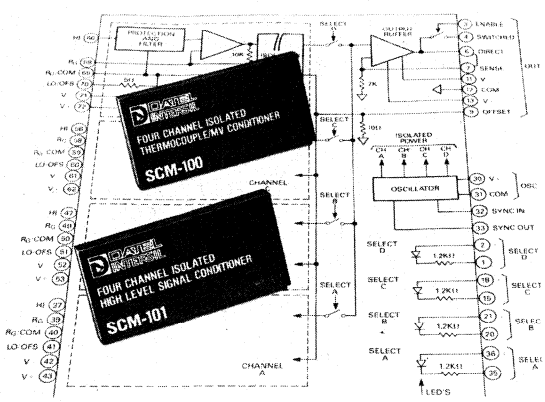

SCM-100, SCM-101
New Four-Channel, Isolated Signal Conditioning Modules

DATEL-INTERSIL's SCM-100 and SCM-101 are low cost, high performance signal conditioning modules designed to interface with low-level thermocouple and high level analog inputs, respectively. Each module is a functionally complete unit, consisting of four individually isolated input channels that are multiplexed into a single output buffer. The SCM-100 features an input span range of ±5 mV to ±100 mV while the SCM-101 is optimized for ±50 mV to ±5V or 4 to 20 mA input signals. Each device is packaged in a compact 2 × 4 × 0.4 inch encapsulated module.

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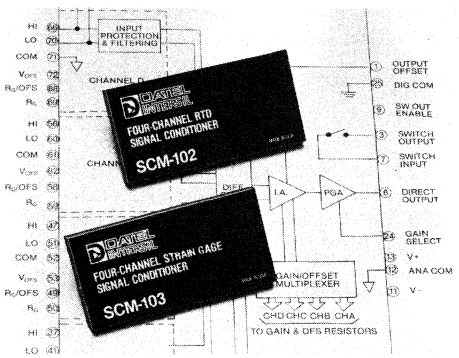
New Products from Datel Intersil



R.T.D., Strain Gage Signal Conditioners Feature Low Cost, Four Channel Operation SCM-102, SCM-103

The SCM-102 and SCM-103 are low-cost, high performance signal conditioning modules specifically designed to interface with RTD (SCM-102) and strain gage (SCM-103) sensors. Each module is a functionally complete unit consisting of four individual input channels multiplexed into a single low-drift instrumentation amplifier which is followed by a digitally controlled programmable gain instrumentation amplifier output stage. Featured specifications include a minimum channel scanning speed of 3000 chan/sec, ±1 μV/°C total offset drift, ±0.01% maximum nonlinearity and user selectable switched or direct outputs.

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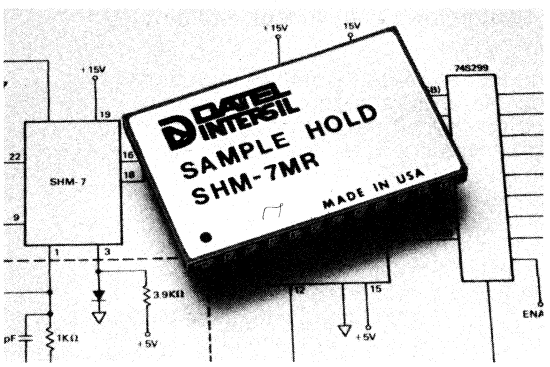

SHM-7 new video speed sample-hold features ultra-high speed and dual outputs

DATEL-INTERSIL's SHM-7 is an ultra-fast sample-hold amplifier designed for high-speed signal processing applications. The SHM-7 acquires a 2V input change to 0.1% in only 40 ns and the hold mode settling time is only 20 ns; making possible sampling rates of up to 17MHz. A unique feature of the SHM-7 is its dual outputs, each with a ±5V output voltage range at 30 mA and an output impedance of 13Ω. The outputs may be tied together to increase the output current and decrease the output impedance.

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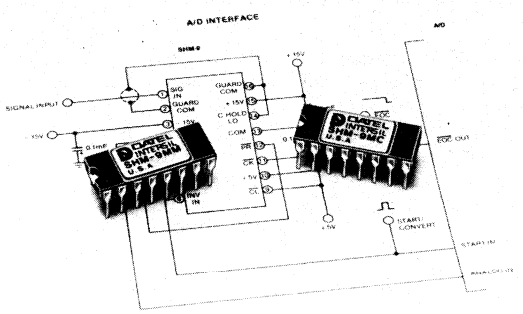

Low cost functionally complete hybrid sample-hold features .01% accuracy SHM-9

The SHM-9 is a complete, self-contained sample-hold amplifier that combines high performance versatility with low cost. The SHM-9 includes a bipolar input amplifier, a low-leakage electronic switch, a FET output amplifier, a precision 1000 pF hold capacitor and logic control circuitry. The internal control circuitry allows the SHM-9 to be interfaced with virtually any A/D converter using the converter's Start/Convert and E.O.C. (status) signals. Active laser trimming of highly stable thin-film resistor networks minimizes offset and sample-to-hold offset errors, eliminating the need for external adjustment circuits.

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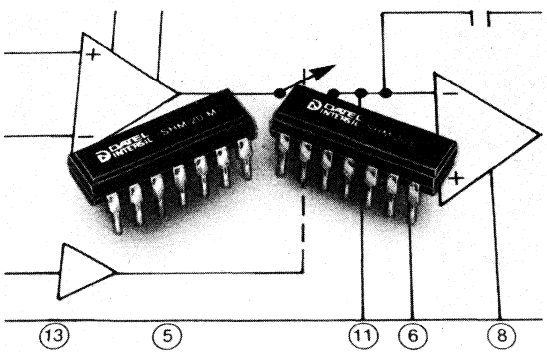
DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340



SHM-20, Fast, High Performance Sample and Hold Features Internal Hold Capacitor.

The SHM-20 is a complete monolithic sample and hold amplifier which includes an internal 100 pF MOS capacitor. Features include an acquisition time of typically 1.0 μS for a 10V input step to 0.01%. Aperture uncertainty is typically 1 nS and droop rate is as low as 0.08 μV/μS. Primarily designed for high speed analog signal processing applications, the SHM-20 combines monolithic reliability and size with high performance versatility and low cost. The SHM-20 is available for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges and is packaged in a 14 pin ceramic DIP.

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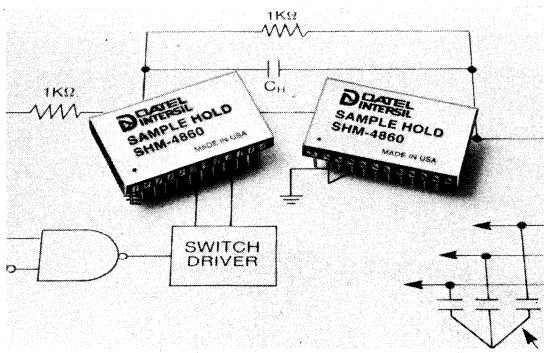

SHM-4860 new 0.01% Hybrid Sample-Hold features 200 nsec acquisition time

DATEL-INTERSIL's SHM-4860 is a high-speed, high resolution sample-hold amplifier manufactured with modern hybrid technology. Designed mainly for precision, high speed analog signal processing applications, the SHM-4860 acquires a 10V input change to ±0.01% in only 200 nsec max. Maximum sample-to-hold settling time is 100 nsec to ±0.01% with an aperture uncertainty of typically ±50 psec. Feedthrough attenuation is typically 74 dB. The digital inputs of the SHM-4860 are TTL compatible.

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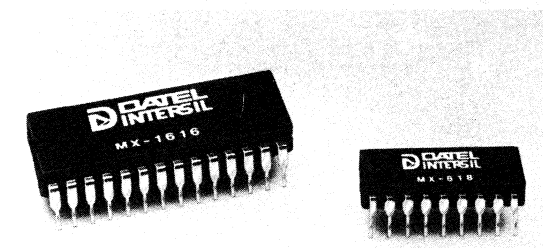

8 and 16 Channel Multiplexers Feature High Speed, High Accuracy, MX-1616, MX-818

DATEL-INTERSIL's MX-1616 and MX-818 are high speed, high performance analog multiplexers featuring transfer accuracies of 0.01% at sampling rates of up to 2.5 MHz over ±10V single ranges. The MX-1616 is user programmable either as a single-ended 16-channel or as a differential 8 channel multiplexer while the MX-818 is programmable as either a single-ended 8 channel or differential 4-channel multiplexer. All models feature an inhibit function, break-before-make switching and a maximum ON resistance of only 750Ω.

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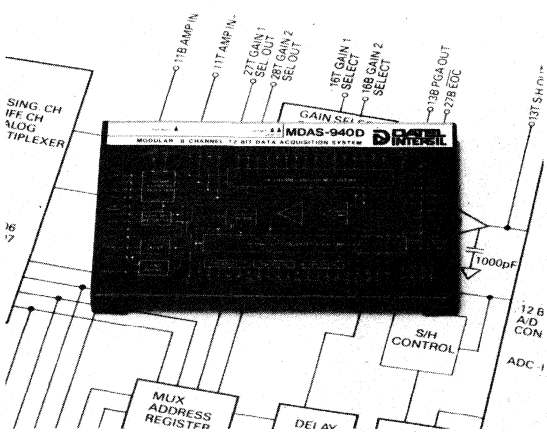

MDAS-940 12-bit, multichannel data acquisition subsystem features digital gain control

DATEL-INTERSIL's MDAS-940S and MDAS-940D are complete, self-contained data acquisition subsystems featuring 16-channel single-ended or 8-channel differential A/D inputs, respectively. Resolution is 12 binary bits with accuracy of ±0.025% at a throughput rate of 33 kHz. Both models contain a programmable gain instrumentation amplifier with digitally selectable gain ranges of 1, 2, 4 and 8. Gain selection is accomplished through the input of a two-bit word. The extensive use of hybrid and monolithic circuits reduces the parts count, increases reliability, and makes possible the small size and low cost of these modules.

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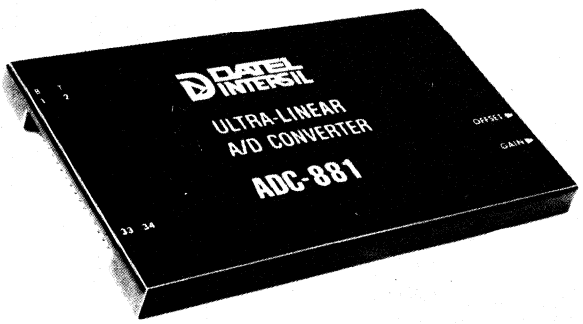
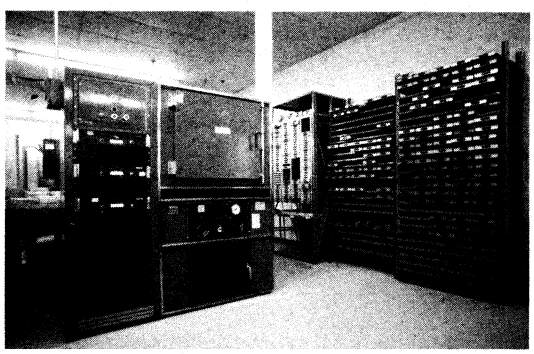
DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340


DATEL INTERSIL
ULTRA-LINEAR
A/D CONVERTER
ADC-881
OFFSET
GAIN



ANALOG TO DIGITAL CONVERTERS

Analog-To-Digital Converters

Counter Type A/D Converter

Analog-to-digital converters, also called ADC's or *encoders*, employ a variety of different circuit techniques to implement the conversion function. As with D/A converters, however, relatively few of these circuits are widely used today. Of the various techniques available, the choice depends on the resolution and speed required.

One of the simplest A/D converters is the *counter*, or *servo*, type. This circuit employs a digital counter to control the input of a D/A converter. Clock pulses are applied to the counter and the output of the D/A is stepped up one LSB at a time. A comparator compares the D/A output with the analog input and stops the clock pulses when they are equal. The counter output is then the converted digital word.

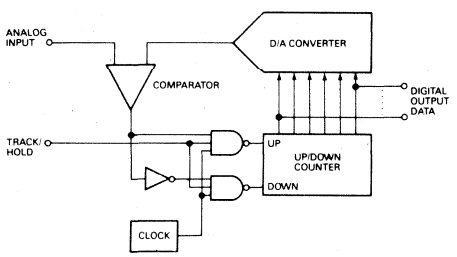


Figure 1. Tracking Type A/D Converter

While this converter is simple, it is also relatively slow. An improvement on this technique is shown in Figure 1 and is known as a *tracking* A/D converter, a device commonly used in control systems. Here an up-down counter controls the DAC, and the clock pulses are directed to the pertinent counter input depending on whether the D/A output must increase or decrease to reach the analog input voltage.

The obvious advantage of the tracking A/D converter is that it can continuously follow the input signal and give updated digital output data if the signal does not change too rapidly. Also, for small input changes, the conversion can be quite fast. The converter can be operated in either the track or hold modes by a digital input control.

Sucessive-Approximation A/D Converters

By far, the most popular A/D conversion technique in general use for moderate to high speed applications is the *successive-approximation* type A/D. This method falls into a class of techniques known as *feedback type* A/D converters, to which the counter type also belongs. In both cases a D/A converter is in the feedback loop of a digital control circuit which changes its ouput until it equals the analog input. In the case of the successive-approximation converter, the DAC is controlled in an optimum manner to complete a conversion in just n-steps, where n is the resolution of the converter in bits.

The operation of this converter is analogous to weighing an unknown on a laboratory balance scale using standard weights in a binary sequence such as 1, ½, ¼, ⅛, ... 1/n kilograms. The correct procedure is to begin with the largest standard weight and proceed in order down to the smallest one.

The largest weight is placed on the balance pan first; if it does not tip, the weight is left on and the next largest weight is added. If the balance does tip, the weight is removed and the next one added. The same procedure is used for the next largest weight and so on down to the smallest. After the nth standard weight has been tried and a decision made, the weighing is finished. The total of the standard weights remaining on the balance is the closest possible approximation to the unknown.

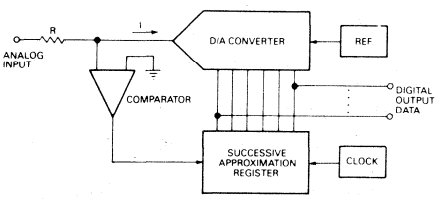


Figure 2. Successive Approximation A/D Converter

In the successive-approximation A/D converter illustrated in Figure 2, a successive-approximation register (SAR) controls the D/A converter by implementing the weighing logic just described. The SAR first turns on the MSB of the DAC and the comparator tests this output against the analog input. A decision is made by the comparator to leave the bit on or turn it off after which bit 2 is turned on and a second comparison made. After n-comparisons the digital output of the SAR indicates all those bits which remain on and produces the desired digital code. The clock circuit controls the timing of the SAR. Figure 3 shows the D/A converter output during a typical conversion.

The conversion efficiency of this technique means that high resolution conversions can be made in very short times. For example, it is possible to perform

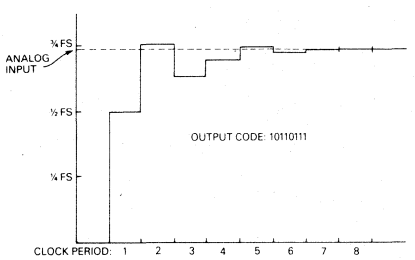


Figure 3. D/A Output for 8-Bit Successive Approximation Conversion

a 10 bit conversion in 1 μsec. or less and a 12 bit conversion in 2 μsec. or less. Of course the speed of the internal circuitry, in particular the D/A and comparator, are critical for high speed performance.

The Parallel (Flash) A/D Converter

For ultra-fast conversions required in video signal processing and radar applications where up to 8 bits resolution is required, a different technique is employed; it is known as the *parallel* (also *flash*, or *simultaneous*) method and is illustrated in **Figure 4.**

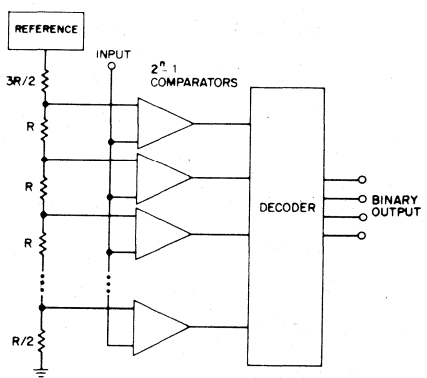


Figure 4. 4-Bit Parallel A/D Converter

This circuit employs 2^n-1 analog comparators to directly implement the quantizer transfer function of an A/D converter.

The comparator trip-points are spaced 1 LSB apart by the series resistor chain and voltage reference. For a given analog input voltage all comparators biased below the voltage turn on and all those biased above it remain off. Since all comparators change state simultaneously, the quantization process is a one-step operation.

A second step is required, however, since the logic output of the comparators is not in binary form.

Therefore an ultra-fast decoder circuit is employed to make the logic conversion to binary. The parallel technique reaches the ultimate in high speed because only two sequential operations are required to make the conversion.

The limitation of the method, however, is in the large number of comparators required for even moderate resolutions. A 4-bit converter, for example, requires only 15 comparators, but an 8-bit converter needs 255. For this reason it is common practice to implement an 8-bit A/D with two 4-bit stages as shown in Figure 5

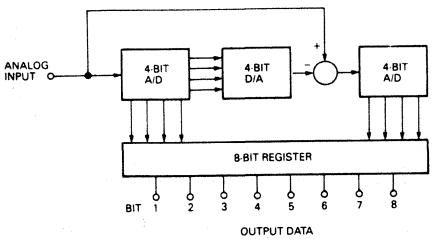


Figure 5. Two-Stage Parallel 8-Bit A/D Converter

The result of the first 4-bit conversion is converted back to analog by means of an ultra-fast 4-bit D/A and then subtracted from the analog input. The resulting residue is then converted by the second 4-bit A/D, and the two sets of data are accumulated in the 8-bit output register.

Converters of this type achieve 8-bit conversions at rates of 20 MHz and higher, while single stage 4-bit conversions can reach 50 to 100 MHz rates.

Integrating Type A/D Converters

Indirect A/D Conversion

Another class of A/D converters known as integrating type operates by an indirect conversion method. The unknown input voltage is converted into a time period which is then measured by a clock and counter. A number of variations exist on the basic principle such as *single-slope*, *dual-slope*, and *triple-slope* methods. In addition there is another technique—completely different—which is known as the *charge-balancing* or *quantized feedback* method.

The most popular of these methods are dual-slope and charge-balancing; although both are slow, they have excellent linearity characteristics with the capability of rejecting input noise. Because of these characteristics, integrating type A/D converters are almost exclusively used in digital panel meters, digital multimeters, and other slow measurement applications.

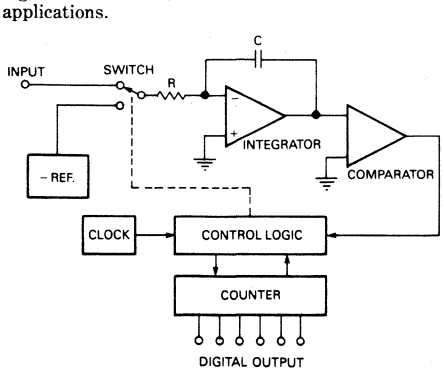


Figure 6. Dual Slope A/D Converter

Dual-Slope A/D Conversion

The dual-slope technique, shown in Figure 6, is perhaps best known. Conversion begins when the unknown input voltage is switched to the integrator input; at the same time the counter begins to count clock pulses and counts up to overflow. At this point the control circuit switches the integrator to the negative reference voltage which is integrated until the output is back to zero. Clock pulses are counted during this time until the comparator detects the zero crossing and turns them off.

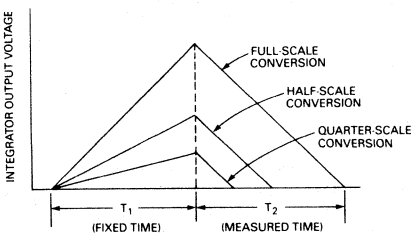


Figure 7. Integrator Output Waveform for Dual Slope A/D Converter

The counter output is then the converted digital word. Figure 7 shows the integrator output waveform where T_1 is a fixed time and T_2 is a time proportional to the input voltage. The times are related as follows:

$$T_2 = T_1 \frac{E_{IN}}{V_{REF}}$$

The digital output word therefore represents the ratio of the input voltage to the reference.

Dual-slope conversion has several important features. First, conversion accuracy is independent of the stability of the clock and integrating capacitor so long as they are constant during the conversion period. Accuracy depends only on the reference accuracy and the integrator circuit linearity. Second, the noise rejection of the converter can be infinite if T_1 is set to equal the period of the noise. To reject 60 Hz power noise therefore requires that T_1 be 16.667 msec. Figure 8 shows digital panel meters which employ dual slope A/D converters.

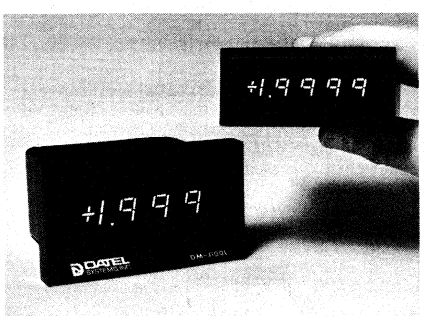


Figure 8. Digital Panel Meters Which Employ Dual Slope A/D Converters

Charge-Balancing A/D Conversion

The charge-balancing, or quantized feedback, method of conversion is based on the principle of generating a pulse train with frequency proportional to the input voltage and then counting the pulses for a fixed period of time. This circuit is shown in Figure 9. Except for the counter and timer, the circuit is a *voltage-to-frequency* (V/F) converter which generates an output pulse rate proportional to input voltage.

The circuit operates as follows. A positive input voltage causes a current to flow into the operational integrator through R_1. This current is integrated, producing a negative going ramp at the output. Each time the ramp crosses zero the comparator output triggers a precision pulse generator which puts out a constant width pulse.

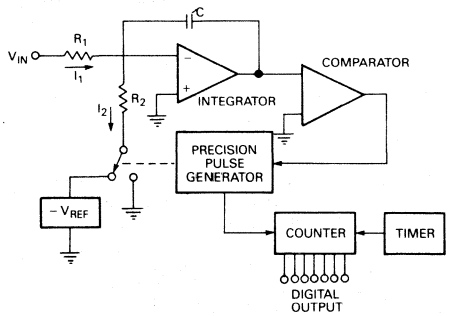


Figure 9. Charge-Balancing A/D Converter

The pulse output controls switch S_1 which connects R_2 to the negative reference for the duration of the pulse. During this time a pulse of current flows out of the integrator summing junction, producing a fast, positive ramp at the integrator output. This process is repeated, generating a train of current pulses which exactly balances the input current—hence the name charge balancing. This balance has the following relationship:

$$f = \frac{1}{\tau} \frac{V_{IN}}{V_{REF}} \frac{R_2}{R_1}$$

where τ is the pulse width and f the frequency.

A higher input voltage therefore causes the integrator to ramp up and down faster, producing higher frequency output pulses. The timer circuit sets a fixed time period for counting. Like the dual-slope converter, the circuit also integrates input noise, and if the timer is synchronized with the noise frequency, infinite rejection results. Figure 10 shows the noise rejection characteristic of all integrating type A/D converters with rejection plotted against the ratio of integration period to noise period.

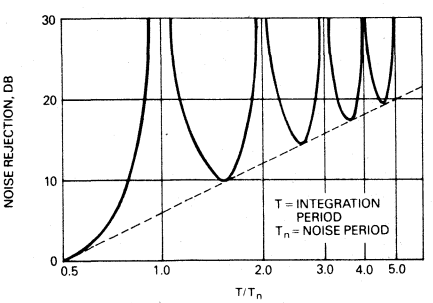


Figure 10. Noise Rejection for Integrating Type A/D Converters

Glossary of analog-to-digital conversion Terms

ABSOLUTE ACCURACY: The worst-case input to output error of a data converter referred to the NBS standard volt.

ACCURACY: The conformance of a measured value with its true value; the maximum error of a device such as a data converter from the true value. See *relative accuracy* and *absolute accuracy.*

ADC: Abbreviation for analog-to-digital converter. See *A/D converter.*

A/D CONVERTER: Analog-to-digital converter. A circuit which converts an analog (continuous) voltage or current into an output digital code.

BCD: See *Binary Coded Decimal.*

BINARY CODE: See *Natural Binary Code.*

BINARY CODED DECIMAL (BCD): A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

BIPOLAR MODE: For a data converter, when the analog signal range includes both positive and negative values.

BIPOLAR OFFSET: The analog displacement of one half of full scale range in a data converter operated in the bipolar mode. The offset is generally derived from the converter reference circuit.

CHARGE BALANCING A/D CONVERTER: An analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator, and the resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also called *quantized-feedback.*

CLOCK: A circuit in an A/D converter that generates timing pulses which synchronize the operation of the converter.

CLOCK RATE: The frequency of the timing pulses of the clock circuit in an A/D converter.

COMPANDING CONVERTER: An A/D or D/A converter which employs a logarithmic transfer function to expand or compress the analog signal range. These converters have large effective dynamic ranges and are commonly used in digitized voice communication systems.

COMPLEMENTARY BINARY CODE: A binary code which is the logical complement of straight binary. All 1's become 0's and vice versa.

CONVERSION TIME: The time required for an A/D converter to complete a single conversion to specified resolution and linearity for a full scale analog input change.

CONVERSION RATE: The number of repetitive A/D or D/A conversions per second for a full scale change to specified resolution and linearity.

COUNTER TYPE A/D CONVERTER: A feedback method of A/D conversion whereby a digital counter drives a D/A converter which generates an output ramp which is compared with the analog input. When the two are equal, a comparator stops the counter and output data is ready. Also called a *servo type* A/D converter.

DATA CONVERTER: An A/D or D/A Converter.

DATA WORD: A digital code-word that represents data to be processed.

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of $FSR/2^n$.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

DIGITIZER: A device which converts analog into digital data; an A/D converter.

DUAL SLOPE A/D CONVERTER: An indirect method of A/D conversion whereby an analog voltage is converted into a time period by an integrator and reference and then measured by a clock and counter. The method is relatively slow but capable of high accuracy.

DYNAMIC ACCURACY: The total error of a data converter or conversion system when operated at its maximum specified conversion rate or throughput rate.

DYNAMIC RANGE: The ratio of full scale range (FSR) of a data converter to the smallest difference it can resolve. In terms of converter resolution:

$$\text{Dynamic Range (DR)} = 2^n$$

It is generally expressed in dB:

$$DR = 20 \log_{10} 2^n = 6.02n$$

where n is the resolution in bits.

ENCODER: A communications term for an A/D converter.

E.O.C.: End of Conversion. See *Status Output.*

FEEDBACK TYPE A/D CONVERTER: A class of analog-to-digital converters in which a D/A converter is enclosed in the feedback loop of a digital control circuit which changes the D/A output until it equals the analog input.

FSR: Full Scale Range.

FLASH TYPE A/D CONVERTER: See *Parallel A/D Converter.*

FULL SCALE RANGE (FSR): the difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

HYSTERESIS ERROR: The small variation in analog transition points of an A/D converter whereby the transition level depends on the direction from which it is approached. In most A/D converters this hysteresis is very small and is caused by the analog comparator.

INDIRECT TYPE A/D CONVERTER: A class of analog-to-digital converters which converts the unknown input voltage into a time period and then measures this period.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTEGRATING A/D CONVERTER: One of several types of A/D conversion techniques whereby the analog input is integrated with time. This includes dual slope, triple slope, and charge balancing type A/D converters.

LEAST SIGNIFICANT BIT (LSB): The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution:

$$\text{LSB Size} = \frac{FSR}{2^n}$$

where FSR is full scale range and n is the resolution in bits.

LINEARITY ERROR: See *Integral Linearity Error* and *Differential Linearity Error.*

LONG TERM STABILITY: The variation in data converter accuracy due to time change alone. It is commonly specified in percent per 1000 hours or per year.

LOW-LEVEL MULTIPLEXING: An analog multiplexing system in which a low amplitude signal is first multiplexed and then amplified.

LSB: Least Significant Bit.

LSB SIZE: See *Quantum.*

MAJOR CARRY: See *Major Transition.*

MAJOR TRANSITION: In a data converter, the change from a code of 1000...000 to 0111...1111 or vice-versa. This transition is the most difficult one to make from a linearity standpoint since the MSB weight must ideally be precisely one LSB larger than the sum of all other bit weights.

MISSING CODE: In an A/D converter, the characteristic whereby not all output codes are present in the transfer function of the converter. This is caused by a nonmonotonic D/A converter inside the A/D.

MONOTONICITY: For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. *Nonmonotonicity* may occur if the converter differential linearity error exceeds ±½ LSB.

MOST SIGNIFICANT BIT (MSB): The leftmost bit in a data converter code. It has the largest weight, equal to one half of full scale range.

MSB: Most Significant Bit.

NATURAL BINARY CODE: A positive weighted code in which a number is represented by

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \ldots + a_n 2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n}$$

and N has a fractional value between zero and one.

NOISE REJECTION: The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type A/D converters.

NORMAL-MODE REJECTION: The attenuation of a specific frequency or band of frequencies appearing directly across two electrical terminals. In A/D converters, normal-mode rejection is determined by an input filter or by integration of the input signal.

OFFSET BINARY CODE: Natural binary code in which the code word 0000....0000 is displaced by one-half analog full scale. The code represents analog values between −FS and +FS (full scale). The code word 1000....0000 then corresponds to analog zero.

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

OFFSET ERROR: The error at analog zero for a data converter operating in the bipolar mode.

ONE'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all one's.

PARALLEL TYPE A/D CONVERTER: An ultra-fast method of A/D conversion which uses an array of $2^n - 1$ comparators to directly implement a quantizer, where n is the resolution in bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

PROPAGATION TYPE A/D CONVERTER: A type of A/D conversion method which employs one comparator per bit to achieve ultra-fast A/D conversion. The conversion propagates down the series of cascaded comparators.

POWER SUPPLY SENSITIVITY: The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

PRECISION: The degree of repeatability, or reproducibility of a series of successive measurements. Precision is affected by the noise, hysteresis, time, and temperature stability of a data converter or other device.

QUANTIZATION NOISE: See *Quantization Error.*

QUANTIZATION UNCERTAINTY: See *Quantization Error.*

QUANTIZED FEEDBACK A/D CONVERTER: See *Charge Balancing A/D Converter.*

QUANTIZER: A circuit which transforms a continuous analog signal into a set of discrete output states. Its transfer function is the familiar staircase function.

QUANTIZING ERROR: The inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process. The quantized value is uncertain by up to ±Q/2 where Q is the quantum size. This error can be reduced only by increasing the resolution of the converter. Also called *quantization uncertainty* or *quantization noise.*

QUANTUM: The analog difference between two adjacent codes for an A/D or D/A converter. Also called *LSB size.*

R-2R LADDER NETWORK: An array of matched resistors with series values of R and shunt values of 2R in a standard ladder circuit configuration.

RATIOMETRIC A/D CONVERTER: An analog-to-digital converter which uses a variable reference to measure the ratio of the input voltage to the reference.

RELATIVE ACCURACY: The worst case input to output error of a data converter, as a percent of full scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

RESOLUTION: The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

SAR: Successive approximation register. A digital control circuit used to control the operation of a successive approximation A/D converter.

SCALE FACTOR ERROR: See *Gain Error.*

SERVO-TYPE A/D CONVERTER: See *Counter-Type A/D Converter.*

SHORT CYCLING: The termination of an A/D conversion process at a resolution less than the full resolution of the converter. This results in a shorter conversion time for reduced resolution in A/D converters with a short cycling capability.

SIGN-MAGNITUDE BCD: A binary coded decimal code in which a sign bit is added to distinguish positive from negative in bipolar operation.

SIGN-MAGNITUDE BINARY CODE: The natural binary code to which a sign bit is added to distinguish positive from negative in bipolar operation.

SIMULTANEOUS TYPE A/D CONVERTER: See *Parallel Type A/D Converter.*

SINGLE-SLOPE A/D CONVERTER: A simple A/D converter technique in which a ramp voltage generated from a voltage reference and integrator is compared with the analog input voltage by a comparator. The time required for the ramp to equal the input is measured by a clock and counter to produce the digital output word.

SKIPPED CODE: See *Missing Code.*

SPAN: For an A/D or D/A converter, the full scale range or difference between maximum and minimum analog values.

START-CONVERT: The input pulse to an A/D converter which initiates conversion.

STATIC ACCURACY: The total error of a data converter or conversion system under DC input conditions.

STATUS OUTPUT: The logic output of an A/D converter which indicates whether the device is in the process of making a conversion or the conversion has been completed and output data is ready. Also called *busy output* or *end of conversion* output.

STRAIGHT BINARY CODE: See *Natural Binary Code.*

SUCCESSIVE APPROXIMATION A/D CONVERTER: An A/D conversion method that compares in sequence a series of binary weighted values with the analog input to produce an output digital word in just n steps, where n is the resolution in bits. The process is efficient and is analogous to weighing an unknown quantity on a balance scale using a set of binary standard weights.

TEMPERATURE COEFFICIENT: The change in analog magnitude with temperature, expressed in ppm/°C.

THREE-STATE OUTPUT: A type of A/D converter output used to connect to a data bus. The three output states are logic 1, logic 0, and off. An *enable* control turns the output on or off.

TRACKING A/D CONVERTER: A counter-type analog-to-digital converter which can continuously follow the analog input at some specified maximum rate and continuously update its digital output as the input signal changes. The circuit uses a D/A converter driven by an up-down counter.

TRANSFER FUNCTION: The input to output characteristic of a device such as a data converter expressed either mathematically or graphically.

TRIPLE-SLOPE A/D CONVERTER: A variation on the dual slope type A/D converter in which the time period measured by the clock and counter is divided into a coarse (fast slope) measurement and a fine (slow slope) measurement.

TWO'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all zero's plus a carry.

TWO-STAGE PARALLEL A/D CONVERTER: An ultra-fast A/D converter in which two parallel type A/D's are operated in cascade to give higher resolution. In the usual case a 4-bit parallel converter first makes a conversion; the resulting output code drives an ultra-fast 4-bit D/A, the output of which is subtracted from the analog input to form a residual. This residual then goes to a second 4 bit parallel A/D. The result is an 8 bit word converted in two steps.

UNIPOLAR MODE: In a data converter, when the analog range includes values of one polarity only.

VIDEO A/D CONVERTER: An ultra-fast A/D converter capable of conversion rates of 5 MHz and higher. Resolution is usually 8 bits but can vary depending on the application. Conversion rates of 20 MHz and higher are common.

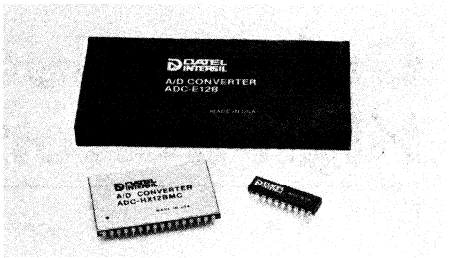
ZERO DRIFT: The change with temperature of analog zero for a data converter operating in the unipolar mode. It is generally expressed in μV/°C.

ZERO ERROR: The error at analog zero for a data converter operating in the unipolar mode.

Quick Selection: General-Purpose A/D Converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX	LINEARITY ERROR, MAX	ANALOG INPUT VOLTAGE RANGE
	ADC-E8B	Fast Dual Slope	8 Bits	312 μs	± ½ LSB	± 1V, ± 5V, ± 10V
	ADC-E10B		10 Bits	1.23 ms		
	ADC-E12B		12 Bits	5.0 ms		
	ADC-E8D		2½ Digits	500 μs		± 2V, ± 10V, ± 20V
	ADC-E12D		3½ Digits	5.0 ms		
	ADC-ECONOVERTER	Low-cost Counter Type	6 Bits	50 μs	± ½ LSB	0 to + 5V, 0 to + 10V ± 2.5V, ± 5V
	ADC-EK8B	Low-cost Low-power Integrating	8 Bits	1.8 ms	± ½ LSB	0 to + 10V ± 5V
	ADC-EK10B		10 Bits	6 ms		
	ADC-EK12B		12 Bits	24 ms		
	ADC-EK12DC		3½ Digits	12 ms		0 to + 10V
	ADC-EK12DR					
	ADC-EK12DM					
	ADC-ET8BC	Low-cost Three-state Outputs	8 Bits	1.8 ms	± ½ LSB	0 to + 10V ± 5V
	ADC-ET8BM					
	ADC-ET10BC		10 Bits	6 ms		
	ADC-ET10BM					
	ADC-ET12BC		12 Bits	24 ms	± 1 ½ LSB	
	ADC-ET12BR				± ½ LSB	
	ADC-ET12BM					
	ADC-HX12BGC	Input Buffer Amp	12 Bits	20 μs	± ½ LSB	0 to + 5V, 0 to + 10V ± 2.5V, ± 5V, ± 10V
	ADC-HX12BMC					
	ADC-HX12BMR					
	ADC-HX12BMM					
	ADC-L8B2	Moderate Speed Successive Approx. A/D	8 Bits	12 μs	± ½ LSB	0 to + 5V, 0 to + 10V ± 5V, ± 10V
	ADC-L10B2		10 Bits	16 μs		
	ADC-L12B2		12 Bits	20 μs		
	ADC-L8D2		2 Digits	12 μs		0 to + 5V, 0 to + 10V
	ADC-L12D2		3 Digits	20 μs		
	ADC-M8B2	Complete, Modular Successive Approx. A/D	8 Bits	4 μs	± ½ LSB	0 to + 5V, 0 to + 10V ± 5V, ± 10V
	ADC-M10B2		10 Bits	11.5 μs		
	ADC-M12B2		12 Bits	13 μs		
	ADC-M8D2		2 Digits	4 μs		0 to + 5V, 0 to + 10V
	ADC-M12D2		3 Digits	13 μs		
	ADC-MA10B2A	Moderate Speed General Purpose Modules	10 Bits	40 μs	± ½ LSB	0 to + 5V, 0 to + 10V ± 5V, ± 10V
	ADC-MA10B2B			20 μs		
	ADC-MA12B2A		12 Bits	40 μs		
	ADC-MA12B2B			20 μs		
	ADC-MC8BC	Multi-function A/D - D/A	8 Bits	500 μs	± ½ LSB	0 to + 2.5V, 0 to + 5V 0 to + 10V
	ADC-MC8BM					
	ADC-89A8B	General Purpose Counter Type Module	8 Bits	200 μs	± ½ LSB	0 to + 10V, ± 5V
	ADC-89A8D		2 Digits	100 μs		0 to + 10V
NEW	ADC-830C	μP Compatible Three-state Outputs	8 Bits	100 μs	± ½ LSB	0 to + 5V
NEW	ADC-847A, B	μP Compatible Three-State Outputs	8 Bits	9 μsec	±1(A), ±¼(B)LSB	− 0.5V to + 3.5V
NEW	ADC-847M				± ¼ LSB	
	ADC-856C	Tracking A/D Latched Outputs	10 Bits	1 μs/LSB	± ½ LSB	0 to + 5V, 0 to + 10V ± 2.5V, ± 5V, ± 10V
	ADC-856M					

DATEL-INTERSIL offers a wide range of moderate performance, general purpose analog to digital converters. A new entry in this category is the ADC-830, a low-cost, microprocessor-compatible, 8-bit A/D. The ADC-830 appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic.



OUTPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
Sign Mag. Binary Sign Mag. BCD	50 ppm/°C	4 x 2 x 0.4 in (102 x 51 x 10 mm)	Module	0 to +70	24
Binary	100 ppm/°C	2 x 2 x 0.375 in (51 x 51 x 10 mm)	Module	0 to +70	—
Binary BCD	25 ppm/°C	24-pin DIP	Monolithic	0 to +70 0 to +70 −25 to +85 −55 to +125	32
Binary	25 ppm/°C	24-pin DIP	Monolithic	0 to +70 −55 to +125 0 to +70 −55 to +125 0 to +70 −25 to +85 −55 to +125	36
C Binary C 2C	20 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70 0 to +70 −25 to +85 −55 to +125	50
Binary 2C BCD	10 ppm/°C	3 x 2 x 0.375 in 4 x 2 x 0.4 in (102 x 51 x 10 mm)	Module	0 to +70	—
Binary 2C BCD	10 ppm/°C	4 x 2 x 0.4 in (102 x 51 x 10 mm)	Module	0 to +70	—
Binary 2C	30 ppm/°C	4 x 2 x 0.4 in (102 x 57 x 10 mm)	Module	0 to +70	—
Binary	10 ppm/°C	16-pin DIP	Monolithic	0 to +70 −55 to +125	—
Binary BCD	50 ppm/°C	3 x 2 x 0.375 in (76 x 51 x 10 mm)	Module	0 to +70	—
Binary	— — —	20-pin DIP	Monolithic	0 to +70	78
Binary	— — —	18-pin DIP	Monolithic	0 to +70 −55 to +125	90
Binary	40 ppm/°C	28-pin DIP	Monolithic	0 to +70 −55 to +125	94

Quick selection: High-performance A/D converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX	LINEARITY ERROR, MAX	ANALOG INPUT VOLTAGE RANGE
	ADC-HC12BMC	Low-power CMOS A/D	12 Bits	300 μs	± ½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-HC12BMR					
	ADC-HC12BMM					
	ADC-HS12BMC	Internal S/H	12 Bits	9 μs	± ½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-HS12BMR					
	ADC-HS12BMM					
	ADC-HZ12BGC	Input Buffer Amplifier	12 Bits	8 μs	± ½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-HZ12BMC					
	ADC-HZ12BMR					
	ADC-HZ12BMM					
NEW	ADC-84-10	Industry Standard Military and Industrial A/D's	10 Bits	6 μs	± ½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
NEW	ADC-84-12		12 Bits	10 μs		
NEW	ADC-85C-10		10 Bits	6 μs		
NEW	ADC-85C-12		12 Bits	10 μs		
NEW	ADC-85-10		10 Bits	6 μs		
NEW	ADC-85-12		12 Bits	10 μs		
NEW	ADC-87-10		10 Bits	6 μs		
NEW	ADC-87-12		12 Bits	10 μs		
	ADC-149-14B	High Resolution Modular A/D	14 Bits	50 μs	± ½ LSB	0 to −10V, 0 to −20V ±5V, ±10V
	ADC-825MC	No Calibration Required	8 Bits	1 μs	± ½ LSB	0 to +5V, 0 to +10V 0 to +20V, ±2.5V ±5V, ±10V
	ADC-825MR					
	ADC-825MM					
	ADC-826MC	Fast Successive Approximation 10-Bit A/D	10 Bits	1.4 μs	± ½ LSB	0 to −5V, 0 to −10V 0 to −20V, ±2.5V ±5V, ±10V
	ADC-826MR					
	ADC-826MM					
	ADC-827MC	Fast Successive Approximation 12-Bit A/D	12 Bits	3 μs	± ½ LSB	0 to −5V, 0 to −10V ±2.5V, ±5V, ±10V
	ADC-827MR					
	ADC-827MM					
	ADC-881	Ultra-linear	8 Bits	1.5 μs	±0.04 LSB	±5V
NEW	ADC-5210	Low-cost Industry Standard Converters Absolute Accuracy Over Temperature Only 0.2% FSR Maximum	12 Bits	13 μs	± ½ LSB	0 to −10V
NEW	ADC-5210E					
NEW	ADC-5210H					
NEW	ADC-5211					±5V
NEW	ADC-5211E					
NEW	ADC-5211H					
NEW	ADC-5212					±10V
NEW	ADC-5212E					
NEW	ADC-5212H					
NEW	ADC-5213					0 to −10V
NEW	ADC-5213E					
NEW	ADC-5213H					
NEW	ADC-5214					±5V
NEW	ADC-5214E					
NEW	ADC-5214H					
NEW	ADC-5215					±10V
NEW	ADC-5215E					
NEW	ADC-5215H					
NEW	ADC-5216					0 to +10V
NEW	ADC-5216E					
NEW	ADC-5216H					
NEW	ADC-7109	High performance μp compatible 12 bit A/D	12 Bits	33 msec	1 count	V+ to V−

This extensive line of high-performance analog to digital converters includes models optimized for low power, high resolution and ultra-linear operation. New additions to this model line include the industry standard ADC-84/85/87 series of military and industrial A/D conveters. Each model in this series is available in two performance grades; 12 bits with a maximum conversion time of 10 μs and 10 bits with a 6 μs maximum conversion rate.

The ADC-5210 series are industry standard, 12-bit, adjustment-free A/D converters offering improved performance at lower cost. Absolute error over the full military operating temperature range is only ±0.2% maximum, one-half that of competing units.

INPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
Binary 2C	30 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	42
				−25 to +85	
				−55 to +125	
C Binary C2C	20 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	46
				−25 to +85	
				−55 to +125	
C Binary C2C	20 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	50
				0 to +70	
				−25 to +85	
				−55 to +100	
C Binary C2C	30 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	54
	40 ppm/°C			0 to +70	
	25 ppm/°C				
	20 ppm/°C			−25 to +85	
	15 ppm/°C				
	20 ppm/°C			−55 to +125	
Binary 2C	15 ppm/°C	4 x 2 x 0.8 in (102 x 51 x 20 mm)	Module	0 to +70	60
Binary 2C	20 ppm/°C	24-pin Ceramic DIP	Hybrid	0 to +70	66
				−25 to +85	
				−55 to +125	
Binary 2C	37 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	70
				−25 to +85	
				−55 to +125	
Binary 2C	25 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	74
				−25 to +85	
				−55 to +125	
Binary	30 ppm/°C	5 x 3 x 0.375 in	Module	0 to +70	102
C Binary	10 ppm/°C	24-pin Ceramic DIP	Hybrid	0 to +70	110
				−25 to +85	
				−55 to +125	
				0 to +70	
				−25 to +85	
				−55 to +125	
				0 to +70	
				−25 to +85	
				−55 to +125	
	3 ppm/°C			0 to +70	
				−25 to +85	
				−55 to +125	
				0 to +70	
				−25 to +85	
				−55 to +125	
	10 ppm/°C			0 to +70	
				−25 to +85	
				−55 to +125	
Binary	5 ppm/°C	40 Pin Plastic DIP	Hybrid	0°C to +70°C	116

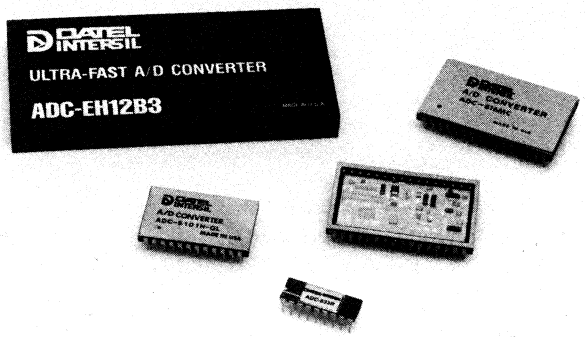
Quick selection: High-speed A/D converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX	LINEARITY ERROR, MAX	ANALOG INPUT VOLTAGE RANGE
	ADC-EH8B1	High-speed Low-profile Case Parallel and Serial outputs	8 Bits	4 μs	± ½ LSB	0 to + 10V ± 5V
	ADC-EH8B2			2 μs		
	ADC-EH10B1		10 Bits	4 μs		
	ADC-EH10B2			2 μs		
	ADC-EH12B1		12 Bits	8 μs		
	ADC-EH12B2			4 μs		
	ADC-EH12B3			2 μs		
	ADC-G8B	Compact, High Speed Module	8 Bits	800 ns	± ½ LSB	0 to − 5V, 0 to − 10V ± 5V, ± 10V
	ADC-G10B		10 Bits	1 μs		
	ADC-HU3BMC	Ultra-fast Flash A/D	3 Bits	20 ns	0.1%	± 2.1V
	ADC-HU3BMR					
	ADC-HU3BMM					
	ADC-SH4B	Internal S/H	4 Bits	500 ns	± ⅓ LSB	0 to + 1V
	ADC-TV8B1	20 MHz Video Speed A/D	8 Bits	50 ns	± ½ LSB	0 to + 1V, + 2V, + 5V ± 1V, ± 2V, ± 5V
	ADC-TV8B2					
	ADC-UH4B	Ultra-fast Flash A/D	4 Bits	40 ns	± ½ LSB	0 to − 2.56V ± 1.28V
	ADC-UH4B2					
	ADC-UH8B		8 Bits	100 ns	± 1 LSB	0 to − 2.56V ± 1.28V
	ADC-UH8B2					
NEW	ADC-810MC	High Speed 12 Bit A/D	12 Bits	2 μsec	± ½ LSB	0 to + 10V 0 to + 20V ± 5V, ± 10V
NEW	ADC-810MR					
NEW	ADC-810MM					
NEW	ADC-811MC	Fast 12 Bit A/D	12 Bits	4 μsec	± ½ LSB	0 to + 10V 0 to + 20V ± 5V, ± 10V
NEW	ADC-811MR					
NEW	ADC-811MM					
	ADC-815MC	Ultra-fast No Calibration Required	8 Bits	700 ns	± ½ LSB	0 to + 5V, 0 to + 10V 0 to + 20V ± 2.5V, ± 5V, ± 10V
	ADC-815MR					
	ADC-815MM					
	ADC-816MC	Ultra-fast	10 Bits	800 ns	± ½ LSB	0 to − 5V, 0 to − 10V 0 to − 20V ± 2.5V, ± 5V, ± 10V
	ADC-816MR					
	ADC-816MM			975 ns		
	ADC-817MC	Ultra-fast	12 Bits	2 μs	± ½ LSB	0 to − 5V, 0 to − 10V ± 2.5V, ± 5V, ± 10V
	ADC-817MR					
	ADC-817MM					
NEW	ADC-833R	Ultra-fast Low-power Flash A/D	6 Bits	66.6 ns	± 0.8 LSB	+ 2.5V to + 10V
NEW	ADC-868	Ultra-fast 12 Bit module	12 Bits	500 nsec	± ½ LSB	0 to 5V ± 2.5V
NEW	ADC-5101	High Temp. Performance at Low-cost	8 Bits	900 ns	± ½ LSB	0 to − 5V, − 10V, − 20V 0 to + 5V, + 10V, + 20V ± 2.5V, ± 5V, ± 10V
NEW	ADC-5101E					
NEW	ADC-5101H					

DATEL-INTERSIL manufactures a comprehensive line of high-speed successive approximation and parallel or flash analog to digital converters capable of thousands to millions of conversion per second.

New additions to this line include the ADC-5101, an industry standard A/D capable of an 8-bit conversion in 900 ns. DATEL-INTERSIL's ADC-5101 is the only 5101 type converter to offer operation over the full military temperature range.

The ADC-833 is a video-speed, low-power, 6-bit flash A/D converter. The ADC-833 is capable of digitizing an analog input at conversion rates up to 15 MHz while its power consumption is only 200 mW.



OUTPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
Binary 2C	50 ppm/°C	2 x 2 x 0.375 in (51 x 51 x 10 mm)	Module	0 to +70	24
	30 ppm/°C	3 x 2 x 0.375 in (76 x 51 x 10 mm)			
		4 x 2 x 0.375 in (102 x 51 x 10 mm)			
Binary 2C	25 ppm/°C	4 x 2 x 0.4 in	Module	0 to +70	—
		4 x 2 x 0.8 in			
Binary	25 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	—
				−25 to +85	
				−55 to +125	
Binary	200 ppm/°C	2 x 2 x 0.375 in	Module	0 to +70	—
Binary (ECL) Binary (TTL)	60 ppm/°C	7.5 x 4.25 x 0.875 in (191 x 108 x 22 mm)	Module	0 to +70	—
Binary	50 ppm/°C	5 x 3 x 1.15 in (167 x 76 x 29 mm)	Module	0 to +70	—
C Binary C2C	20 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	62
				−25 to +85	
				−55 to +125	
C Binary C2C	20 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	62
				−25 to +85	
				−55 to +125	
Binary 2C	20 ppm/°C	24-pin Ceramic DIP	Hybrid	0 to +70	66
				−25 to +85	
				−55 to +125	
Binary 2C	38 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	70
				−25 to +85	
				−55 to +125	
Binary 2C	25 ppm/°C	32-pin Ceramic DIP	Hybrid	0 to +70	74
				−25 to +85	
				−55 to +125	
Binary	25 ppm/°C	24-pin DIP	Monolithic	−25 to +85	84
Binary	±30 ppm/°C	4 × 6 × 0.375	Module	0°C to +70°C	98
Binary	— — — —	24-pin Ceramic DIP	Hybrid	0 to +70	106
				−25 to +85	
				−55 to +125	

Fast, 8 Bit Analog-to-Digital Converters ADC-EH8B

FEATURES

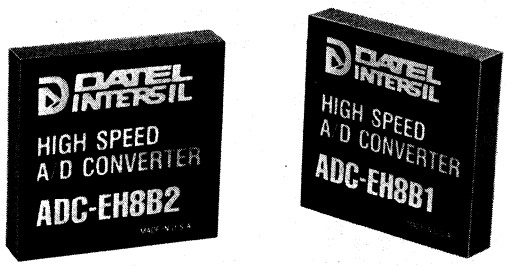
- 8 Bit Resolution
- 4.0 & 2.0 μsec. Conversion Time
- Unipolar or Bipolar Operation
- Parallel & Serial Outputs
- Low Cost

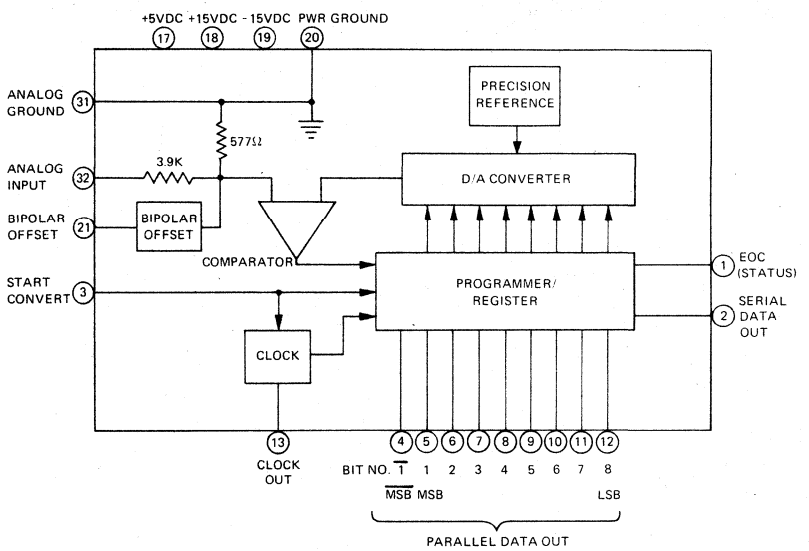
GENERAL DESCRIPTION

The model ADC-EH8B is a fast, 8 bit successive approximation type analog to digital converter in a compact 2 x 2 x .375 inch module. These converters are low cost devices with application in pulse code modulation systems and instrumentation and control systems requiring fast data conversion rates up to 500,000 per second. There are two models to choose from based on conversion speed: ADC-EH8B1 with a conversion time of 4.0 μsec. (250 kHz rate), and ADC-EH8B2 with a conversion time of 2.0 μsec. (500 kHz rate).

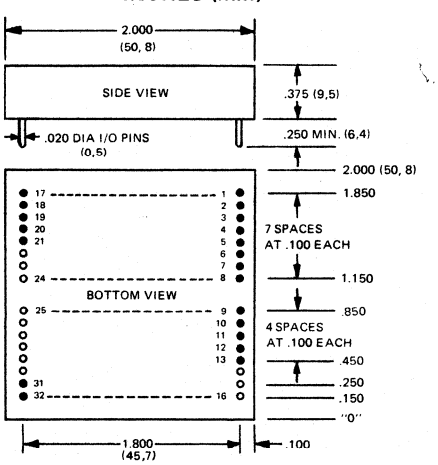
The high speed in a small size is made possible by the use of an MSI integrated circuit which provides all the necessary successive approximation logic, along with other new integrated circuit components. The analog input range is either unipolar 0 to +10V or bipolar -5V to +5V, determined by external pin connection. For unipolar operation no external adjustments are necessary; for bipolar operation only a bipolar offset adjustment must be made externally. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight or offset binary coding. Other outputs are clock output for synchronization with serial data, and $\overline{\text{MSB}}$ output for two's complement coding.

Other specifications include full scale temperature coefficient of 50 ppm/°C max., long term stability of .05%/year, and linearity of ±1/2 LSB. Power requirement is ±15VDC and +5VDC.





MECHANICAL DIMENSIONS INCHES (MM)



NOTES
1. Open dots designate omitted pins.
2. 0.100 inch = 2.5 mm, 0.150 inch = 3.8 mm.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	SERIAL DATA OUTPUT
3	START CONVERT
4	$\overline{\text{BIT 1 OUT (MSB)}}$
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT (LSB)
13	CLOCK OUT
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	BIPOLAR OFFSET
31	ANALOG GROUND
32	ANALOG INPUT

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-EH8B

(Typical at 25° C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	4.45K ohms ±50 ohms
Input Overvoltage	±20V (no damage)
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <50 ns. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Output Data	8 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar Operation	Straight Binary, positive true
Bipolar Operation	Offset Binary, positive true. Two's Complement, positive true.
Serial Output Data	NRZ successive decision pulse output generated during conversion, with MSB first. Straight binary or offset binary coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ 0.4V indicates conversion time completed. V out ("1") ≥ +2.4V during reset and conversion periods. Loading: 4 TTL loads.
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	8 Bits (1 part in 256)
Linearity Error	± 1/2 LSB max.
Differential Nonlinearity	± 1/2 LSB max.
Temp. Coeff. of Gain	± 50ppm/°C max.
Temp. Coeff. of Zero, Unipolar	± 100μV/°C max.
Temp. Coeff. of Offset, Bipolar	± 35 ppm of FS/°C max.
Long Term Stability	± .05%/year
Power Supply Rejection	± .02% of FS/% supply, max.
Conversion Time	4.0 μsec. max., ADC-EH8B1 2.0 μsec. max., ADC-EH8B2

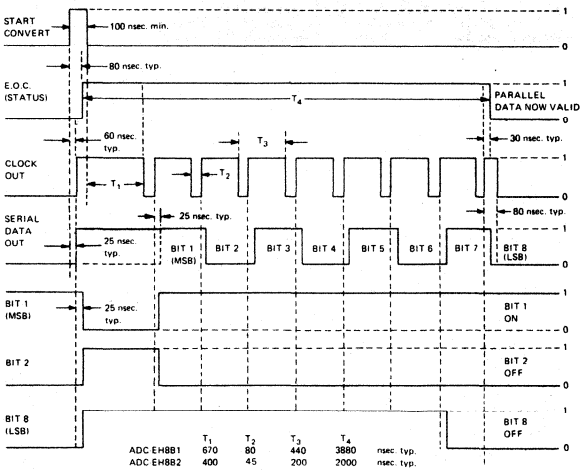
POWER REQUIREMENT

± 15VDC ±0.5V @ 25mA max.
+5VDC ± 0.25V @ 125mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	−55°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	2 x 2 x 0.375 inches (50,8 x 50,8 x 9,5 mm)
Case Material	Black diallyl phthalate per MIL-M-14
Pins	.020" round, gold plated, .250" lg. min.
Weight	2 oz. max. (57g.)

TIMING DIAGRAM FOR ADC-EH8B Output: 10101010



OUTPUT CODING

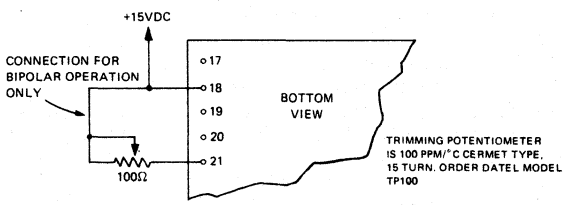
UNIPOLAR (0 TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS−1 LSB	+9.96V	1111 1111
+7/8 FS	+8.75V	1110 0000
+3/4 FS	+7.50V	1100 0000
+1/2 FS	+5.00V	1000 0000
+1/4 FS	+2.50V	0100 0000
+1 LSB	+0.04V	0000 0001
0	0.00V	0000 0000

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BIN	2'S COMPLEMENT
+FS−1 LSB	+4.96V	1111 1111	0111 1111
+3/4 FS	+3.75V	1110 0000	0110 0000
+1/2 FS	+2.50V	1100 0000	0100 0000
0	0.00V	1000 0000	0000 0000
−1/2 FS	−2.50V	0100 0000	1100 0000
−3/4 FS	−3.75V	0010 0000	1010 0000
−FS+1 LSB	−4.96V	0000 0001	1000 0001
−FS	−5.00V	0000 0000	1000 0000

ADC-EH8B CALIBRATION



1. UNIPOLAR – No adjustments are necessary and 100Ω trimming pot is not used. Full scale and zero are internally set to better than 1/2 LSB. Pin 21 is left open.
2. BIPOLAR – Connect pin 18 (+15VDC) to pin 21 through a 100Ω trimming potentiometer as shown. Connect a precision voltage source to pin 32 and set the input voltage to + 1/2 LSB or +0.020V. Adjust the trimming potentiometer so that the output code flickers equally between 1000 0000 and 1000 0001.

ORDERING INFORMATION

ADC-EH8B ——

CONVERSION TIME
1 = 4.0 μSEC. 2 = 2.0 μSEC.

PRICES (1-9)

ADC-EH8B1
ADC-EH8B2

MATING SOCKETS:
DILS-2 (2/MODULE)
TP100 TRIMMING POT.

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	−25°C to +85°C operation
−EXX−HS	−55°C to +85°C operation with hermetically sealed semiconductor components.

NOTE: ADC-EH8B1 & 2 replace former models ADC-EH1 & 2 and are improved models of these units respectively. The only difference from the previous models is the 3 additional output pins for serial output, clock output, and $\overline{MSB}$ output, and a change in input impedance from 5K ohms to 4.45K ohms. If the newly used pins (nos. 2, 4, and 13) cause a problem in an existing application, they should be clipped off.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

10 Bit, 2.0 and 4.0 μSec. Analog-to-Digital Converters ADC-EH10B

FEATURES

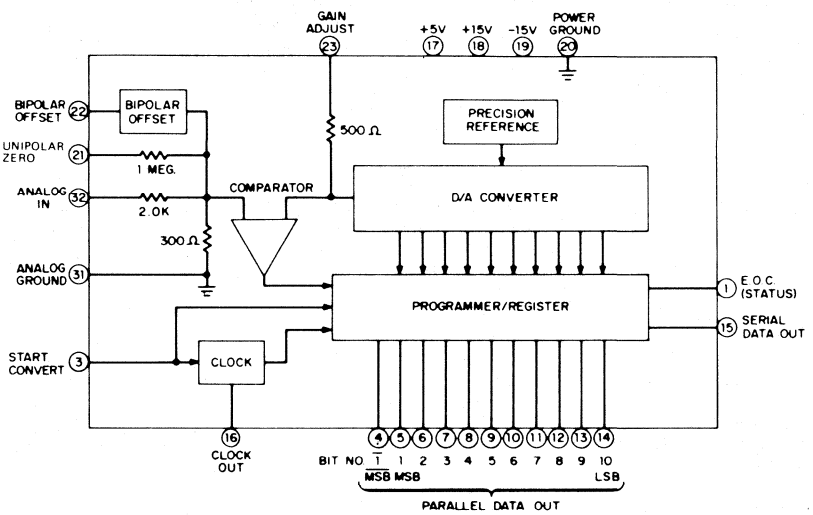
- **2.0 μsec. Conversion – ADC-EH10B2**
- **4.0 μsec. Conversion – ADC-EH10B1**
- **10 Bit Resolution**
- **Compact 3" x 2" x .375" Module**
- **±30ppm/°C max. Tempco**

GENERAL DESCRIPTION

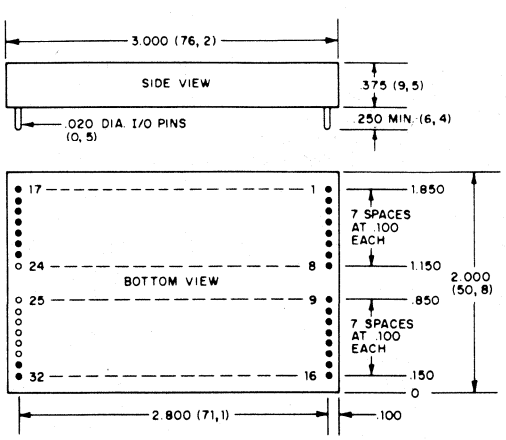
Model ADC-EH10B is a very fast 10 bit successive approximation type A/D converter in a compact low profile package. Low pricing makes this converter an ideal choice for many applications including fast scanning data acquisition systems, PCM systems, and fast pulse analysis. This converter is available in two versions based on conversion speed: ADC-EH10B1 with 4.0 μsec. (250kHz rate) and ADC-EH10B2 with 2.0 μsec. (500kHz rate).

High speed and moderate power consumption (1.7 watts) in a compact size (3" x 2" x .375") are made possible by use of an MSI integrated circuit successive approximation programmer/register used with 10 fast switching current sources driving a low impedance R-2R ladder network. A fast precision comparator and precision voltage reference circuit are also used.

Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. The converter has a maximum full scale temperature coefficient of ±30ppm/°C and is monotonic over the full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronizing serial data, MSB output for two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible. Power requirement is ±15VDC and +5VDC. The ADC-EH10B is also available in extended temperature range versions.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	NO CONNECTION
3	START CONVERT
4	BIT 1 OUT (MSB)
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT (LSB)
15	SERIAL DATA OUT
16	CLOCK OUT
17	+5VDC POWER IN
18	+15VDC POWER IN
19	-15VDC POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET.
23	GAIN ADJUST.
31	ANALOG GROUND
32	ANALOG IN

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SPECIFICATIONS, ADC-EH10B
(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	2.3K ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 50 nsec. min. Rise and fall times <500 nsec. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Output Data	10 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.4V indicates conversion completed. V out ("1") ≥ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

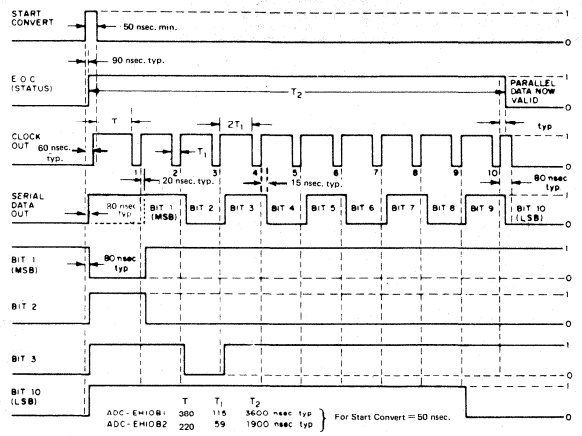
Resolution	10 Bits (1 part in 1024)
Nonlinearity	±1/2 LSB max.
Differential Nonlinearity	±1/2 LSB max.
Differential Nonlinearity T.C.	±10ppm/°C max.
Temp. Coeff. of Gain	±30ppm/°C max.
Temp. Coeff. of Zero, unipolar	±150 μV/°C max.
Temp. Coeff. of Offset, bipolar	±20ppm/°C max.
Power Supply Rejection	.01% FS/% supply, max.
Conversion Time	4.0 μsec. max., ADC-EH10B1 2.0 μsec. max., ADC-EH10B2

POWER REQUIREMENT	+15VDC ±0.5VDC @ 75mA max. -15VDC ±0.5VDC @ 20mA max. +5VDC ±0.25VDC @ 150mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	-25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	3 x 2 x .375 inches (76,2 x 30,8 x 9,5mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	.020" round, gold plated, .250" long min.
Weight	3 oz. max. (85g.)

TIMING DIAGRAM FOR ADC-EH10B Output: 1010101010



OUTPUT CODING

UNIPOLAR (0V TO +10V)

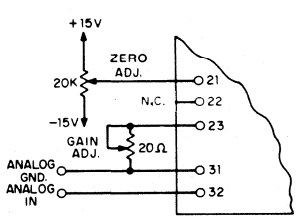
SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9902V	1111 1111 11
+7/8 FS	+8.7500V	1110 0000 00
+3/4 FS	+7.5000V	1100 0000 00
+1/2 FS	+5.0000V	1000 0000 00
+1/4 FS	+2.5000V	0100 0000 00
+ 1 LSB	+0.0098V	0000 0000 01
0	0.0000V	0000 0000 00

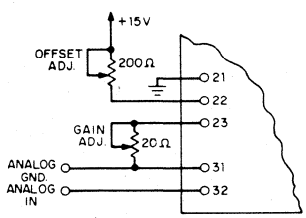
BIPOLAR (-5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS -1 LSB	+4.9902V	1111 1111 11	0111 1111 11
+3/4 FS	+3.7500V	1110 0000 00	0110 0000 00
+1/2 FS	+2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
-1/2 FS	-2.5000V	0100 0000 00	1100 0000 00
-3/4 FS	-3.7500V	0010 0000 00	1010 0000 00
-FS + 1 LSB	-4.9902V	0000 0000 01	1000 0000 01
-FS	-5.0000V	0000 0000 00	1000 0000 00

*Using $\overline{\text{MSB}}$ output for Bit 1

GAIN & OFFSET ADJUSTMENTS





UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 3 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero + ½ LSB (+4.9mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 00 and 0000 0000 01.
3. Adjust the output of the voltage reference to +FS − 1½ LSB (+9.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 10 and 1111 1111 11.

BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 3 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to 0.0000V. Adjust the offset trimming potentiometer so that the output code is 1000 0000 00.
3. Adjust the output of the voltage reference to +FS-1½ LSB (+4.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 10 and 1111 1111 11.

ORDERING INFORMATION

ADC-EH10B —

CONVERSION TIME
1 = 4.0 μsec.
2 = 2.0 μsec.

PRICES (1-9)
ADC-EH10B1
ADC-EH10B2

MATING SOCKETS:
DILS-2 (2/MODULE)
TRIMMING POTENTIOMETERS:
TP20, TP200, TP20K

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

-EX	-25°C to +85°C operation
-EXX-HS	-55°C to +85°C operation with hermetically sealed semiconductor components

NOTE: ADC-EH10B1 replaces former Datel model ADC-EH10B and is an improved version of the model. The only differences from the previous model is the change in input impedance from 10K ohms to 2.3K ohms, and the reduction in 5V supply current from 280mA to 150mA.

THE ADC-EH10B CONVERTERS ARE COVERED BY GSA CONTRACT

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

12 Bit, 4.0 and 8.0 μSec. Analog-to-Digital Converters ADC-EH12B1, B2

FEATURES

- 4.0 μsec. Conversion—ADC-EH12B2
- 8.0 μsec. Conversion—ADC-EH12B1
- 12 Bit Resolution
- 30PPM/°C Tempco
- Low Profile—0.4" High

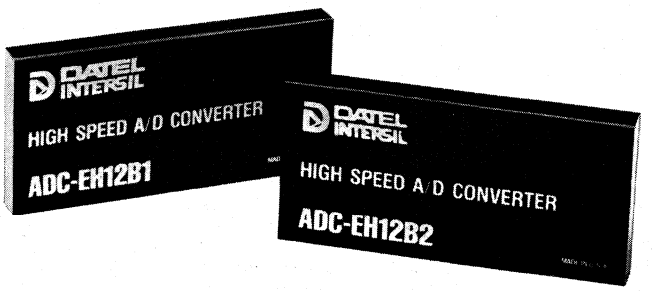
GENERAL DESCRIPTION

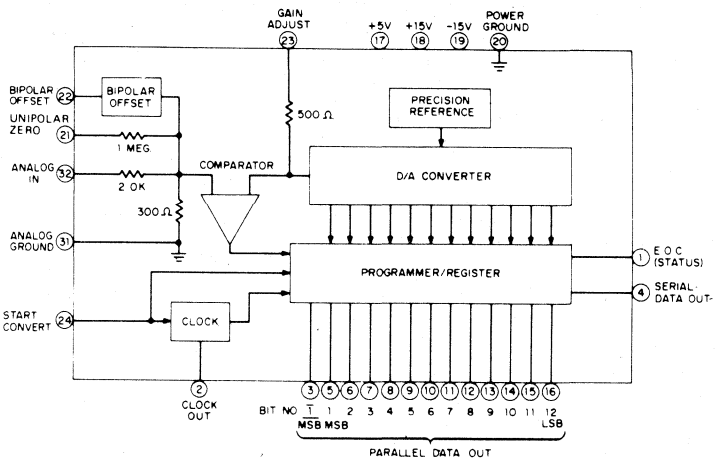
Model ADC-EH12B is a 4 microsecond, 12 bit successive approximation type A/D converter in a low profile 4 x 2 x 0.4 inch module. This high performance converter is priced at about half that of other competing models; in addition, it consumes only 2.0 watts of power, much less than competing devices. It is ideal for application in PCM systems, data acquisition systems, and other instrumentation and control systems requiring very fast data conversion rates up to 250,000 per second. The ADC-EH12B is also available in an even lower cost 8.0 μsec. version.

The ADC-EH12B design utilizes an MSI integrated circuit successive approximation programmer/register, 12 fast switching current sources, a low impedance R-2R resistor network, a precision voltage reference circuit, and a fast precision comparator to achieve its very fast conversion rate.

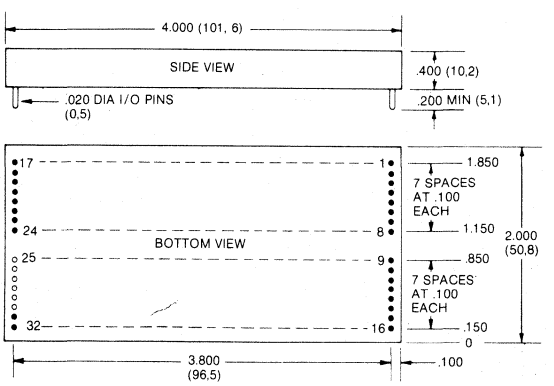
Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. Full scale temperature coefficient is 30ppm/°C maximum and the converter is monotonic over its full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronization with serial data, MSB output for use in two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible.

Power requirement is ±15VDC and +5VDC. Extended temperature range versions are also available.





MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	CLOCK OUT
3	BIT 1 OUT (MSB)
4	SERIAL DATA OUT
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT
15	BIT 11 OUT
16	BIT 12 OUT (LSB)
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST
24	START CONVERT IN
31	ANALOG GROUND
32	ANALOG IN

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-EH12B
(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	2.3K ohms ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <500 nsec. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Output Data	12 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.4V indicates conversion completed. V out ("1") ≥ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	12 Bits (1 part in 4096)
Nonlinearity	±1/2 LSB max.
Differential Nonlinearity	±1/2 LSB max.
Differential Nonlinearity T.C.	±3ppm/°C max.
Temp. Coeff. of Gain	±30ppm/°C max.
Temp. Coeff. of Zero, unipolar	±150 μV/°C max.
Temp. Coeff. of Offset, bipolar	±15ppm of F.S./°C max.
Power Supply Rejection	.01% FS/% supply, max.
Conversion Time	8.0 μsec. max., ADC-EH12B1 4.0 μsec. max., ADC-EH12B2

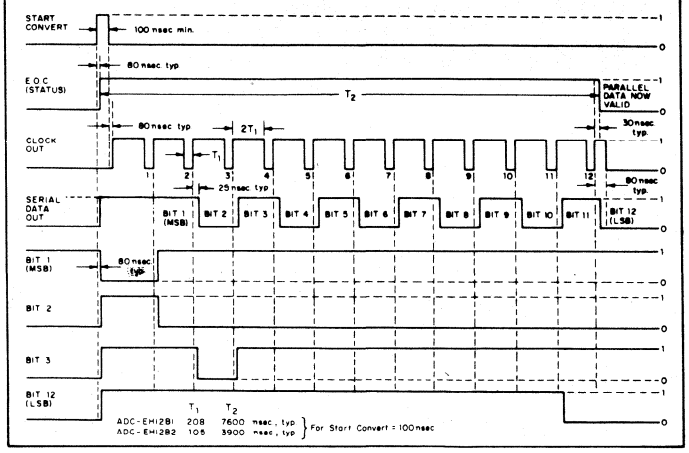
POWER REQUIREMENT

±15VDC ±0.5VDC @ 40mA max.
+5VDC ±0.25VDC @ 150mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	-25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	.020" round, gold plated, .200" long min.
Weight	4 oz. max. (114 g.)

TIMING DIAGRAM FOR ADC-EH12B Output: 101010101010



OUTPUT CODING

UNIPOLAR (0V TO +10V)

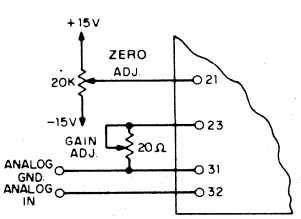
SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (–5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS - 1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS + 1 LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

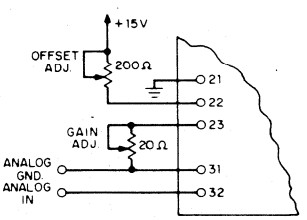
*Using $\overline{\text{MSB}}$ output for Bit 1

GAIN & OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero + 1/2 LSB (+1.2mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to + FS – 1 1/2 LSB (+9.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to 0.0000V. Adjust the offset trimming potentiometer so that the output code is 1000 0000 0000.
3. Adjust the output of the voltage reference to + FS – 1 1/2 LSB (+4.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

ORDERING INFORMATION

ADC-EH12B–

CONVERSION TIME
1= 8.0 μsec.
2= 4.0 μsec.

PRICES (1-9)

ADC-EH12B1 . . . .
ADC-EH12B2 . . . .

MATING SOCKETS:
DILS-2 (2/MODULE)
TRIMMING POTENTIOMETERS:
TP20, TP200, TP20K

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

–EX	-25°C to +85°C operation
–EXX–HS	-55°C to +85°C operation with hermetically sealed semiconductor components

THE ADC-EH12B CONVERTERS ARE COVERED BY GSA CONTRACT.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

Ultra-Fast, 12 Bit Analog-to-Digital Converter ADC-EH12B3

FEATURES

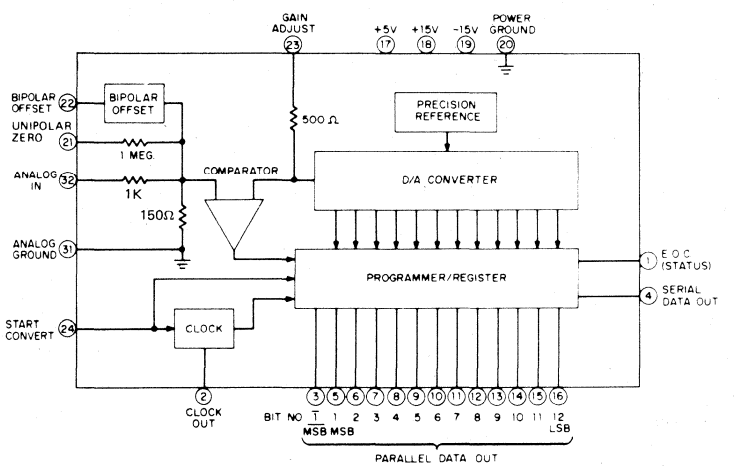
- 2.0 μsec. Conversion Time
- 12 Bit Resolution
- Low Power Consumption – 2.25W
- Low Profile Case – 0.4" High
- Economy Price

GENERAL DESCRIPTION

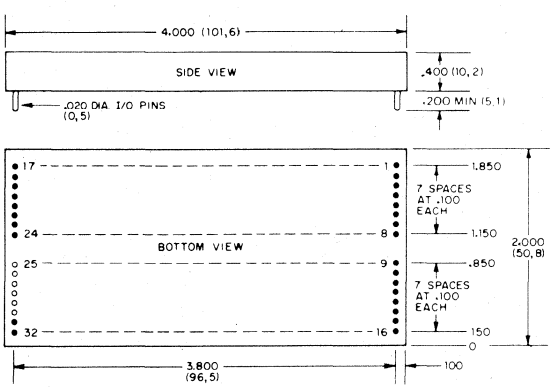
Model ADC-EH12B3 is a new, ultra fast, 12 bit successive approximation A/D converter with a 2.0 microsecond maximum conversion time. This converter utilizes 12 very fast switched current sources with a low impedance R-2R ladder network, a fast precision comparator, a precision zener reference source, and an MSI integrated circuit successive approximation register to achieve its state of the art performance. It is encapsulated in a low profile 2 x 4 x 0.4 inch module and consumes only 2.25 watts of power. The ADC-EH12B3 opens up a broad range of fast data conversion applications where conversion rates up to 500,000 per second are required.

Input voltage ranges are 0 to +10V unipolar or ±5V bipolar by external pin connection; input impedance is 1.15K ohms. The parallel output is in straight binary, offset binary, or two's complement coding. Serial output data is also brought out in the form of an NRZ format MSB first pulse train. Full scale temperature coefficient is ±30ppm/°C maximum and zero temperature coefficient is ±150μV/°C maximum. Due to its low differential linearity temperature coefficient there are no missing codes over the 0°C to 70°C operating temperature range. Provision is made for precise alignment in a given application.

Other DTL/TTL compatible outputs include clock, $\overline{MSB}$ output (for two's complement coding), and end of conversion (status) output. Power supply requirement is ±15VDC and +5VDC.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	CLOCK OUT
3	BIT 1 OUT (MSB)
4	SERIAL DATA OUT
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT
15	BIT 11 OUT
16	BIT 12 OUT (LSB)
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST
24	START CONVERT IN
31	ANALOG GROUND
32	ANALOG IN

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-EH12B3
(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	1.15K ohms ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <500 nsec. Logic "1" resets converter Logic "0" initiates conversion **Loading: 3 TTL loads**

OUTPUTS

Parallel Output Data	12 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.4V indicates conversion completed. V out ("1") ≥ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	12 Bits (1 part in 4096)
Nonlinearity	±1/2 LSB max.
Differential Nonlinearity	±1/2 LSB max.
Differential Nonlinearity T.C.	±3ppm/°C max.
Temp. Coeff. of Gain	±30ppm/°C max.
Temp. Coeff. of Zero, unipolar	±150μV/°C max.
Temp. Coeff. of Offset, bipolar	±15ppm of F.S./°C max.
Power Supply Rejection	.01% FS/% supply, max.
Conversion Time	2.0 μsec. maximum

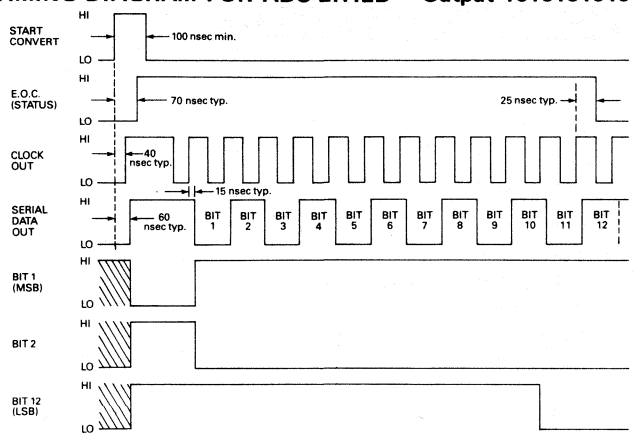
POWER REQUIREMENT

+15VDC ±0.5V @ 80mA max.
−15VDC ±0.5V @ 20mA max.
+5VDC ±0.25V @ 150mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	-25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	.020" round, gold plated, .200" long min.
Weight	4 oz. max. (114 g.)

TIMING DIAGRAM FOR ADC-EH12B Output 101010101010



OUTPUT CODING

UNIPOLAR (0V TO +10V)

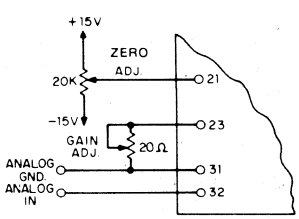
SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS - 1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS + 1 LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

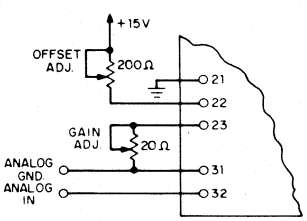
*Using $\overline{MSB}$ output for Bit 1

GAIN & OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero + 1/2 LSB (+1.2mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to + FS − 1 1/2 LSB (+9.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to 0.0000V. Adjust the offset trimming potentiometer so that the output code is 1000 0000 0000.
3. Adjust the output of the voltage reference to + FS − 1 1/2 LSB (+4.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

ORDERING INFORMATION

PRICES (1-9)

ADC-EH12B3 .....

MATING SOCKETS:
DILS-2 (2/MODULE)
TRIMMING POTENTIOMETERS:
TP20, TP200, TP20K

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	-25°C to +85°C operation
−EXX−HS	-55°C to +85°C operation with hermetically sealed semiconductor components

THE ADC-EH12B3 CONVERTER IS COVERED UNDER GSA CONTRACT.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

Monolithic Integrating Analog-to-Digital Converters ADC-EK Series

FEATURES

- **Monolithic CMOS**
- **Binary or BCD Models**
- **20mW Power Consumption**
- **To 12 Bit Accuracy**
- **No Missing Codes**
- **Low Cost**

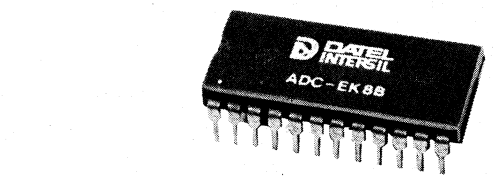
GENERAL DESCRIPTION

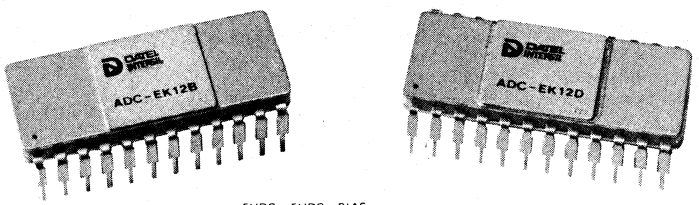
The ADC-EK series are low power, integrating A/D converters fabricated on a single monolithic chip using CMOS technology. The circuit employs a charge balancing integrator, current switch, comparator, clock counter, data counter, and control logic circuitry to implement conversion. The charge balancing integration technique gives high linearity and noise immunity along with inherent monotonicity resulting in no missing codes. Output data appears in parallel form on latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The ADC-EK series consists of 5 different models with 8, 10, and 12 bit binary coding and 3½ digit BCD coding.

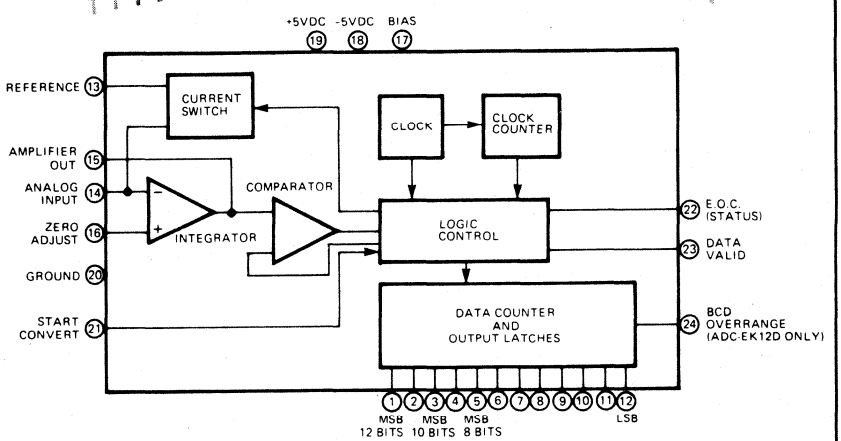
Conversion time is 1.8 to 24 milliseconds maximum depending on model. Nonlinearity is ±½ LBS max. while differential nonlinearity is ±¼ LSB typical. Other specifications include gain tempco of ±25ppm/°C typ. and zero drift of ±50μ V/°C max. An external reference, integrating capacitor, and several other components are required for operation. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10μA full scale. Standard operating mode is unipolar but bipolar operation is accomplished using an external op amp to provide an offset current from the reference.

Power requirement is ±5VDC at 2mA, giving a power consumption of only 20 milliwatts. The units are packaged in 24 pin ceramic or plastic DIP's.

CAUTION: The ADC-EK Series are CMOS devices and should be handled carefully to prevent static charge pick-up which might damage the devices. The devices should be kept in the shipping containers until ready for installation.

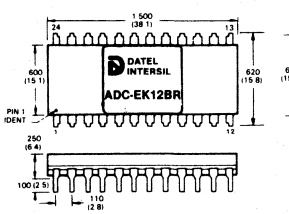




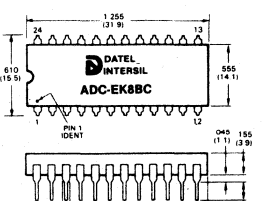


MECHANICAL DIMENSIONS INCHES (MM)

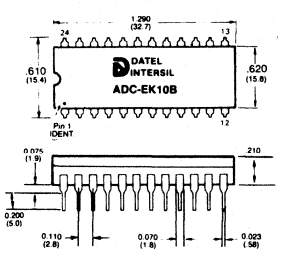
CERAMIC PACKAGE



PLASTIC PACKAGE



CERDIP



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-EK SERIES
(Typical at 25°C, ±5V Supplies, R_{BIAS} = 100K, unless otherwise noted)

	ADC-EK8B/10B/12B	ADC-EK12DC/DR/DM
MAXIMUM RATINGS		
I_{IN}	±10 mA	
I_{REF}	±10 mA	
Digital Input Voltage	−0.3V to V_{DD} + 0.3V	
$V_{DD} - V_{SS}$	18V	
Package Dissipation	500 mW	
ANALOG INPUTS		
Type Analog Input	Single Ended	
Full Scale Input Current	+10 μA	
Reference Current	−20 μA	
DIGITAL INPUTS		
Logical "1" V_{IN}	3.5V min.	
Logical "0" V_{IN}	1.5V max.	
Start Convert Pulse	>3.5V for 500 nsec. min.	
OUTPUTS		
Parallel Output Data	8, 10, 12 Lines	12 Lines and Overrange
Logic "1" Output Voltage	+4.5V min. at −10 μA, +2.4V min. at −360 μA[2]	
Logic "0" Output Voltage	+0.4 max. at −360 μA[2]	
E.O.C. (Status)	HI During Conversion, LO When Completed	
DATA VALID	HI When Data Valid, LO When Data Changing	
PERFORMANCE		
Resolution	8, 10, 12 Bits	3½ Digits
Coding	Straight Binary	BCD
Nonlinearity	½ LSB, max.	0.025% max.
Differential Nonlinearity	¼ LSB, typ. ½ LSB max.	0.025% max.
Diff. Nonlinearity Tempco	±2.5 ppm/°C typ., ±5 ppm/°C max.	
No Missing Codes	Over Operating Temperature Range	
Initial Gain Error, Adj. to Zero	+5, −3% max.[1]	
Gain Temperature Coefficient	±25 ppm/°C typ., ±75 ppm/°C max.[1]	
Initial Zero Error, Adj. to Zero	±50 mV max.	
Zero Drift Tempco	±50 μV/°C max.[1]	
Conversion Time, max.	1.8 msec. (8 Bits) 6 msec. (10 Bits) 24 msec. (12 Bits)	12 msec (3½ Digits)
Power Supply Sensitivity	±0.05% of Full Scale Gain[3]	
POWER REQUIREMENT		
Voltage, Rated Performance	±5 VDC	
Voltage Range, Operating	±3.5 VDC to ±7 VDC	
Supply Quiescent Current		
ADC-EK8B, EK12DC	± 5.0 mA	
ADC-EK10B, EK12B, EK12DR	± 2.5 mA max.	
ADC-EK12DM	± 3.5 mA max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range	See Ordering Information	
Storage Temp. Range	−65°C to +150°C	
Package	24 Pin DIP	

NOTES: 1. For the ADC-EK12DM Only. Initial Gain Error is ±5%, Gain Tempco is ±40 ppm/°C typ., ±80 ppm/°C max. and Zero Drift Tempco is 80 μV/°C.
2. ADC-EK12DM outputs can sink and source 500 μA.
3. Supply Sensitivity given for $V_{DD} = V_{SS} = 5V \pm 1V$.

TECHNICAL NOTES

1. The ADC-EK series are CMOS devices and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive form or shorting all pins together with aluminum foil. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open circuit the zero adjust, reference, or start convert pins while power is on. It should also be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference, and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and +5% −3% tolerance on the converter scale factor, the actual resistor value can vary by almost ±10%. R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and R_T be 1% of R_{OFF} (nominal). They should both be 100ppm/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is to set the R_G and R_T to center of range and then choose 1% metal film resistor which gives the nearest fit at the full scale point 1111... 111 for R_{IN} and one that gives the nearest fit to zero scale point 1000... 000 for R_T.
3. To choose any intermediate scale values for R_{IN} and R_T or values of R_{REF} for other reference voltages, use the following formulas:

$$R_{IN}\,(\text{nom.}) = \frac{FSR}{10\mu A}$$

FSR is full scale range or total input voltage span for the converter.

$$R_{OFF}\,(\text{nom.}) = \frac{V_{REF}}{5\mu A}$$

$$R_{REF}\,(\text{nom.}) = \frac{V_{REF}}{20\mu A}$$

It is recommended that large full-scale voltage ranges be chosen such

ORDERING INFORMATION

MODEL NO.	OPER. TEMP RANGE	PACKAGE	PRICE (1-24)
BINARY			
ADC-EK8B	0°C to +70°C	Plastic	
ADC-EK10B	−25°C to +85°C	Cerdip	
ADC-EK12B	−25°C to +85°C	Ceramic	
BCD			
ADC-EK12DC	0°C to +70°C	Plastic	
ADC-EK12DR	−25°C to +85°C	Ceramic	
ADC-EK12DM	−55°C to +125°C	Ceramic	

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

TECHNICAL NOTES (Cont'd.)

as 0 to +10V, 0 to +5V etc. in order to keep the error due to input offset voltage drift to a minimum.

4. The temperature stability of the ADC-EK converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF}, and V_{REF}. Since the converter is typically ±20ppm/°C it is recommended that a **10ppm/°C reference be used along with 10ppm/°C metal film resistors for** R_{IN}, R_{REF}, and R_{OFF} for best performance over temperature. On a statistical basis this would give about 28ppm/°C stability for the complete converter.
5. Other passive components used with the converter may have tolerances as indicated here: R_C is a ±10% carbon comp. resistor; C_C is a ±20% ceramic capacitor; C_{INT} is a ±10% glass or ceramic capacitor; R_{BIAS} is a ±10% carbon comp. resistor; and the two zero adjust resistors are ±10% carbon composition type. It is recommended that two 0.1μF bypass capacitors be used right at the power supply pins. C_{INT} should be connected as close as possible to pins 14 and 15 away from any noisy lines.
6. The start convert pulse initiates conversion on the LO to HI transition after which the conversion cycle cannot be interrupted and must run to completion.
7. Logic signals should not be routed under these devices or near the input reference, or zero adjust pins.
8. The unused data output pins on the 8 and 10 bit models should not be used for external connection points since they have internal connections to the converter.
9. All digital outputs will drive 2 low power TTL loads or 1 low power Schottky TTL load. They should not be overloaded as this will affect the performance of the converter.
10. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be ±.04% for 8 bit models, ±.01% for 10 bit models and ±.0025% for 12 bit models.

INPUT/OUTPUT CONNECTIONS

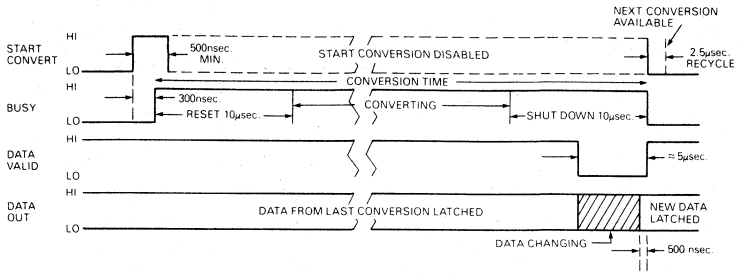
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB-12 BITS)	13	REFERENCE
2	BIT 2 OUT	14	ANALOG INPUT
3	BIT 3 OUT (MSB-10 BITS)	15	AMPLIFIER OUT
4	BIT 4 OUT	16	ZERO ADJUST
5	BIT 5 OUT (MSB-8 BITS)	17	BIAS
6	BIT 6 OUT	18	-5V POWER
7	BIT 7 OUT	19	+5V POWER
8	BIT 8 OUT	20	GROUND
9	BIT 9 OUT	21	START CONVERT
10	BIT 10 OUT	22	E O C (STATUS)
11	BIT 11 OUT	23	DATA VALID
12	BIT 12 OUT (LSB-ALL)	24	BCD OVERRANGE*

*NO CONNECTION FOR OTHER MODELS

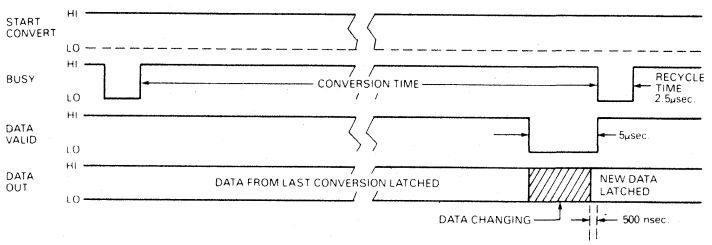
NOTE:
FOR 8 AND 10 BIT MODELS DO NOT CONNECT TO UNUSED DATA OUTPUT TERMINALS SINCE THEY HAVE INTERNAL CONNECTIONS

TIMING DIAGRAMS

CLOCKED OPERATION



FREE RUNNING OPERATION



CODING TABLES

STRAIGHT BINARY

	8 BIT		10 BIT		12 BIT	
SCALE	0 TO +10V	CODE	0 TO +10V	CODE	0 TO +10V	CODE
FS-1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

	8 BIT		10 BIT		12 BIT	
SCALE	±5V	CODE	±5V	CODE	±5V	CODE
+FS-1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
-FS + 1LSB	-4.96	0000 0001	-4.990	00 0000 0001	-4.9976	0000 0000 0001
-FS	-5.00	0000 0000	-5.000	00 0000 0000	-5.0000	0000 0000 0000

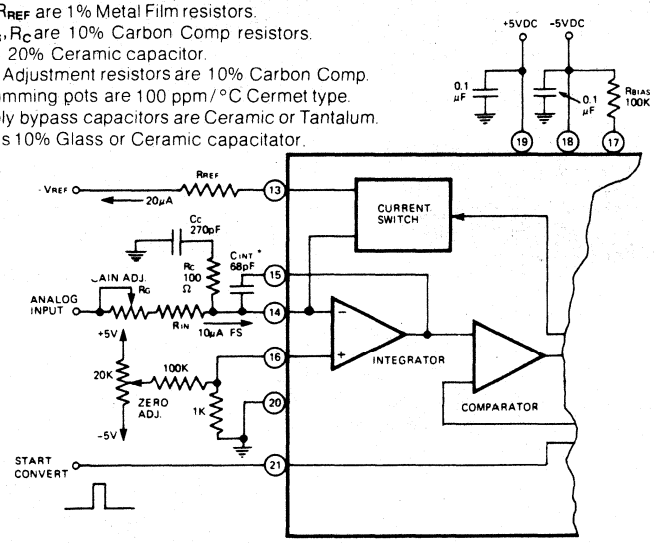
BCD

	FULL SCALE RANGE			
SCALE	0 TO +2V	0 TO +10V	0 TO +20V	CODE
FS-1 LSB	+1.999V	+9.995V	+19.990V	1 1001 1001 1001
½ FS	+1.000	+5.000	+10.000	1 0000 0000 0000
1 LSB	+0.001	+0.005	+ 0.010	0 0000 0000 0001
0	0.000	0.000	0.000	0 0000 0000 0000

CONNECTIONS AND CALIBRATION

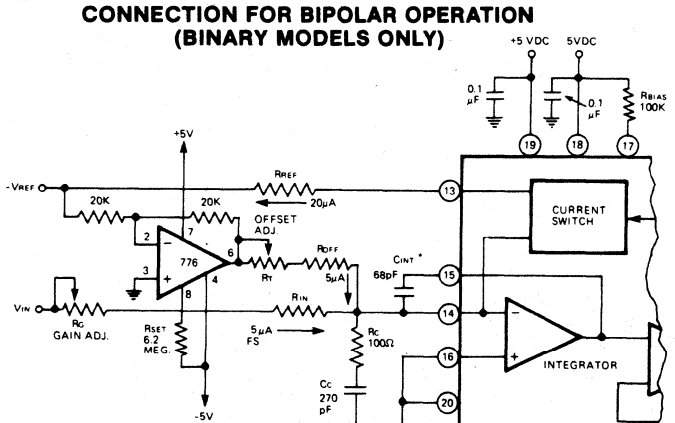
CONNECTION FOR UNIPOLAR OPERATION

R_{IN}, R_{REF} are 1% Metal Film resistors.
R_{BIAS}, R_C are 10% Carbon Comp resistors.
C_C is 20% Ceramic capacitor.
Zero Adjustment resistors are 10% Carbon Comp.
All trimming pots are 100 ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.
C_{INT} is 10% Glass or Ceramic capacitator.



*33pF for ADC-EK8B

CONNECTION FOR BIPOLAR OPERATION (BINARY MODELS ONLY)

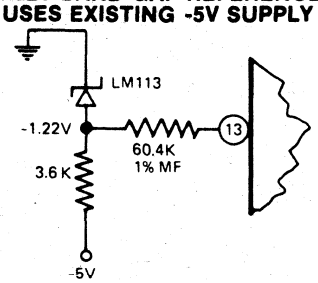


R_{IN}, R_{REF}, R_{OFF} and the two 20K resistors are 1% Metal Film types.
All other resistors are 10% Carbon Comp. type.
C_C is 20% Ceramic capacitor.
C_{INT} is 10% Glass or Ceramic capacitor.
All trimming pots are 100ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.

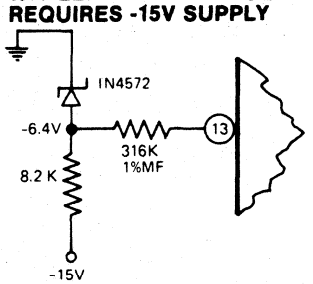
*33pF for ADC-EK8B

REFERENCE CIRCUITS

1.22V BAND GAP REFERENCE USES EXISTING -5V SUPPLY



6.4V ZENER REFERENCE REQUIRES -15V SUPPLY



RESISTOR TABLES

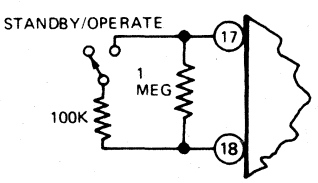
UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOM.)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG.
0 TO +20V	±10V	2 MEG.

V_{REF}	R_{REF} (NOM.)	R_{OFF} (NOM.)
-1.22V	61K	244K
-2.5V	125K	500K
-6.4V	320K	1.28 MEG.

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic HI to the start convert input (pin 21) to give free-running operation.
2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or -FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000....000 and 000....001.
3. **Gain Adjustment.** Set the output of the reference source to +FS −1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111....110 and 111....111.
   For BCD coding the output code should flicker between 1001 1001 1000 and 1001 1001 1001.

REDUCTION OF STAND-BY POWER



This reduces power consumption to about 200μA during Standby

Monolithic A/D Converters with Three-State Outputs ADC-ET Series

FEATURES

- **Monolithic CMOS**
- **Three State Outputs**
- **To 12 Bit Accuracy**
- **No Missing Codes**
- **Low Cost**
- **Microprocessor Compatible**

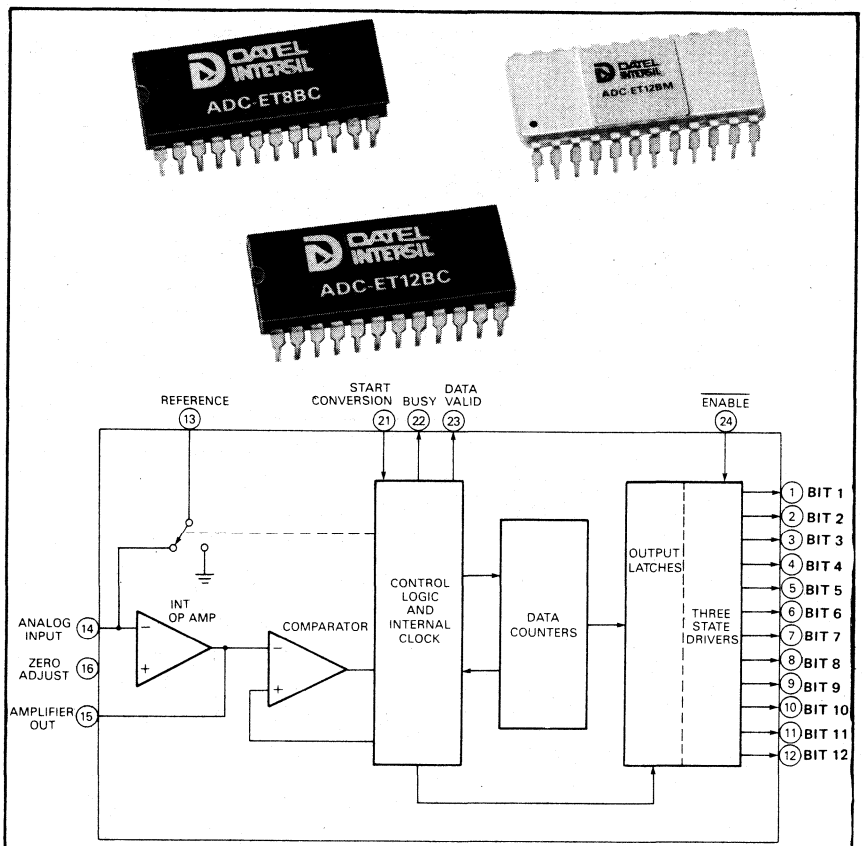
GENERAL DESCRIPTION

The ADC-ET series devices are low cost integrating A/D converters optimized for high accuracy, linearity and noise immunity. They operate at low power consumption, with sufficient speed to handle most industrial and instrumentation requirements. Discretely controllable three state outputs allow bus organized output connections making these units ideal for microprocessor interfacing.

Fabricated with monolithic CMOS techniques, each device is housed in a single 24 pin dual in-line package. The converter consists of an integrating operational amplifier, comparator, current switch, internal clock, two counters, latching output buffers and control logic circuitry. Operation of the circuit requires only a few external passive components and connection to external reference and power supplies. Conversion is accomplished by an incremental charge balancing technique which assures high linearity and noise immunity, along with inherent monotonicity resulting in no missing codes. At the completion of a conversion, the binary coded result appears in parallel form on discretely controlled latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The controllable outputs may be switched to a high impedance or off state by holding the $\overline{\text{ENABLE}}$ high.

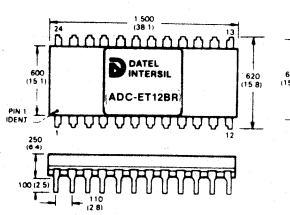
Conversion times are 1.8, 6 and 24 msec. for the 8, 10 and 12 bit units respectively. Other typical specifications include linearity to ¼ LSB and a gain tempco of 25 ppm/°C. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10 μA full scale. Standard operating mode is unipolar but bipolar operation can be implemented by using an external op amp to provide an offset current from the reference. Power requirement is ±5 VDC at 2 mA which, for intermittent duty applications, may be reduced to only 200 μA during standby periods without affecting data in the output latches.

CAUTION: These are CMOS devices and may be damaged by static discharge.

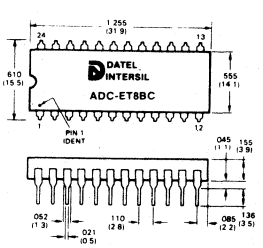


MECHANICAL DIMENSIONS INCHES (MM)

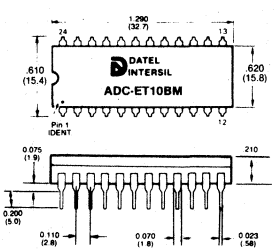
CERAMIC PACKAGE



PLASTIC PACKAGE



CERDIP



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-ET SERIES
(Typical at 25 C, 5V Supplies, R_{BIAS} 100K, unless otherwise noted)

MAXIMUM RATINGS

I_{IN}	±10 mA
I_{REF}	±10 mA
Digital Input Voltage	−0.3V to V_{DD} +0.3V
V_{DD}-V_{SS}	18V
Package Dissipation	500 mW

ANALOG INPUTS

Type Analog Input	Single Ended
Input Current Range	0 to +10 μA
Reference Current	−20 μA

DIGITAL INPUTS

Logical "1" V_{IN}	3.5V min.
Logical "0" V_{IN}	1.5V max.
Start Convert Pulse Width	500 nsec. min.
ENABLE Propagation Delay	500 nsec.

OUTPUTS

Output Off State Current	0.1 μA typ, ±10 μA max.
Logic "1" Output Voltage	+4.5V min at −10 μA
	+2.4V min at −360 μA[4]
Logic "0" Output Voltage	+0.4V max at 360 μA[4]
Data Valid Output	Hi for Data Valid, Lo When Loading
Busy Output	Hi During Conversion

PERFORMANCE

Resolution	8, 10, 12 Bits
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary
Conversion Times	
8 Bits	1.8 msec. max
10 Bits	6 msec. max.
12 Bits	24 msec. max.
Nonlinearity	±1/4 LSB typ., ±1/2 LSB Max.[1]
Differential Nonlinearity	±1/4 LSB typ., ±1/2 LSB max.
Diff. Nonlinearity Tempco	±2.5 ppm/°C
No Missing Codes	Over Operating Temp. Range
Initial Gain Error, (Adj. to Zero)	±5% max.
Gain Temperature Coefficient	±25 ppm/°C typ, ±75 ppm/°C max.[2]
Initial Zero Error (Adj. to Zero)	±50 mV max.
Zero Drift Tempco	±50 μV/°C max.[2]
Power Supply Sensitivity	±0.05%/% max.[3]

POWER REQUIREMENT

Voltage, Rated Performance	±5 VDC
Voltage Range, Operating	±3.5 VDC to ±7 VDC
Supply Quiescent Current	
C Suffix	±5.0 mA max.
R Suffix	±2.5 mA max.
M Suffix	±3.5 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	
C Suffix	0°C to +70°C
R Suffix	−25°C to +85°C
M Suffix	−55°C to +125°C
Package	
C Suffix	24 Pin Plastic DIP
R & M Suffix	24 Pin Ceramic DIP

NOTES:
1. Nonlinearity for model ADC-ET12BC only is typically ±1/4 LSB, ±1-1/2 LSB max.
2. For M suffix units only gain tempco is typically 40 ppm/°C, 80 ppm/°C max. and zero drift tempco is ±80 μV/°C.
3. V_{DD} ±1V, V_{SS} ±1V
4. M suffix logic outputs can sink and source 500 μA.

TECHNICAL NOTES

1. The ADC-ET series are CMOS devices and must be properly handled to prevent damage due to static discharge. Proper anti-static precautions should be taken, including storage and transport in anti-static containers or conductive foam, and grounding of work stations, handling equipment and personnel. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open circuit the zero adjust, reference or start convert pins while the power is on. It should be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and the +5%, −3% tolerance of the converter scale factor, the actual resistor value can vary by almost ±10%. R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and that R_T be 1% of R_{OFF} (nominal). They should both be 100 PPM/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is to set R_G and R_T to the center of their ranges and choose a 1% metal film resistor which gives the closest fit at the full scale point 1111....111 for R_{IN} and one that gives the closest fit to the zero scale point 0000...000 for R_T.
3. To choose any intermediate scale values for R_{IN} and R_T or values of R_{REF} for other reference voltages, use the following formulas:

$$R_{IN}\ (NOM.) = \frac{FSR}{10\mu A}$$

FSR is full scale range or total input voltage span for the converter.

$$R_{OFF}\ (NOM.) = \frac{V_{REF}}{5\mu A} \qquad R_{REF}\ (NOM.) = \frac{V_{REF}}{20\mu A}$$

It is recommended that large full scale voltage ranges be chosen, such as 0 to +10V, 0 to +5V etc., in order to keep the error due to input offset voltage drift to a minimum.
4. The temperature stability of the ADC-ET converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF} and V_{REF}. Since the converter is typically ±25ppm/°C it is recommended that a 10ppm/°C reference be used along with 10ppm/°C metal film resistors for R_{IN}, R_{REF} and R_{OFF} for best performance over temperature.
5. Passive components used with the converter may have tolerances as indicated here: C_c is a ±20% ceramic capacitor; C_{INT} is a ±10% glass or ceramic capacitor; R_{c1}, R_{BIAS} and the two zero adjust resistors are ±10% carbon composition type.
6. It is recommended that two 0.1 μF bypass capacitors be used at the power supply pins as shown in the connection diagram. C_{INT} should be connected as close as possible to pins 14 and 15 and as far as possible from any noisy lines.
7. Logic signals should not be routed under these devices or near the input, reference or zero adjust pins.
8. All digital outputs will drive two low power TTL loads or one low power Schottky TTL load. The outputs should not be overloaded as this will affect the performance of the converter.
9. It should be noted that there is a propagation delay of approximately 500 nsec. between the time ENABLE changes state and the time that the outputs change state.
10. For intermittent conversion applications the ADC-ET can be configured to use only 200μA during standby. In this mode the op amp and internal clock are shut down but data at the output latches remains available. See application diagram.
11. Two's complement coding can be implemented by inverting the MSB signal.
12. I_{IN} and I_{REF}, pins 14 and 13 respectively, connect to the summing junction of an operational amplifier which requires a current input. Voltage sources cannot be attached directly to them, but must be buffered by external resistors. Refer to Test Circuit Diagrams. Analog input can be any positive voltage when applied through the proper scaling resistor.
13. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be ±.04% for 8 bit models, ±.01% for 10 bit models and ±.0025% for 12 bit models.

DESCRIPTION OF OPERATION

When the START CONVERT input is strobed with a positive pulse of at least 500 nsec. duration, the busy line latches high and a start up cycle of approximately 10 μsec. begins, during which the integrating capacitor is discharged and both counters are reset. Conversion begins at the end of an internal reset pulse.

During conversion, the sum of a continuous current, I_{IN} and pulses of an inversely signed reference current I_{REF}, is integrated. I_{IN} is proportional to the analog input voltage and I_{REF} is proportional to the reference voltage. A pulse of I_{REF} is applied as required to maintain the summing input of the integrating op amp near zero. The total number of pulses of I_{REF} required to maintain the summing input near zero is counted and the binary coded result is latched into the outputs at the end of conversion.

The end of conversion is signaled by a pulse generated by the clock counter or by the data counter when an overflow condition occurs; this pulse disables further inputs into both counters and begins a 10 μsec. shutdown cycle. During the shutdown cycle, Data Valid goes low for 5 μsec., while the result of the latest conversion is being transferred to the outputs. Until transfer is complete, the data at the outputs is not valid. At the end of the shutdown cycle, Data Valid goes high indicating that the outputs are latched with the result of the last conversion, and the Busy Output goes low indicating the completion of the conversion cycle and the availability of the converter for the next conversion.

When the converter is employed in a free-running mode, the START CONVERT input is held high (simply connect pin 21 to pin 19), the Busy Output will go low for approximately 2.5 μsec. to mark the completion and initiation of consecutive conversion cycles. It should be noted that once conversion is initiated, the cycle cannot be interrupted; the START CONVERT pin is disabled when the Busy Output is high, and thus its logic state has no effect until completion of the conversion cycle. After the completion of a conversion, the output data remains valid for as long as power is applied to the circuit, or until Data Valid goes low at the end of a conversion.

RESISTOR TABLES

UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOM.)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG
0 TO +20V	±10V	2 MEG

V_{REF}	R_{REF} (NOM.)	R_{OFF} (NOM.)
-1.22V	61K	244K
-2.5V	125K	500K
-6.4V	320K	1.28 MEG.

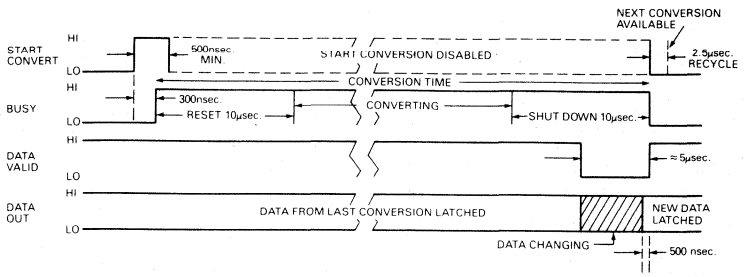
INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB-12 BITS)	13	REFERENCE
2	BIT 2	14	ANALOG INPUT
3	BIT 3 (MSB-10 BITS)	14	AMPLIFIER OUT
4	BIT 4	16	ZERO ADJUST
5	BIT 5 (MSB-8 BITS)	17	BIAS
6	BIT 6	18	-5V POWER
7	BIT 7	19	+5V POWER
8	BIT 8	20	GROUND
9	BIT 9	21	START CONVERT
10	BIT 10	22	BUSY OUTPUT
11	BIT 11	23	DATA VALID
12	BIT 12 (LSB-ALL)	24	$\overline{\text{ENABLE}}$

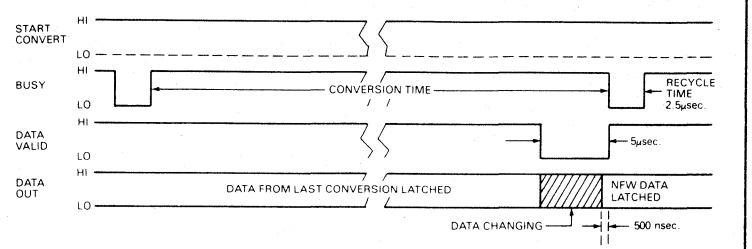
NOTE:
Do not connect unused data output pins on 8 and 10 bit models, they are internally connected to the converter.

TIMING DIAGRAMS

CLOCKED OPERATION



FREE RUNNING OPERATION



CODING TABLES

STRAIGHT BINARY

SCALE	8 BIT		10 BIT		12 BIT	
	0 TO +10V	CODE	0 TO +10V	CODE	0 TO +10V	CODE
FS-1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

SCALE	8 BIT		10 BIT		12 BIT	
	±5V	CODE	±5V	CODE	±5V	CODE
+FS-1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
-FS + 1LSB	-4.96	0000 0001	-4.990	00 0000 0001	-4.9976	0000 0000 0001
-FS	-5.00	0000 0000	-5.000	00 0000 0000	-5.0000	0000 0000 0000

ORDERING INFORMATION

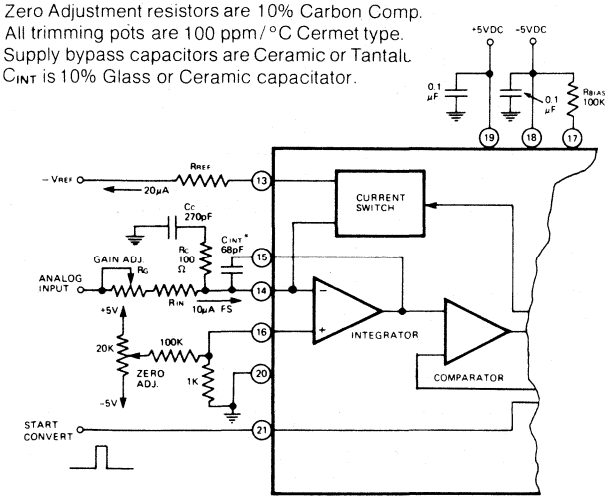
MODEL	OPERATING TEMP. RANGE	PACKAGE	PRICE (1-24)
ADC-ET8BC	0°C to +70°C	Plastic	
ADC-ET8BM	-55°C to +125°C	Cerdip	
ADC-ET10BC	0°C to +70°C	Plastic	
ADC-ET10BM	-55°C to +125°C	Cerdip	
ADC-ET12BC	0°C to +70°C	Plastic	
ADC-ET12BR	-25°C to +85°C	Ceramic	
ADC-ET12BM	-55°C to +125°C	Ceramic	

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

CONNECTIONS AND CALIBRATION

CONNECTION FOR UNIPOLAR OPERATION

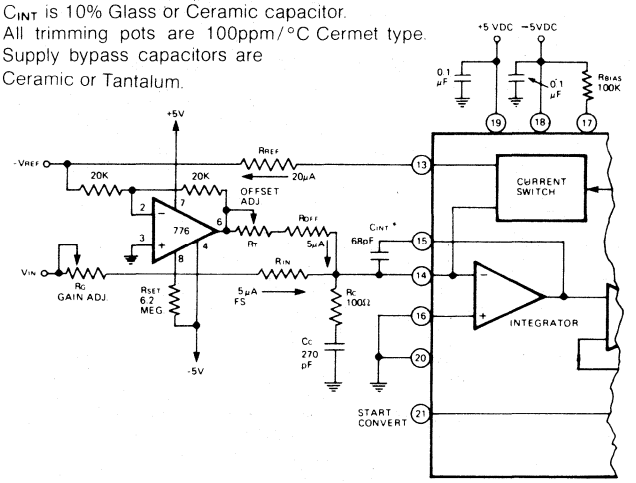
R_{IN}, R_{REF} are 1% Metal Film resistors.
R_{BIAS}, R_C are 10% Carbon Comp resistors.
C_C is 20% Ceramic capacitor.
Zero Adjustment resistors are 10% Carbon Comp.
All trimming pots are 100 ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.
C_{INT} is 10% Glass or Ceramic capacitator.



*33pF for ADC-ET8BC

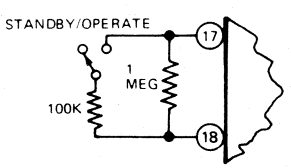
CONNECTION FOR BIPOLAR OPERATION

R_{IN}, R_{REF}, R_{OFF} and the two 20K resistors are 1% Metal Film types.
All other resistors are 10% Carbon Comp. type.
C_C is 20% Ceramic capacitor.
C_{INT} is 10% Glass or Ceramic capacitor.
All trimming pots are 100ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.



*33pF for ADC-ET8BC

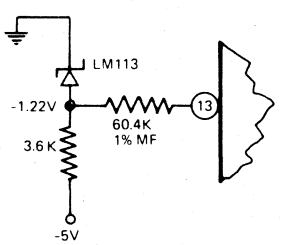
REDUCTION OF STAND-BY POWER



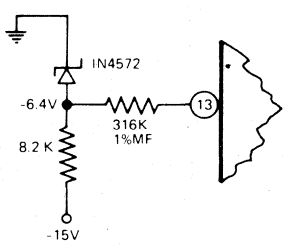
This reduces power consumption to about 200µA during Standby

REFERENCE CIRCUITS

1.22V BAND GAP REFERENCE USES EXISTING -5V SUPPLY



6.4V ZENER REFERENCE REQUIRES -15V SUPPLY



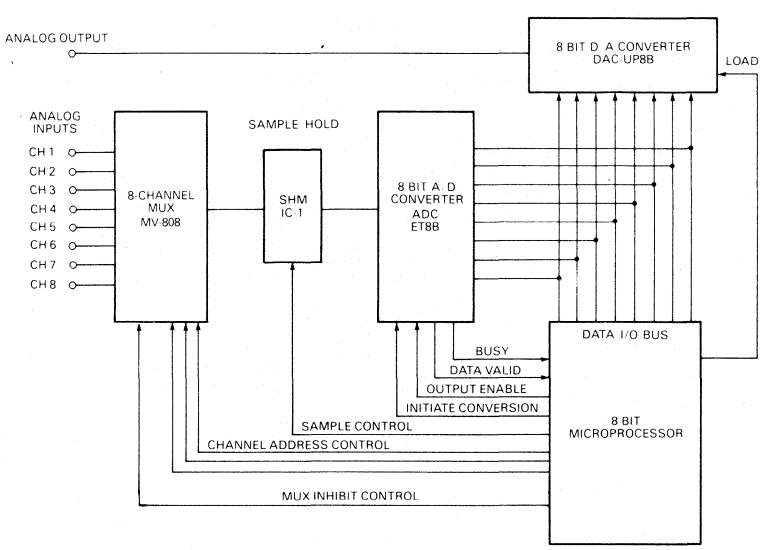
CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic HI to the start convert input (pin 21) to give free-running operation.

2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or -FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000 .... 000 and 000 .... 001.

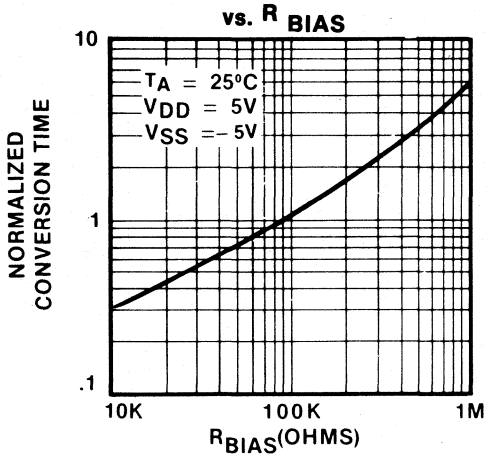
3. **Gain Adjustment.** Set the output of the reference source to +FS-1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111 .... 110 and 111 .... 111.

LOW COST MICROPROCESSOR A/D, D/A INTERFACE

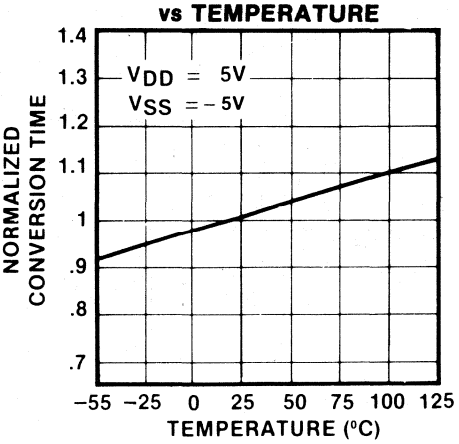


TYPICAL PERFORMANCE CURVES

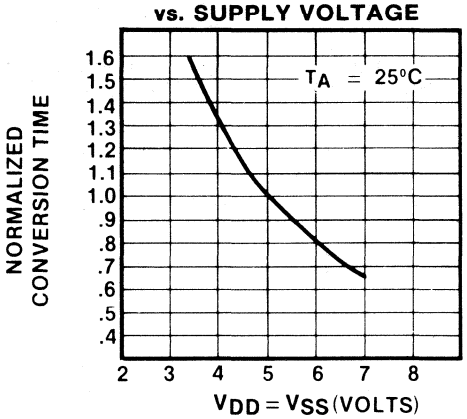
CONVERSION TIME vs. R_{BIAS}



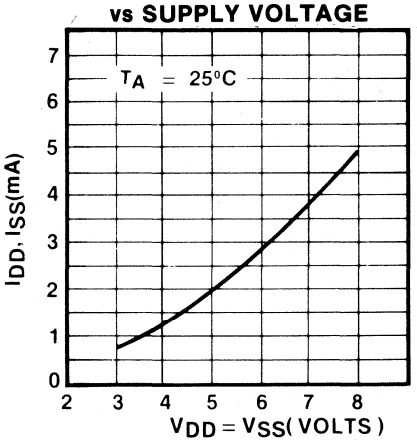
CONVERSION TIME vs TEMPERATURE



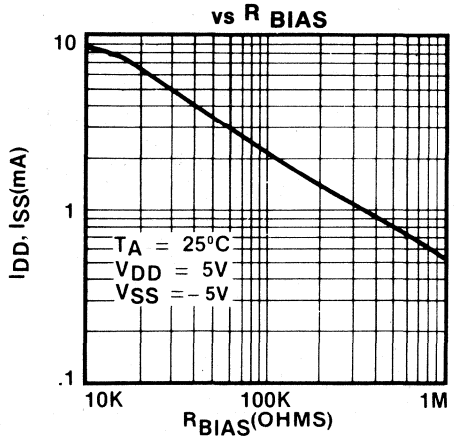
CONVERSION TIME vs. SUPPLY VOLTAGE



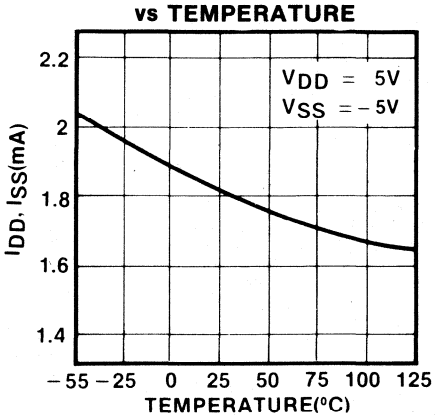
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

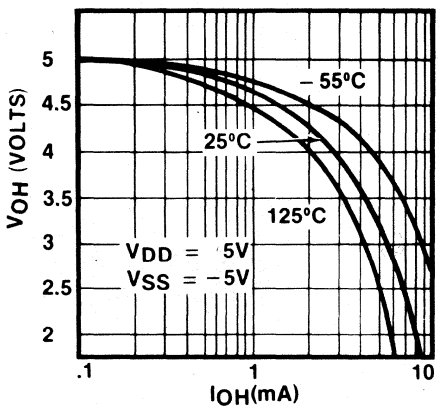


SUPPLY CURRENT vs TEMPERATURE

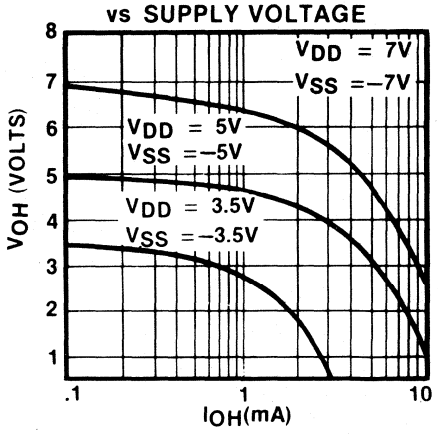


TYPICAL PERFORMANCE CURVES

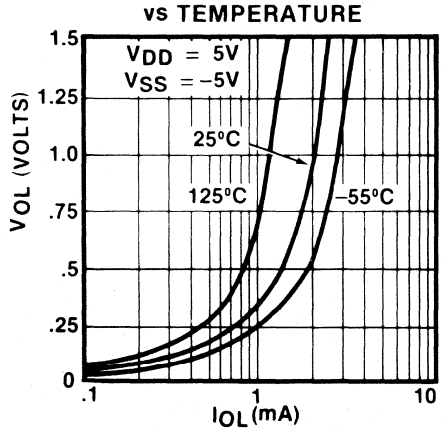
OUTPUT SOURCE CURRENT vs TEMPERATURE



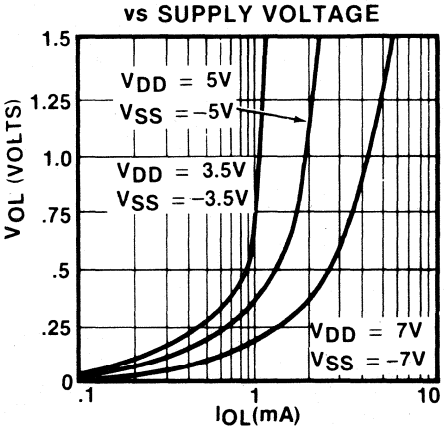
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



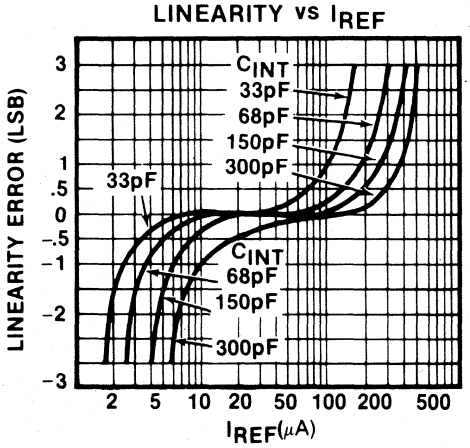
OUTPUT SINK CURRENT vs TEMPERATURE



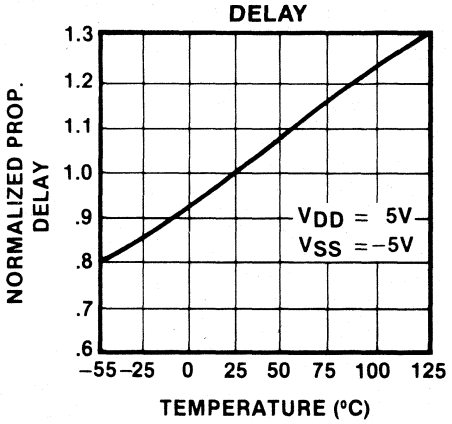
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}



THREE-STATE PROPAGATION DELAY



12 Bit, Low Power A/D Converter ADC-HC12B

FEATURES

- **Single Supply Operation**
- **Automatic Standby Mode Control**
- **Low Power Consumption**
- **Six Input Ranges**
- **MIL Temp Range Available**

GENERAL DESCRIPTION

The ADC-HC is a complete, 12 bit, low power analog to digital converter utilizing CMOS technology. This hybrid IC incorporates active laser trimming of highly stable thin-film resistors to provide module performance with IC price, size and reliability.

The device is ideal for portable and remote applications such as seismology, oceanography, meteorology, pollution monitoring and battery operation system. Other key applications include military and aerospace, requiring wide operating temperature range and high reliability.

The ADC-HC converter has the capability of operating from either a single +9V DC to +15V DC power source (interrupt power mode) or from a ±9VDC to ±15VDC power source (continuous power mode) at a maximum conversion rate of 3.3 kHz.

A key feature of this unit when operating in the interrupt power mode is the extremely low quiescent power consumption (less than 10μA @ 12V, 25°C).

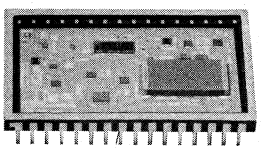
Upon receipt of a convert command, the analog circuitry of the converter is energized and stabilizes in 50 μsec. A complete conversion is performed at which time the EOC goes low, turning off the analog circuitry, and returns to its quiescent state. The digital data remains valid until it is updated by the next conversion.

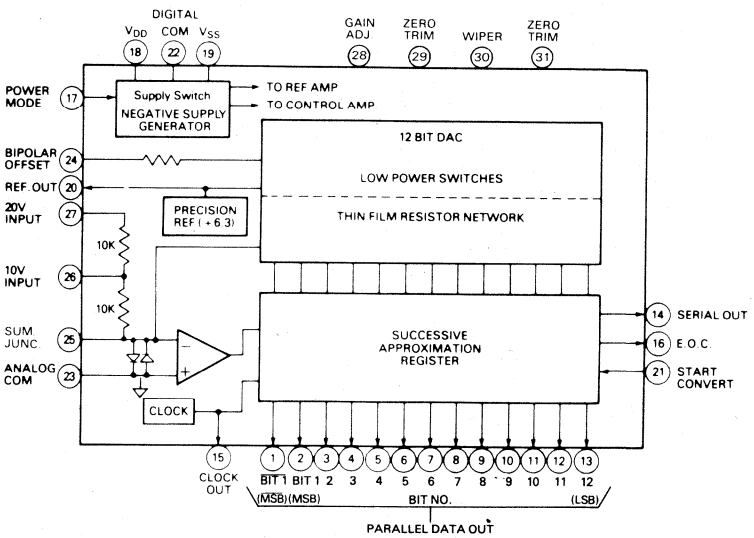
Power consumption is a function of conversion rate. For 100, 1K and 2K conversions per second, the average power drain is approximately 3.5, 26 and 50 milliwatts respectively.

Six input voltage ranges are provided by external pin connection: 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V, and ±10V. Nonlinearity is specified at ±½ LSB max. with a gain tempco of ±30 ppm/°C. Output coding is straight binary, offset binary or 2's complement. Serial data is also brought out.

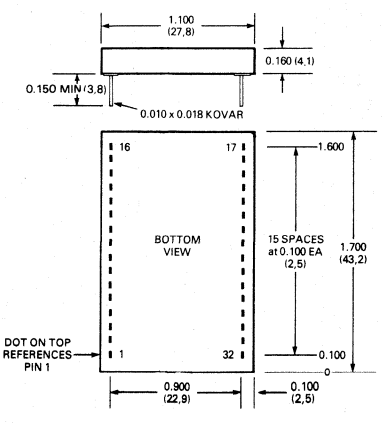
The converters are cased in 32 pin DIP packages. Models are available for three different operating temperature ranges: 0 to +70, −25 to +85 and −55 to +125 degrees centigrade. High reliability versions of each temperature range are also available.

CAUTION: The ADC-HC Series are CMOS devices and should be handled carefully to prevent static charge pickup which might damage the devices. The devices should be kept in the shipping containers until ready for installation.





MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 1 (MSB)
3	BIT 2
4	BIT 3
5	BIT 4
6	BIT 5
7	BIT 6
8	BIT 7
9	BIT 8
10	BIT 9
11	BIT 10
12	BIT 11
13	BIT 12 (LSB)
14	SERIAL OUT
15	CLOCK OUT
16	E.O.C. (STATUS)

PIN	FUNCTION
17	POWER MODE
18	V_{DD}
19	V_{SS}
20	REF OUT
21	START CONVERT
22	DIGITAL COM.
23	ANALOG COM.
24	BIPOLAR OFFSET
25	SUM. JUNC.
26	10V INPUT
27	20V INPUT
28	GAIN ADJ.
29	ZERO TRIM
30	ZERO ADJ (WIPER)
31	ZERO TRIM
32	N.C.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-HC12B
(Typical at 25°C, ±12V, unless otherwise noted)

MAXIMUM RATINGS

Positive Supply (V_{DD})	+18V
Negative Supply (V_{SS})	−18V
Analog Inputs	±25V
Digital Inputs	0 to V_{DD}

INPUTS

Analog Input Ranges, unipolar	0 to +5V, 0 to +10V, 0 to +20V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance	5K (0 to +5V, ±2.5V) 10K (0 to +10V, ±5V) 20K (0 to +20V, ±10V)
Start Convert, Interrupt Mode	Positive Pulse with duration of 50μS min.
Start Convert, Continuous Mode	Positive Pulse with duration of 5μS min.
V_{IL} (Logic "0")	0.05 V_{DD} max.
V_{IH} (Logic "1")	0.95 V_{DD} min.
Input Current	30 pA
Input Capacitance	15 pF

OUTPUTS

Parallel Output Data	12 parallel lines of data, held until next conversion command
V_{OL} (Logic "0")	0V, −2.0mA
V_{OH} (Logic "1")	V_{DD}, +4.0mA
All Digital Outputs	CMOS Compatible
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary, 2's Complement
Serial Output	NRZ successive decision pulses out MSB first, Straight Binary or Offset Binary
Clock Output	Train of positive going (V_{DD}) 25 μS pulses, 40 kHz
E.O.C. (Status)	Conversion Status Signal, Logic "1" during reset and conversion, Logic "0" when conversion complete (data valid)

PERFORMANCE

Resolution	12 Bits
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±½ LSB max.
Gain Error	Adjust to zero
Offset or Zero Error	Adjust to zero
Gain Tempco	±30 ppm/°C max.
Offset Tempco	±20 ppm/°C of FSR max.
Zero Tempco	±10 ppm/°C of FSR
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR
No Missing Codes	Guaranteed over operating temperature range
Conversion Time	300 μS max.
Throughput Time	305 μS max. continuous power mode 350 μS max. interrupt power mode
Power Supply Rejection	.003%/% Supply

POWER REQUIREMENT

Continuous Power Mode V_{DD}	+9.0V to +15.0V
V_{SS}	−9.0V to −15.0V
Interrupt Power Mode V_{DD}	+9V to +15.0V
Power Consumption, Continuous Mode	112 mW
Quiescent Mode	120μW max., 12μW typ.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to +70°C (BGC, BMC) −25°C to +85°C (BMR) −55°C to +125°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 oz. (14 g.)

TECHNICAL NOTES

1. The ADC-HC contains CMOS components and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive foam or shorting all pins together with aluminum foil. Do not connect in circuit under "power on" conditions. Digital signals should be applied after the converters power has been turned on.
2. It is recommended for single supply (+12V nominal) or dual supply (±12V nominal) operation, the power input pins should be bypassed to ground with a .1μF ceramic capacitor. It is not critical that the supplies be balanced.
3. Analog and digital grounds should be kept separate whenever possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Common (Pin 23) and Digital Ground (Pin 22) are not connected internally and must be tied together externally.
4. The ADC-HC can operate from either a single or dual supply. When using dual supplies, tie POWER MODE (Pin 17) to V_{DD} (Pin 18). In this continuous power mode, an A/D conversion will take place when a 5μsec. or greater positive going pulse is applied to START CONVERT (Pin 21). For single supply operation (interrupt power mode), tie Power Mode (Pin 17) to E.O.C. (Pin 16). When EOC goes low the converter is switched to standby mode (power is disconnected to analog circuitry) and digital output data becomes valid and remains valid until next start pulse is applied. Upon receipt of a 50 μsec. min., 500 usec. max. pulse on START CONVERT (Pin 21), the converter will stabilize, make a complete conversion and return to standby mode.
5. Digital output codes are listed in coding tables. Parallel data is valid when EOC is in low state. This data can be transferred into latches during logic "1" to logic "0" transition of EOC line. Serial data out (Pin 14) is in NRZ (non-return to zero) format. This data is guaranteed valid in a 50 nsec. to 300 nsec. time frame after positive edge of clock. All digital inputs and outputs are CMOS compatible. See application notes for CMOS-TTL interface.
6. REF OUT (Pin 20) is a 6.3V ±5% internal reference pin connection.
7. For zero or offset and gain adjustment refer to connections and calibration notes. The trim pots should be located as close as possible to the converter to avoid noise pickup. Zero point is always adjusted first followed by gain the adjustment with analog input at the most positive end of analog range. The range of the OFFSET (ZERO)ADJ. is ±15 mV. The range of GAIN ADJ. is .1% of full scale range can also be increased by decreasing the value of the series resistor (3.9 MΩ nominal). Potentiometer values are 10K and should be 100 ppm/°C ceramic type (such as Datel TP series).

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
ADC-HC12BMC	0 to +70°C	Hermetic
ADC-HC12BMR	−25°C to +85°C	Hermetic
ADC-HC12BMM	−55°C to +125°C	Hermetic

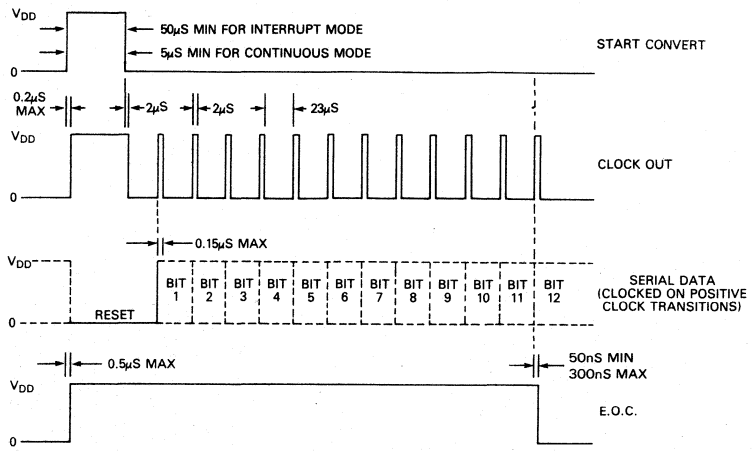
Trimming Potentiometers: TPK 10K (10K ohms)

For high reliability versions of the ADC-HC series, including units screened to MIL-STD-883 Level B, contact factory.

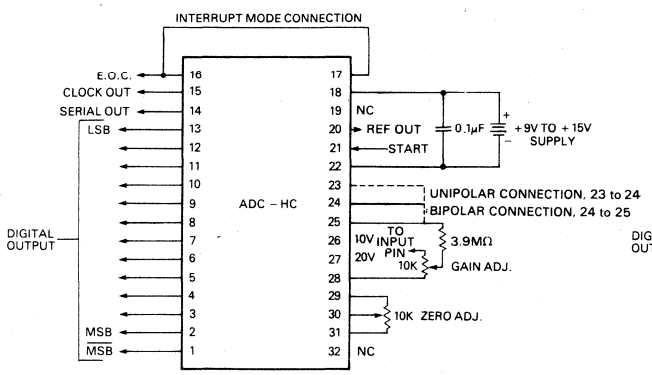
THE CONVERTERS ARE COVERED BY GSA CONTRACT

CONNECTIONS AND CALIBRATION

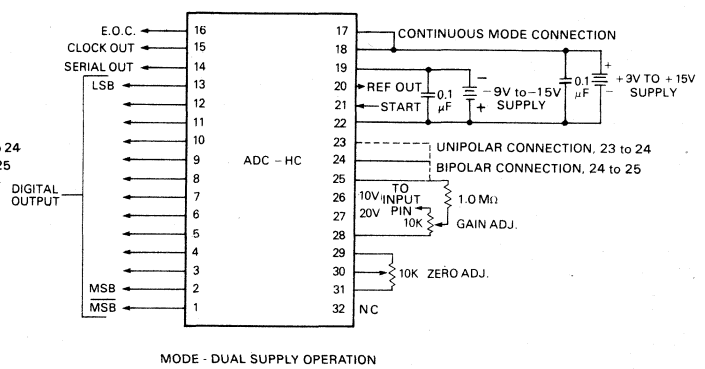
ADC-HC TIMING DIAGRAM



CONNECTIONS DIAGRAM



MODE - SINGLE SUPPLY OPERATION



MODE - DUAL SUPPLY OPERATION

OUTPUT CODING

INPUT VOLTAGE RANGE				CODING
	UNIPOLAR			STRAIGHT BINARY
	0 to +20V	0 to +10V	0 to +5V	MSB LSB
+FS-1 LSB	+19.9951	+9.9976	+4.9988	1111 1111 1111
+½ FS	+10.0000	+5.0000	+2.5000	1000 0000 0000
+1 LSB	+0.0049	+0.0024	+0.0012	0000 0000 0001
ZERO	0.0000	0.0000	0.0000	0000 0000 0000

	BIPOLAR			OFFSET BINARY*
	±10V	±5V	±2.5V	MSB LSB
+FS-1 LSB	+9.9951	+4.9976	+2.4988	1111 1111 1111
+½ FS	+5.0000	+2.5000	+1.2500	1100 0000 0000
+1 LSB	+0.0049	+0.0024	+0.0012	1000 0000 0001
ZERO	0.0000	0.0000	0.0000	1000 0000 0000
–FS-1 LSB	–9.9951	–4.9976	–2.4988	0000 0000 0001
–FS	–10.0000	–5.0000	–2.5000	0000 0000 0000

* For 2's COMPLEMENT, MSB is inverted, use $\overline{\text{MSB}}$ (pin 1)

INPUT PIN CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT THESE PINS TOGETHER
0 to +5V	26	23 to 24, 25 to 27
0 to +10V	26	23 to 24
0 to +20V	27	23 to 24
±2.5V	26	24 to 25, 25 to 27
±5V	26	24 to 25
±10V	27	24 to 25

CALIBRATION PROCEDURE

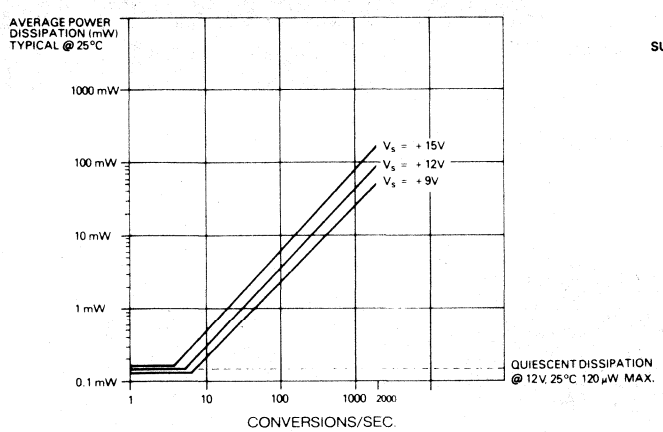
1. Connect converter as shown in the Connection Diagram. Use the Input Pin Connections table for the desired input voltage range. Apply start conversion pulses to start pin.

2. **Zero and Offset Adjustment.**
   Apply a precision voltage reference source between the selected analog input range and ground. Adjust the output of the reference source to + ½ LSB. Adjust zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 for unipolar and 1000 0000 0000 and 1000 0000 0001 for bipolar mode.

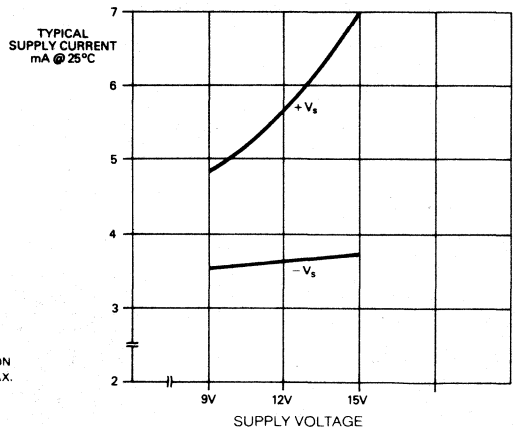
3. **Full Scale Adjustment**
   Change the output of the precision reference source for +FS-1½ LSB. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS

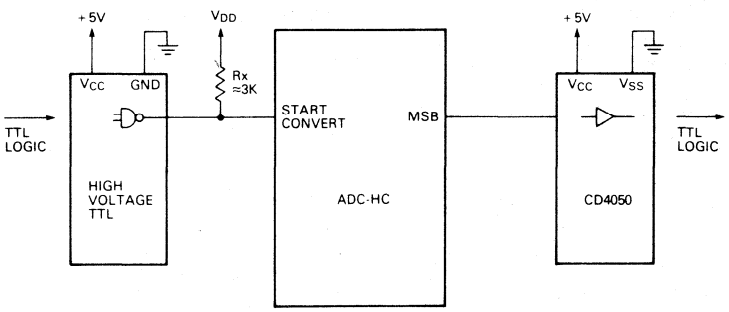
ADC-HC INTERRUPT POWER MODE



ADC-HC CONTINUOUS POWER MODE



TTL-CMOS INTERFACE

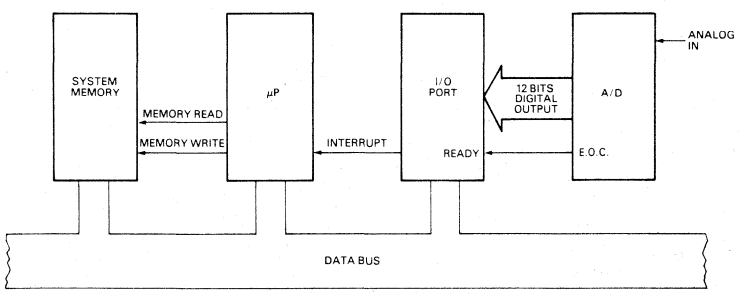


CMOS and TTL logic are not compatible due to different threshold levels. They can, however, be interfaced by simple techniques.

The START CONVERT (Pin 21) can be driven directly from an open collector, high voltage TTL gate. Resistor Rx is used to source current and bring the TTL output up to the CMOS threshold level. Typical values of Rx are 3.3K to 10K ohms.

CMOS to TTL interface requires sufficient sink current in the low state. The CD4049 (inverting) and CD4050 (noninverting) buffers, powered from +5V logic supply can accept input voltage swings of +5 to +15V from the CMOS system. Each buffer gate can drive at least one input from any TTL family.

LOW POWER MICRO-PROCESSOR INTERFACE



SYSTEMS COMPONENTS	MANUFACTURE	MODEL	DATA BITS	TYPE
LOW POWER MICROPROCESSOR	RCA	CDP1802	8	CMOS
	INTERSIL	IM6100	12	CMOS
A/D CONVERTER	DATEL SYSTEMS	ADC-HC	12	CMOS

12 Bit Microelectronic A/D Converter With Sample-Hold ADC-HS12B

FEATURES

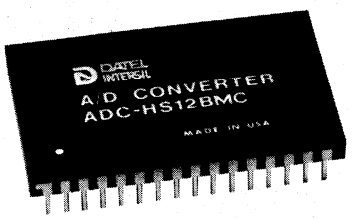
- **12 Bit Resolution**
- **Internal Sample Hold**
- **6μsec. Acquisition Time**
- **9μsec. Conversion Time**
- **Programmable Input Ranges**
- **Parallel & Serial Outputs**

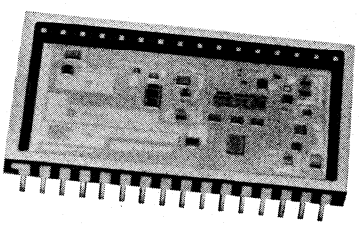
GENERAL DESCRIPTION

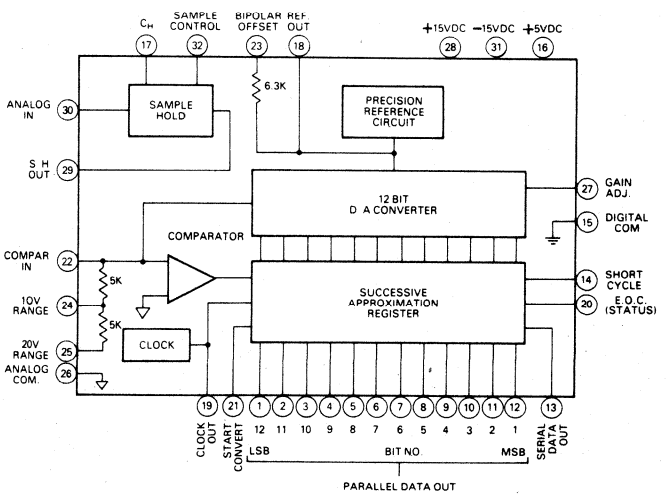
The ADC-HS12B is a high performance 12 bit hybrid A/D converter with a self-contained sample-hold. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The internal sample-hold has a 6μsec. acquisition time for a full 10V input change; the A/D converter has a fast 9μsec. conversion time. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. Input impedance to the sample-hold is 100 megohms. Output coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation, with both parallel and serial outputs brought out.

This converter incorporates proven thin film hybrid technology used in high volume production. Quad current switches are combined with a nichrome thin film resistor network to implement the internal 12 bit DAC. To achieve 9μsec. conversion time, the thin film resistors are fabricated on glass, giving lower stray capacitance. Other internal circuits include a precision zener reference, fast comparator, successive approximation register, clock, and sample hold. The thin film resistor network is functionally laser trimmed for optimum converter linearity.

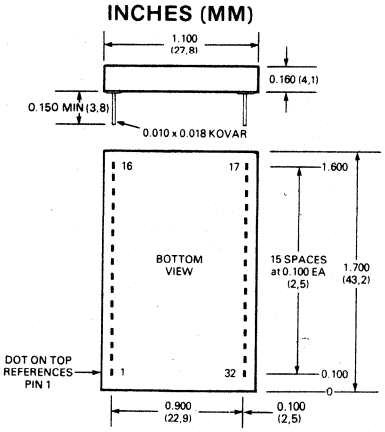
Other features include a gain tempco of 20ppm/°C maximum and differential nonlinearity tempco of ±2ppm/°C; there are no missing codes over the operating temperature range. The package is a miniature 32 pin triple spaced DIP and different models are offered for each of the operating temperature ranges: 0 to 70C, −25 to +85C, and −55 to +100C. Power supply requirement is ±15VDC and +5VDC. High reliability versions are also available.







MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CH
2	BIT 11 OUT	18	REF OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E O C (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ
12	BIT 1 OUT (MSB)	28	+15V POWER
13	SERIAL DATA OUT	29	S/H OUTPUT
14	SHORT CYCLE	30	ANALOG IN
15	DIGITAL COM	31	15V POWER
16	+5V POWER	32	SAMPLE CONTROL

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-HS12B

(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

MAXIMUM RATINGS

Positive Supply, pin 28	+18V
Negative Supply, pin 31	−18V
Logic Supply Voltage, pin 16	+5.5V
Digital Input Voltage, pins 14, 21, 32	+5.5V
Analog Input Voltage, pin 30	±15V

INPUTS

Analog Input Ranges, unipolar	0 to +5V, 0 to +10V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance[1]	100 megohms
Input Bias Current[1]	50nA typ., 200nA max.
Start Conversion	2V min. to +5.5V max. positive pulse with 100 nsec. duration min. Rise and fall times <30 nsec. Logic HI to LO transition resets converter and initiates next conversion. Loading: 1 TTL load
Sample Control Input	Logic HI = hold Logic LO = sample Loading: 1 TTL load

OUTPUTS[2]

Parallel Output Data	12 parallel lines of data held until next conversion command. VOUT ("0") ≤ +0.4V VOUT ("1") ≥ +2.4V
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary
Serial Output Data	Successive decision pulses out, NRZ format, MSB first
End of Conversion (status)	Conversion status signal. Output is logic HI during reset and conversion and LO when conversion is complete.
Clock Output	Train of positive going +5V, 100 nsec. pulses at 1.5 MHz rate.

SAMPLE-HOLD PERFORMANCE[3]

Input Offset Drift	25μV/°C
Acquisition Time, 10V to 0.01%	6μsec.
Bandwidth	1 MHz
Aperture Delay Time	100 nsec.
Aperture Uncertainty Time	10 nsec.
Sample to Hold Error	2.5mV max.
Hold Mode Droop	200nV/μsec. max.
Hold Mode Feedthrough	0.01% max.

CONVERTER PERFORMANCE

Resolution	12 bits (1 part in 4096)
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±½ LSB max.
Temp. Coefficient of Gain	±20ppm/°C max.
Temp. Coefficient of Zero, unipolar	±5ppm/°C of FSR max.
Temp. Coefficient of Offset, bipolar	±10ppm/°C of FSR max.
Differential Nonlinearity Tempco	±2ppm/°C of FSR
Missing Codes	None over oper. temp. range
Conversion Time	9μsec. max.
Power Supply Rejection	0.002%/% max.

POWER REQUIREMENT

+15VDC ±0.5V @ 60mA
−15VDC ±0.5V @ 50mA
+5VDC ±0.25V @ 100mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to 70°C (BMC) −25°C to +85°C (BMR) −55°C to +100°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 oz. (14 g.)

NOTES:

1. For sample-hold input
2. All digital outputs can drive 2 TTL loads
3. For 1000pF external hold capacitor

TECHNICAL NOTES

1. It is recommended that the −15V power input pins both be bypassed to ground with a .01μF ceramic capacitor in parallel with a 1μF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 1μF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01μF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100ppm/°C cermet types (such as Datel Systems TP series). The adjustment range is ±0.5% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. Calibration of the ADC-HS12B is performed with the sample-hold connected and operating dynamically. This results in adjusting out the sample-hold errors along with the A/D converter. For slow throughput applications it is recommended that a 0.01μF hold capacitor be used for best accuracy. With this value the acquisition time becomes 25μsec. and the external timing must be adjusted accordingly.
4. The recommended timing shown in the Timing Diagram allows 6 microseconds for the sample-hold acquisition and then 1 microsecond after the sample-hold goes into the hold mode to allow for output settling before the A/D begins its conversion cycle.
5. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example for an 8 bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions in the Table.
6. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary. In cases where bipolar coding of offset binary is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS−1LSB gives 1111 1111 1111.
7. These converters dissipate approximately 2 watts of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
8. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock. The pulse width of the external clock should be between 100 nsec. and 300 nsec. Each N bit converison cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8 bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-HS12BMC	0 to + 70C
ADC-HS12BMR	−25 to + 85C
ADC-HS12BMM	−55 to + 100 C

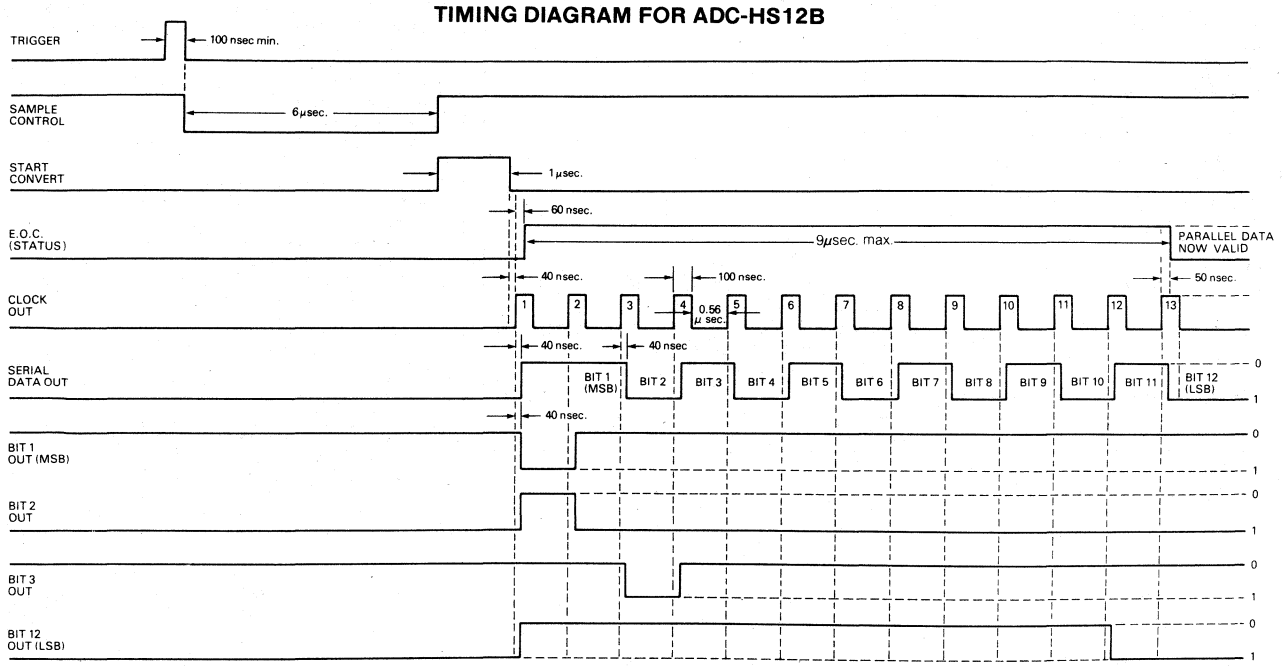
Mating Socket: DILS-2 (2 required per converter) at $3.30 each
Trimming Potentiometers: TP50K at $3.50 each

For high reliability versions of the ADC-HS12B including units screened to MIL-STD-883 level B, contact factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

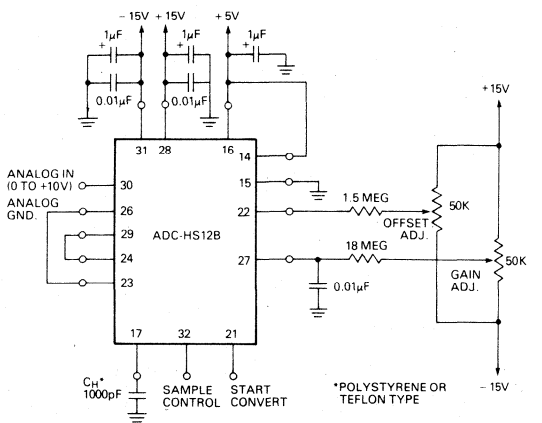
TIMING, CONNECTIONS, AND CODING

TIMING DIAGRAM FOR ADC-HS12B

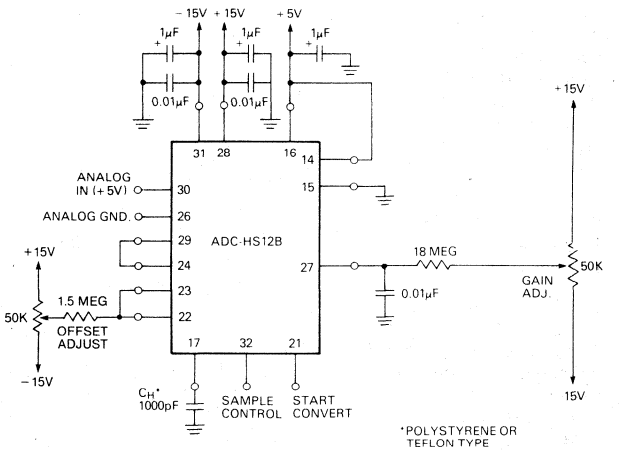


NOTE: TRIGGER, SAMPLE CONTROL, AND START CONVERT PULSES MUST BE EXTERNALLY GENERATED

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, ±5V



CODING TABLES

UNIPOLAR OPERATION

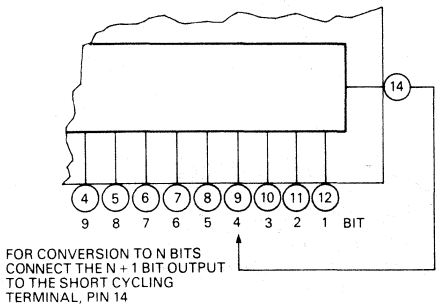
INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +5V	MSB		LSB
+9.9976V	+4.9988V	0000	0000	0000
+8.7500	+4.3750	0001	1111	1111
+7.5000	+3.7500	0011	1111	1111
+5.0000	+2.5000	0111	1111	1111
+2.5000	+1.2500	1011	1111	1111
+1.2500	+0.6250	1101	1111	1111
+0.0024	+0.0012	1111	1111	1110
0.0000	0.0000	1111	1111	1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		
±10V	±5V	±2.5V	MSB		LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000
+7.5000	+3.7500	+1.8750	0001	1111	1111
+5.0000	+2.5000	+1.2500	0011	1111	1111
0.0000	0.0000	0.0000	0111	1111	1111
−5.0000	−2.5000	−1.2500	1011	1111	1111
−7.5000	−3.7500	−1.8750	1101	1111	1111
−9.9951	−4.9976	−2.4988	1111	1111	1110
−10.0000	−5.0000	−2.5000	1111	1111	1111

CONNECTIONS AND CALIBRATION

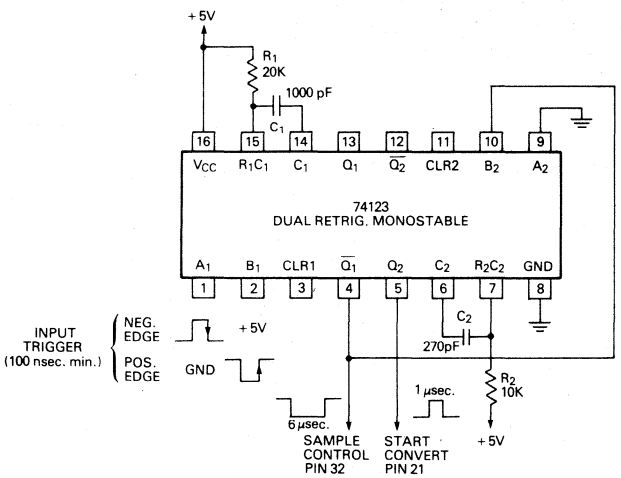
SHORT CYCLE OPERATION



PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	CONV. TIME
1	PIN 11	0.7 μsec.
2	PIN 10	1.3
3	PIN 9	2.0
4	PIN 8	2.6
5	PIN 7	3.3
6	PIN 6	4.0
7	PIN 5	4.6
8	PIN 4	5.3
9	PIN 3	6.0
10	PIN 2	6.6
11	PIN 1	7.3
12	PIN 16	9.0

RECOMMENDED CIRCUIT FOR GENERATING SAMPLE CONTROL AND START CONVERT PULSES



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER		
0 to +5V	29 & 24	22 & 25	23 & 26
0 to +10V	29 & 24	—	23 & 26
±2.5V	29 & 24	22 & 25	23 & 22
±5V	29 & 24	—	23 & 22
±10V	29 & 25	—	23 & 22

CALIBRATION PROCEDURE

1. Connect the ADC-HS12B as shown in one of the connection diagrams. The sample-hold and A/D converter should be timed as shown in the timing diagram. The trigger pulse should be applied at a rate of 70 kHz or less and should be 100 nsec. minimum width.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally betwen 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	−2.4994V +2.4982V
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

12-Bit Microelectronic Analog-to-Digital Converters ADC-HX, ADC-HZ Series

FEATURES

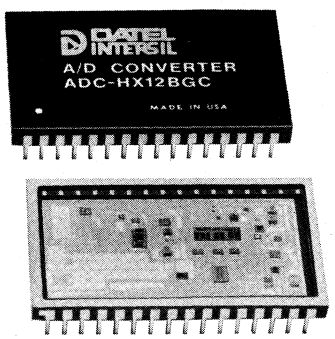
- **12 Bits Resolution**
- **8 or 20 μSec. Conversions**
- **5 Input Ranges**
- **Internal Hi Z Buffer**
- **Short Cycle Operation**

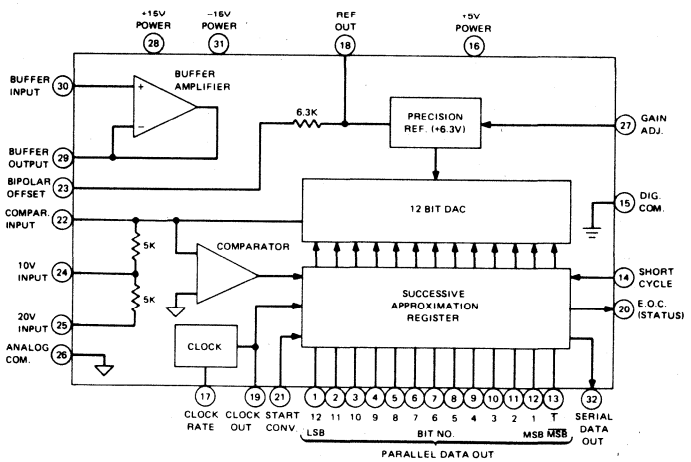
GENERAL DESCRIPTION

The ADC-HX12B and ADC-HZ12B are self-contained, high performance, 12 bit A/D converters manufactured with thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12 bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

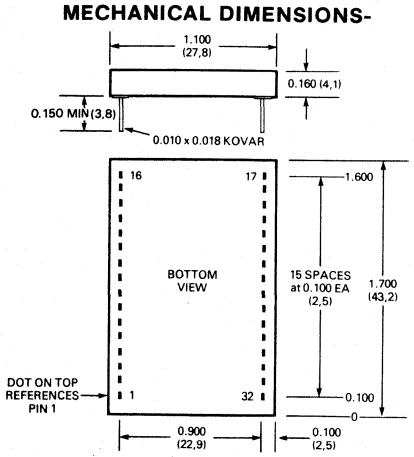
These converters utilize a fast 12 bit DAC consisting of tightly matched monolithic quad current switches, a stable nichrome thin-film resistor network, and a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12 bit successive approximation register, a clock, and a monolithic buffer amplifier. The thin-film resistor network is functionally trimmed by a laser to precisely set the 8-4-2-1 current weighting in the quad current switches. The close tracking of the thin-film resistor and quad current switches result in a differential nonlinearity tempco of only ±2ppm/°C. Gain tempco is ±20ppm/°C maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3μsec., the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary 2's complement. Serial data is also brought out. The package is a 32 pin ceramic case. Eight different models are offered covering the operating temperature ranges of 0 to 70°C, –25 to +85°C, and –55 to +100°C.





MECHANICAL DIMENSIONS-



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT
9	BIT 4 OUT	25	20V INPUT
10	BIT 3 OUT	26	ANALOG COM.
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT ($\overline{\text{MSB}}$)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM.	31	-15V POWER
16	+5V POWER	32	SERIAL OUTPUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-HX12B, ADC-HZ12B
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

	ADC-HX12B	ADC-HZ12B
INPUTS		
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V FS	
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V FS	
Input Impedance	2.5K (0 to +5V, ±2.5V) 5K (0 to +10V, ±5V) 10K (±10V)	
Input Impedance with Buffer	100 Megohms	
Input Bias Current of Buffer	125nA typ., 250nA max.	
Input Overvoltage	±15V	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100nsec. min. Rise and fall times <30nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 1 TTL load	
OUTPUTS[1]		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V	
Coding, unipolar	Complementary Binary	
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V 100nsec. pulses. 600 kHz for ADC-HX12B and 1.5MHz for ADC-HZ12B (pin 17 grounded).	
PERFORMANCE		
Resolution	12 bits (1 part in 4096)	
Nonlinearity	±1/2 LSB max.	
Differential Nonlinearity	±1/2 LSB max.	
Gain Error, before adjustment	±0.1%	
Zero Error, unipolar, before adj.	±.05% of FSR[3]	
Offset Error, bipolar, before adj.	±0.1% of FSR[3]	
Temp. Coeff. of Gain	±20ppm/°C max.	
Temp. Coeff. of Zero, unipolar	±5ppm/°C of FSR max.[3]	
Temp. Coeff. of Offset, bipolar	±10ppm/°C of FSR max.[3]	
Diff. Nonlinearity Tempco	±2ppm/°C of FSR[3]	
No Missing Codes	Over oper. temp. range	
Conversion Time[2], 12 bits	20 µsec. max.	8.0 µsec. max.
10 bits[4]	15 µsec. max.	6.0 µsec. max.
8 bits[4]	10 µsec. max.	4.0 µsec. max.
Buffer Settling Time, 10V step	3.0 µsec. to .01%	
Power Supply Rejection	.002% / % Supply max.	
POWER REQUIREMENT	+15VDC ±0.5V @ 55mA −15VDC ±0.5V @ 45mA + 5VDC ±0.25 @ 100mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0 to 70°C, -25 to +85°C, or -55 to +100°C	
Storage Temperature Range	-65°C to +150°C	
Package Size	1.700 x 1.100 x 0.160 inches	
Package Type	32 pin ceramic	
Pins	0.010 x 0.018 inch Kovar	
Weight	0.5 oz. (14g.)	

NOTES:

1. All digital outputs can drive 2 TTL loads.
2. Without buffer amplifier used. ADC-HZ12B may require external adjustment of clock rate.
3. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.
4. Short cycled operation.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a .01µF ceramic capacitor in parallel with a 1µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10µF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a .01µF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100ppm/°C cermet types (such as Datel-Intersil's TP series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.
4. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example for an 8 bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases the clock rate is also speeded up by connecting the clock rate adjust (pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.
5. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary or complementary 2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS−1LSB gives 1111 1111 1111.
6. These converters dissipate approximately 2 watts of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL	PRICE (1-24)
ADC-HX12BGC	0 to +70C	EPOXY	
ADC-HX12BMC	0 to +70C	HERM.	
ADC-HX12BMR	−25 to +85C	HERM.	
ADC-HX12BMM	−55 to +100C	HERM.	
ADC-HZ12BGC	0 to +70C	EPOXY	
ADC-HZ12BMC	0 to +70C	HERM.	
ADC-HZ12BMR	−25 to +85C	HERM.	
ADC-HZ12BMM	−55 to +100C	HERM.	

Mating Socket: DILS-2 (2/converter)

Trimming Potentiometers: TP2K, TP5K, TP10K, TP20K, TP50K or TP100K

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

TECH. NOTES (cont'd)

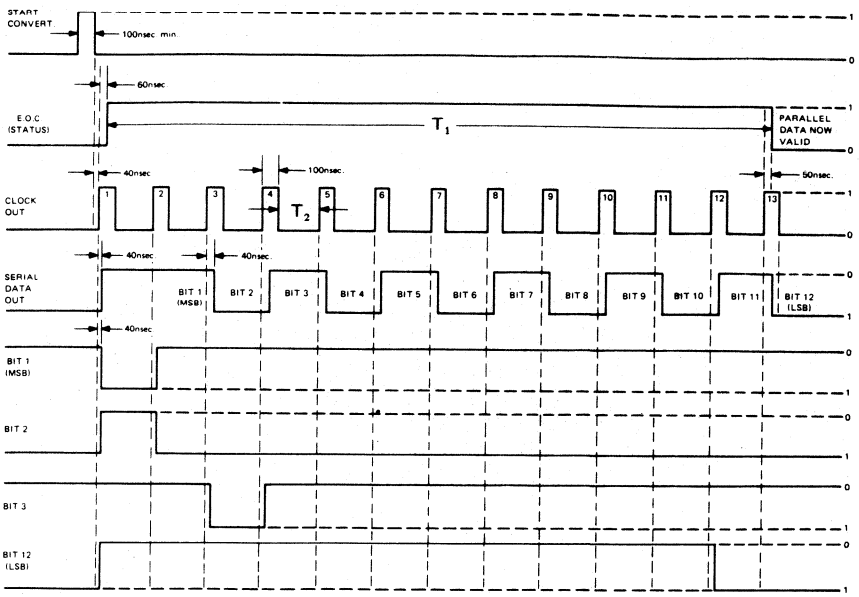
7. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see clock rate adjustment diagram) for the converter resolution selected. The pulse width of the external clock should be between 100 nsec. and 300 nsec. Each N bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8 bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

TIMING DIAGRAM OPERATING PERIODS

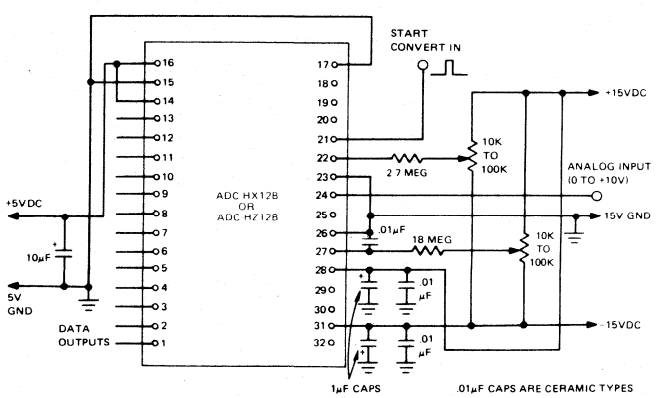
	ADC-HX12B	ADC-HZ12B
T_1	20 μsec.	8.0 μsec.
T_2	1.56 μsec.	0.56 μsec.

TIMING AND CONNECTION DIAGRAMS

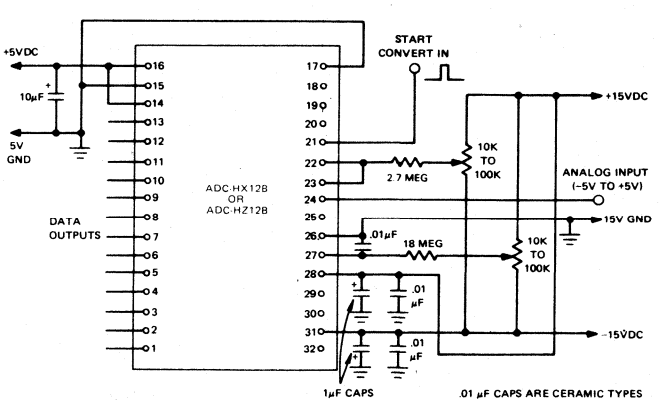
TIMING DIAGRAM FOR ADC-HX12B, ADC-HZ12B OUTPUT: 010101010101



UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, -5V TO +5V



CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +5V	MSB		LSB
+9.9976V	+4.9988V	0000	0000	0000
+8.7500	+4.3750	0001	1111	1111
+7.5000	+3.7500	0011	1111	1111
+5.0000	+2.5000	0111	1111	1111
+2.5000	+1.2500	1011	1111	1111
+1.2500	+0.6250	1101	1111	1111
+0.0024	+0.0012	1111	1111	1110
0.0000	0.0000	1111	1111	1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY			COMP. TWO'S COMPLEMENT		
±10V	±5V	±2.5V	MSB		LSB	MSB		LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000	1000	0000	0000
+7.5000	+3.7500	+1.8750	0001	1111	1111	1001	1111	1111
+5.0000	+2.5000	+1.2500	0011	1111	1111	1011	1111	1111
0.0000	0.0000	0.0000	0111	1111	1111	1111	1111	1111
–5.0000	–2.5000	–1.2500	1011	1111	1111	0011	1111	1111
–7.5000	–3.7500	–1.8750	1101	1111	1111	0101	1111	1111
–9.9951	–4.9976	–2.4988	1111	1111	1110	0111	1111	1110
–10.0000	–5.0000	–2.5000	1111	1111	1111	0111	1111	1111

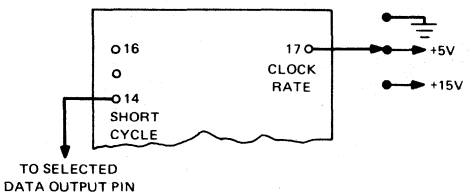
CONNECTIONS AND CALIBRATION

INPUT CONNECTIONS

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 TO +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 TO +10V	24	–	23 & 26	30	–	23 & 26	29 & 24
±2.5V	24	22 & 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	–	23 & 22	30	–	23 & 22	29 & 24
±10V	25	–	23 & 22	30	–	23 & 22	29 & 25

SHORT CYCLE OPERATION

CONNECTIONS



8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX12B CONV. TIME	20 µsec.	15 µsec.	10 µsec.
ADC-HZ12B CONV. TIME	8 µsec.	6 µsec.	4 µsec.
CONNECT THESE	17 & 15	17 & 16	17 & 28
PINS TOGETHER	14 & 16	14 & 2	14 & 4

CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE	
	ADC-HX12B	ADC-HZ12B
0V	600 kHz	1.5MHz
+5V	720 kHz	1.8MHz
+15V	880 kHz	2.2MHz

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO
1	PIN 11
2	PIN 10
3	PIN 9
4	PIN 8
5	PIN 7
6	PIN 6

RES. (BITS)	PIN 14 TO
7	PIN 5
8	PIN 4
9	PIN 3
10	PIN 2
11	PIN 1
12	PIN 16

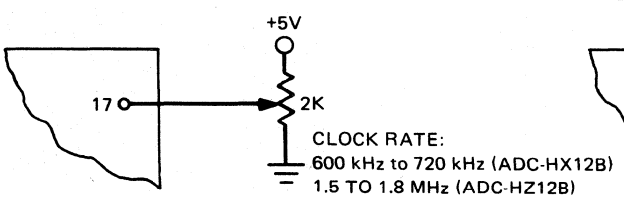
CALIBRATION PROCEDURE

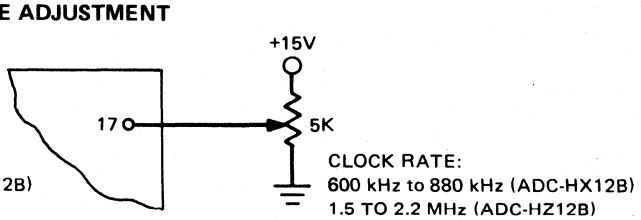
1. Connect converter as shown in the Standard Connection diagrams. Use the Input Connection Table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nsec. minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (–FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS–1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	–2.4994V
	GAIN	+2.4982V
±5V	OFFSET	–4.9988V
	GAIN	+4.9963V
±10V	OFFSET	–9.9976V
	GAIN	+9.9927V

CLOCK RATE ADJUSTMENT





NEW

DATEL

10 & 12 Bit Military and Industrial A/D Converters ADC-84, ADC-85, ADC-87

PRELIMINARY

FEATURES

- ADC-87: Military Version
- ADC-84/85: Industrial Versions
- MIL-STD-883B Versions Available
- High Performance Design
- Industry Standard Converter

GENERAL DESCRIPTION

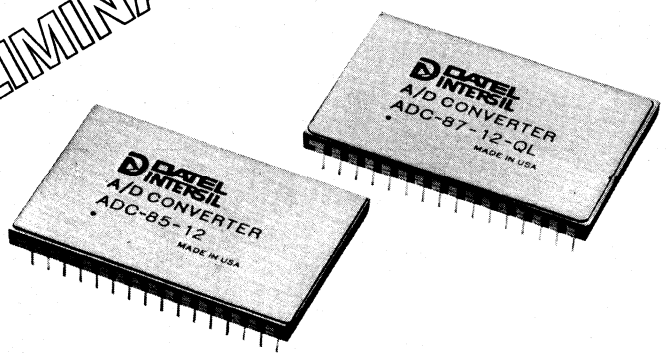
Datel-Intersil's ADC-84, ADC-85 and ADC-87 series devices are high performance, low cost 10- and 12-bit successive approximation analog to digital converters. Direct replacements for standard ADC-84, 85 and 87 converters, these devices offer improved performance and reliability.

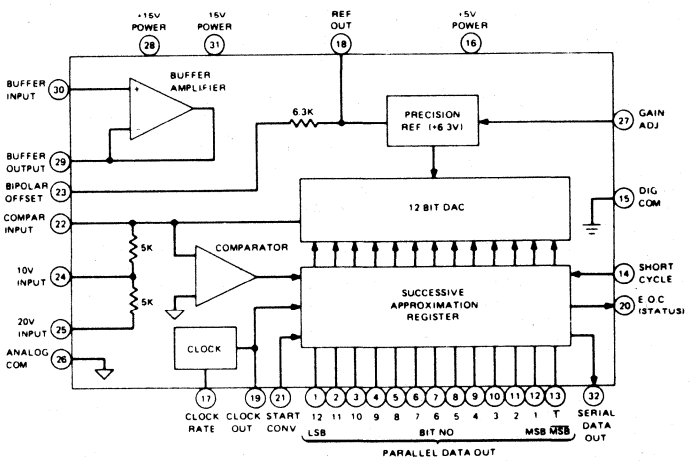
The ADC-87 is specified for operation over the full military operating temperature range of −55°C to +125°C. Versions of this model, screened to MIL-STD-883, class B, by Datel-Intersil's stringent QL program are available. The ADC-84 and ADC-85 are the same converter specified over the commercial, 0 to +70°C and the industrial, −25°C to +85°C, temperature ranges.

These devices are complete, self-contained units including an internal clock, precision +6.3V reference, comparator, and input buffer amplifier. Each converter is available in two performance grades; 12 bits of resolution at a maximum conversion speed of 10 μsec, or 10 bits of resolution at a conversion speed of 6 μsec maximum. Faster conversion speeds at lower resolutions are possible with short cycle operation. The maximum linearity error for all models is ± ½ LSB.

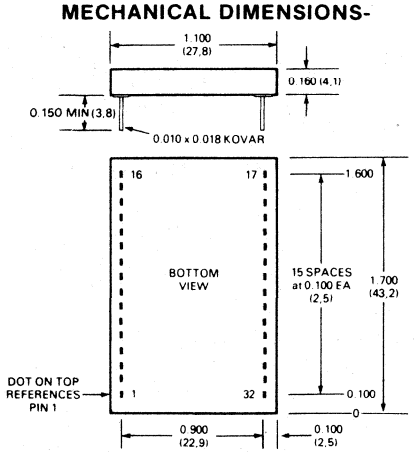
Internal thin-film scaling resistors are provided for the selection of analog input signal ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, or ±10V. Output coding is complementary binary, complementary offset binary, or complementary 2's complement. All digital inputs and outputs are fully DTL and TTL compatible and output data is available in either serial or parallel form.

These converters are packaged in a 32 pin ceramic package, the ADC-85 and ADC-87 being hermetically sealed. Power supply requirement is ±15 VDC and ±5 VDC.





MECHANICAL DIMENSIONS-



NOTE PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	*BIT 12 OUT (LSB)	17	CLOCK RATE
2	*BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT
9	BIT 4 OUT	25	20V INPUT
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT (MSB)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM.	31	−15V POWER
16	+5V POWER	32	SERIAL OUTPUT

*NO CONNECTION ON 10 BIT MODELS

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-84, ADC-85, ADC-87
Typical at +25°C, ±15 VDC and +5 VDC supplies unless otherwise noted

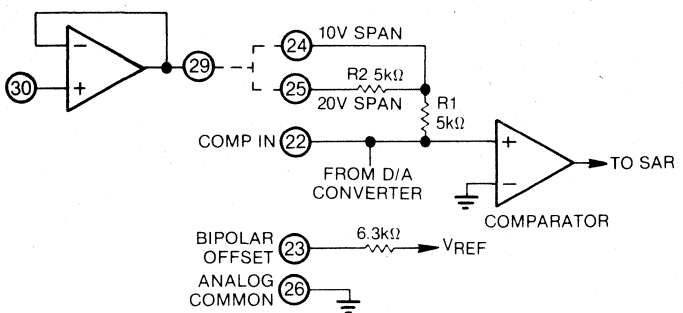
	ADC-87		ADC-85		ADC-85C		ADC-84	
RESOLUTION	**10 Bits**	**12 Bits**	**10 Bits**	**12 Bits**	**10 Bits**	**12 Bits**	**10 Bits**	**12 Bits**
ANALOG INPUTS								
Voltage Ranges, Unipolar	0 to +5V, 0 to +10V							
Bipolar	±2.5V, ±5 V, ±10V							
Impedance (Direct Input)								
0 to +5V, ±2.5V	2.5 kΩ							
0 to +10V, ±5V	5 kΩ							
±10V	10 kΩ							
Buffer Amplifier								
Impedance, min.	100 MΩ							
Bias Current	500 nA							
Settling Time[1]	2 μsec							
DIGITAL INPUTS[2]								
Convert Command	Positive Pulse, 50 nsec min., Trailing Edge initiates conversion							
Logic Loading	1TTL Load							
TRANSFER CHARACTERISTICS								
Gain Error[3]	±0.1% typ., ±0.25% max.							
Offset Error[3], Unipolar	±0.5% of FSR[4] typ., ±0.2% of FSR max.							
Bipolar	±0.1% of FSR typ., ±0.25% of FSR max.							
Linearity Error[5], max.	± ½ LSB							
Inherent Quantization Error	± ½ LSB							
Differential Linearity Error	± ½ LSB							
No Missing Codes	−55°C to +125°C		−25°C to +85°C		0°C to +70°C		0°C to +70°C	
Power Supply Sensitivity, ±15V	±0.004% of FSR/% Supply							
+5V	±0.001% of FSR/% Supply							
DRIFT								
Specification Temperature Range	−55°C to +125°C		−25°C to +85°C		0°C to +70°C		0°C to +70°C	
Full Scale Absolute Accuracy Error, Max.[6]								
+25°C	±0.1% FSR		-----		-----		-----	
−55°C to +125°C	±0.3% FSR		-----		-----		-----	
Gain, max.	±20 ppm/°C		±20 ppm/°C	±15 ppm/°C	±40 ppm/°C	±25 ppm/°C	±30 ppm/°C	
Offset, Unipolar	±5 ppm/°C		±3 ppm/°C		±3 ppm/°C		±3 ppm/°C	
Bipolar, max.	±10 ppm/°C		±10 ppm/°C	±7 ppm/°C	±20 ppm/°C	±12 ppm/°C	±15 ppm/°C	
Linearity, max.	±3 ppm/°C		±3 ppm/°C	±2 ppm/°C	±3 ppm/°C		±3 ppm/°C	
Monotonicity	Guaranteed Over Temperature							
CONVERSION SPEED, max.	6 μsec	10 μsec	6 μsec	10 μsec	6 μsec	10 μsec	6 μsec	10 μsec
DIGITAL OUTPUT								
Parallel								
Output Codes								
Unipolar	Complementary Straight Binary							
Bipolar	Complementary Offet Binary, Complementary Two's Complement							
Output Drive	2 TTL Loads							
Serial Data Codes, NRZ	Complementary Straight Binary, Complementary Offset Binary							
Output Drive	2 TTL Loads							
Status	Logic "1"During Conversion							
Status Output Drive	2 TTL Loads							
Internal Clock								
Clock Output Drive	2 TTL Loads							
Frequency	1.9 MHz	1.2 MHz	1.9 MHz	1.2 MHz	1.9 MHz	1.2 MHz	1.9 MHz	1.2MHz
INTERNAL REFERENCE								
VOLTAGE	+6.3V ±15 mV max.							
Maximum External Current	1 mA							
Tempco of Drift, max	±5 ppm/°C		±5 ppm/°C		±10 ppm/°C		±20 ppm/°C	
POWER REQUIREMENTS								
Rated Voltages	±15V, +5V							
Range for Rated Accuracy	±13.5V to ±16.5V and +4.75V to +5.25V							
Supply Drain, max., +15V	25 mA							
−15V	30 mA							
+5V	100 mA							
Total Power Dissipation, max.	1100 mW							
TEMPERATURE RANGE								
Specification	−55°C to +125°C		−25°C to +85°C		0°C to +70°C		0°C to +70°C	
Operating (Derated Specs)	---		---		−25°C to +85°C		−25°C to +85°C	
Storage	−55°C to +125°C							
PACKAGE	Hermetic Ceramic		Hermetic Ceramic		Hermetic Ceramic		Ceramic	

1. Specified for 20V step to 0.01%. This settling time adds to conversion speed when buffer is connected to input.
2. DTL/TTL compatible, Logic "0" = +0.8V max., Logic "1" = +2.0V min. for inputs. For digital outputs Logic "0" = + 0.4V max., Logic "1" = +2.4V min.
3. Adjustable to Zero.
4. FSR is Full Scale Range
5. ± ½ LSB is equal to ±0.048% of FSR for 10 bits of resolution and ±0.012% of FSR for 12 bits of resolution.
6. Absolute Accuracy Error includes offset, gain, linearity and all other errors. Because this error is measured and specified without adjustment, it includes all factors that may affect the devices accuracy at the point of measurement.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PACKAGE SEAL	PRICE (1-24)
12 Bit Resolution — 10 μsec Conversion Time			
ADC-84-12	0°C to +70°C	Epoxy	$
ADC-85C-12	0°C to +70°C	Hermetic	$
ADC-85-12	−25°C to +85°C	Hermetic	$
ADC-87-12	−55°C to +125°C	Hermetic	$
10 Bit Resolution - 6 μsec Conversion Time			
ADC-84-10	0°C to +70°C	Epoxy	$
ADC-85C-10	0°C to +70°C	Hermetic	$
ADC-85-10	−25°C to +85°C	Hermetic	$
ADC-87-10	−55°C to +125°C	Hermetic	$
Mating Socket: DILS-2 (2/converter)			$
Trimming Potentiometers: TP2K, TP5K, TP10K, T020K, TP50K or TP100K			$

INPUT SCALING



Input Signal Range	Output Code	Buffered Or Direct Input: Pin 23 to pin	Buffered Or Direct Input: Pin 25 to	Buff. Input Only Pin 29 to pin	Dir. Input Only Input to pin
±10V	COMP OFF BIN[1]	22	INPUT	25	25
±5V	COMP OFF BIN[1]	22	open	24	24
±2.5V	COMP OFF BIN[1]	22	pin 22	24	24
0 to +5V	COMP BIN	26	pin 22	24	24
0 to +10V	COMP BIN	26	open	24	24

1. For 2's complementary coding use MSB

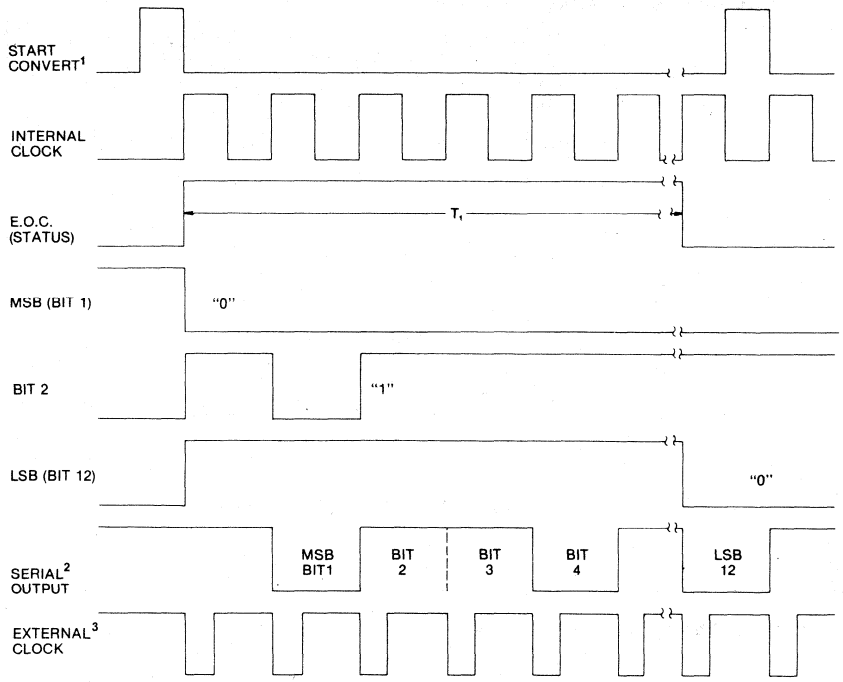
In order to utilize the maximum signal resolution of these converters, the analog input should be scaled as close to the maximum input signal range as possible. The analog input signal can be connected directly to the converter (pin 24 or pin 25) or through the internal buffer amplifier (pin 30). If the buffer amp is not used, pin 30 should be grounded. For the desired input range, connect the converter as shown in the input range selection table.

TECHNICAL NOTES

1. The ±15V (pins 28 and 31) and +5V (pin 16) power input pins should be bypassed to ground with a .01 μF ceramic capacitor in parallel with a 1 μF electrolytic capacitor. In addition, pin 27 should be bypassed to ground with a .01 μF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams (Pg. 60). The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/°C cermet types (such as Datel-Intersil's TP series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.
4. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary or complementary 2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS-1 LSB gives 1111 1111 1111.
5. These converters will accept an external clock if this is required for system synchronization. Connect the external clock to the START CONVERT pin (pin 21); the start convert command shown in the timing diagram is not used. The external clock must be a negative going pulse with a width between 100 and 200 nanoseconds. A total of 13 pulses are necessary to perform conversion; the falling edge of the following pulse will initiate a new conversion.
6. These converters dissipate approximately 1 watt of power. To operate at elevated temperatures, good thermal contact should be established between the case bottom and the circuit board ground plane by use of a silicone thermal joint compound. Care should be taken not to restrict air circulation in the vicinity of the converter.
7. Applications of these converters that require the use of a Sample-Hold may be satisfied by Datel-Intersil's SHM-6. The SHM-6 is a high speed hybrid Sample-Hold featuring 1.0 μsec acquisition time, 0.01% accuracy, programmable gains from ±1 to ±10 and a ±10V output range.

TIMING AND CONNECTION

TIMING DIAGRAM



T_1

12 bit models — 10μsec
10 bit models — 6μsec

NOTES:

1. The start convert pulse must be at least nsec wide and must remain low during conversion. The conversion is initiated by the trailing edge of the start convert command.
2. Use trailing edge of clock to strobe serial output.
3. The optional external clock pulse must be a negative going pulse with a width between 100 nsec and 200 nsec.

CODING TABLES

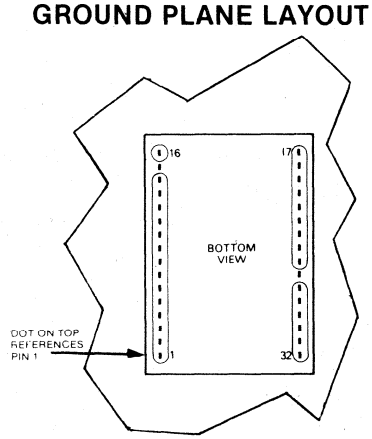
UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +5V	MSB		LSB
+9.9976V	+4.9988V	0000	0000	0000
+8.7500	+4.3750	0001	1111	1111
+7.5000	+3.7500	0011	1111	1111
+5.0000	+2.5000	0111	1111	1111
+2.5000	+1.2500	1011	1111	1111
+1.2500	+0.6250	1101	1111	1111
+0.0024	+0.0012	1111	1111	1110
0.0000	0.0000	1111	1111	1111

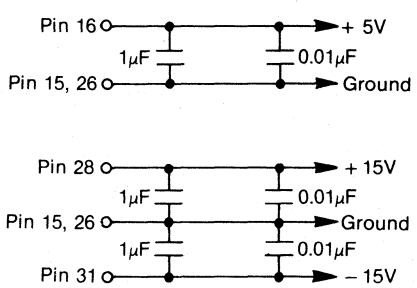
BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY			COMP. TWO'S COMPLEMENT		
±10V	±5V	±2.5V	MSB		LSB	MSB		LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000	1000	0000	0000
+7.5000	+3.7500	+1.8750	0001	1111	1111	1001	1111	1111
+5.0000	+2.5000	+1.2500	0011	1111	1111	1011	1111	1111
0.0000	0.0000	0.0000	0111	1111	1111	1111	1111	1111
−5.0000	−2.5000	−1.2500	1011	1111	1111	0011	1111	1111
−7.5000	−3.7500	−1.8750	1101	1111	1111	0101	1111	1111
−9.9951	−4.9976	−2.4988	1111	1111	1110	0111	1111	1110
−10.0000	−5.0000	−2.5000	1111	1111	1111	0111	1111	1111

GROUND PLANE LAYOUT



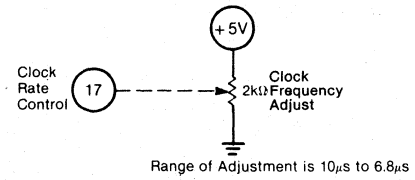
POWER SUPPLY DECOUPLING



CONNECTION AND CALIBRATION

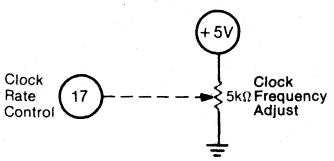
CLOCK RATE CONTROL

12 Bit Resolution



Range of Adjustment is 10μs to 6.8μs

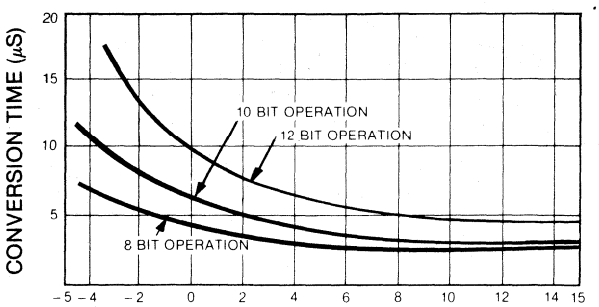
8 or 10 Bit Resolution



Range of Adjustment is 6μs to 4.0μs for 10 Bit and 3.5μs For 8 Bit Resolutions.

High conversion speeds may be obtained by connecting the CLOCK RATE pin (pin 17) to an external multi-turn trim potentiometer as shown. The potentiometer should have a TCR of 100 ppm/°C or less.

Conversion Time vs. Clock Rate Control Voltage



SHORT CYCLE CONNECTION

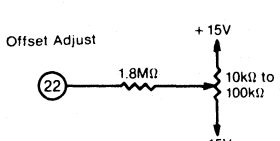
For applications requiring less than 12 bits of resolution, these converters may be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at N bits, simply connect the N + 1 bit output to the short cycle pin (pin 14).

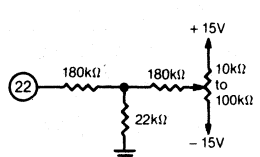
Conversion Time vs. Bit Resolution

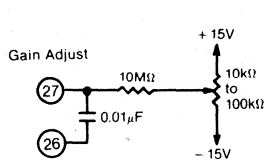
Resoltuion (Bits)	12	10	8
Maximum Conversion Time (μS)	10	6	4
Maximum Nonlinearity at 25°C (% of F.S.R.)	0.012	0.048	0.20
Connect Pin 17 to	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4

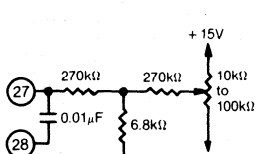
OPTIONAL EXTENAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external trim potentiometers. Multiturn potentiometers with 100 ppm/°C or better TCR of any value from 10 KΩ to 100 KΩ are recommended for minimum drift over temperature and time. The Gain Adjust pin (pin 27) and Offset Adjust pin (pin 22) may be left open if no external adjustment is required.









Calibration Procedure

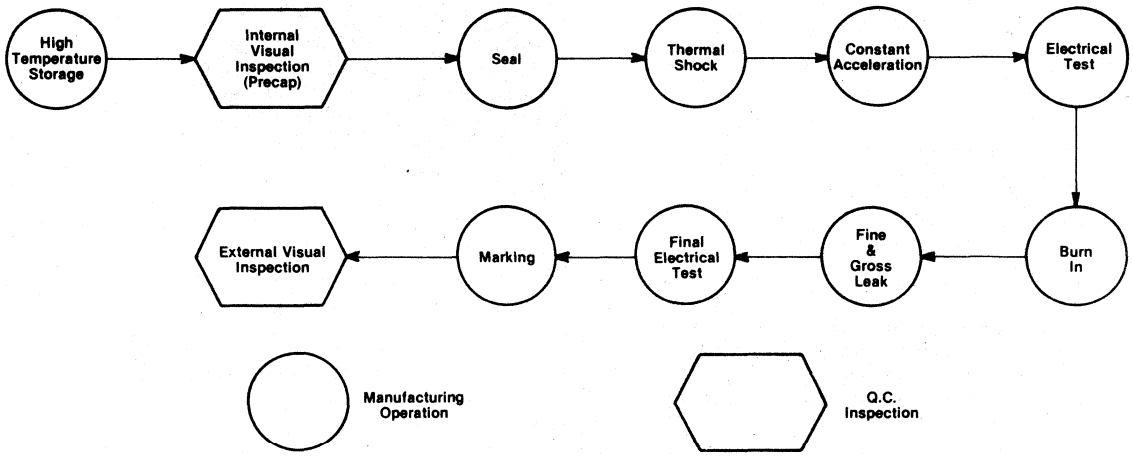
1. Apply a + ½ LSB analog input and adjust the OFFSET ADJ. potentiometer (pin 22) for a digital output that alternates between 111 . . . 11 and 111 . . . 10.
2. Apply a (FS − ½ LSB) analog input and set the GAIN ADJ. potentiometer (pin 27) for a digital output that alternates between 000 . . . 01 and 000 . . . 00.

Bipolar

1. Apply a (− FS + ½ LSB) analog input and adjust the OFFSET ADJ. potentiometer (pin 22) for a digital output that alternates between 111 . . . 11 and 111 . . . 10.
2. Apply a (+ FS − ½ LSB) analog input and adjust the GAIN ADJ. potentiometer (pin 27) for a digital output that alternates between 000 . . . 01 and 000 . . . 00.

MIL-STD-883B PROCESSING QL PROGRAM

Military and Aerospace programs require high reliability devices subjected to rigorous screening procedures. To meet this need, Datel-Intersil has developed its QL program, a high level of screening, strictly in accordance with MIL-STD-883, method 5008, Class B. All devices in this program are hermetically sealed and designated with the suffix "QL". The ADC-87 is available with 100% screening to Datel-Intersil's QL program. The following flow diagram and chart briefly summarize the test procedures followed by the QL program in conformance with MIL-STD-883B. For more complete information, contact your nearest sales office for Datal-Intersil's brochure "HIGH RELIABILITY HYBRID MICROCIRCUITS FOR DATA ACQUISITION".



TEST	METHOD	PURPOSE
HIGH TEMPERATURE STORAGE	Method 1008, Test condition C, 24 hrs @ +150°C	Eliminates device failure due to storage at elevated temperatures.
INTERNAL VISUAL (PRECAP)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical or thermal stress.
SEAL, FINE AND GROSS	Method 1014, test condition A (fine), 5×10^{-7} cc/sec., test condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
THERMAL SHOCK[1]	Method 5011, test condition A, 15 cycles @ 0°C to +100°C.	Determines resistance of device to sudden exposure to extreme temperate changes. Removes potential failures due to thermal stress on bonds, etc.
CONSTANT ACCELERATION	Method 2001, test condition A, Y, AXIS, 10Kg.	Eliminates potential failures due to structural or mechanical weaknesses not detected in shock or vibration tests.
BURN-IN TEST	Method 1015, test condition B, 160 hrs @ +125°C.	Stresses device at or above maximum rated operating temperature in order to eliminate infant mortality failures.
FINAL ELECTRICAL TESTS	Performed at +25°C, and at maximum & minimum operating temperatures.	Verifies that device still meets specified data sheet parameters.
EXTERNAL VISUAL	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

1. Per MIL-STD-883B. Thermal shock may be substituted for temperature cycling; however, temperature cycling, method 1010, condition C is available upon request

14 Bit, 50 Microsecond Analog-to-Digital Converter ADC-149

FEATURES

- **14 Bit Resolution**
- **50 μsec. Conversion Time**
- **Low Price**
- **Unipolar or Bipolar Inputs**
- **15ppm/°C Gain Temp. Coeff.**

GENERAL DESCRIPTION

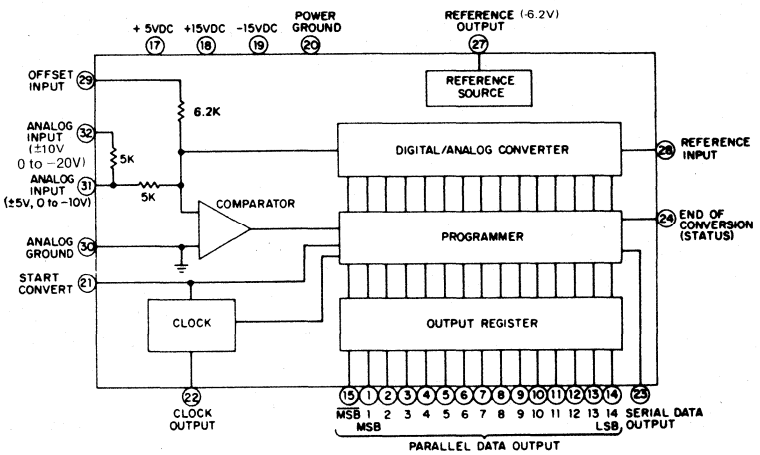
The ADC-149 is a 14 bit successive approximation type analog to digital converter for OEM use. It was specifically designed to give high resolution and accuracy at moderate cost for incorporation into precision instruments for process control systems and test and measurement systems.

This converter accepts either unipolar or bipolar input voltages of 0 to −10V, 0 to −20V, ±5V, or ±10V full scale by external pin connection and performs a 14 bit conversion in 50 μsec. Several output codes are available including straight binary for unipolar inputs and either offset binary or two's complement for bipolar inputs. Two's complement is obtained by using the $\overline{\text{MSB}}$ output pin. Reverse coding sense is used with the most negative analog input corresponding to full scale digital output. A serial data output is also provided and has a nonreturn-to-zero (NRZ) format. Logic outputs ate DTL/TTL compatible and will drive 6 standard TTL loads.

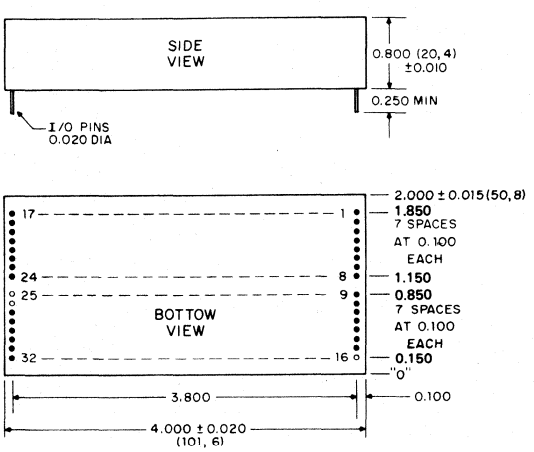
The ADC-149 can resolve 1 part in 16,384 giving an operating dynamic range of 84.3dB. On the 10 volt full scale range it can detect an input change of less than 1 millivolt. Accuracy is adjustable to ±.005% of full scale ±½LSB. The temperature coefficient is held to a low ±15ppm/°C over the 0° to 70°C operating temperature range.

This converter is encapsulated in a compact 2X4X0.8 inch module with DIP compatible pin spacing for PC board mounting. It can be stored from −55°C to +85°C. Power supplies required are standard ±15VDC and +5VDC. (Available from Datel's line of modular power supplies.)

The high resolution and accuracy of the ADC-149 make it particularly valuable in applications such as moderate speed data reduction, and computer arithmetic processing of analog inputs. Digitizing inputs from sensors and transducers allows data transmission or storage with drastically reduced degradation of accuracy compared to analog methods. This is also vital for automatic process and alarm limit computer control, and digital linearization of logarithmic or special function analog inputs. The ADC-149 offers at least a $100. price advantage over competitive converters in these applications.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN HOLES DESIGNATE WHERE PINS ARE OMITTED

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13	BIT 13
14	BIT 14 (LSB)
15	$\overline{\text{BIT 1 (MSB)}}$
16	NOT USED
17	+5V POWER
18	+15V POWER
19	−15V POWER
20	POWER GROUND
21	START CONVERT
22	CLOCK OUTPUT
23	SERIAL OUTPUT
24	END OF CONVERT (STATUS)
25	NOT USED
26	NOT USED
27	REFERENCE OUTPUT
28	REFERENCE INPUT
29	OFFSET INPUT
30	ANALOG GROUND
31	ANALOG IN (0 to +10, ±5V)
32	ANALOG IN (±10V)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS (Typical @ +25°C unless noted)

INPUTS

Analog Input Range (single-ended input referenced to ground) . . . . . ±5V FS, ±10V FS
0 to -10V FS, 0 to -20V FS

Input Overvoltage . . . . . ±15VDC without damage to unit.

Input Impedance . . . . . 5K Ohms (±5V and 0 to -10V FS range)
10K Ohms (±10V and 0 to −20V FS range)

Start of Conversion . . . . . +2.5V min. to +5.5V max. positive pulse with 150 nsec. min. duration.
Loading: 1mA
Logic "1" resets converter
Logic "0" initiates conversion

OUTPUTS

Parallel Output Data . . . . . 14 parallel lines of data held until the next conversion command.
Vout (Logic "0") ≤ +0.4V
Vout (Logic "1") ≥ +2.4V
Each output capable of driving up to 6 TTL loads.

Coding . . . . . Straight Binary (Unipolar Input)
Offset Binary (Bipolar Input)
Two's Complement (Bipolar Input)
Pin 15 provides MSB output for this coding. (Reverse coding sense used).

Serial Output . . . . . NRZ successive decision pulse output generated during conversion with MSB first. LO = "1", HI = "0"
Straight binary or offset binary coding

End of Conversion . . . . . Conversion Status Signal
Vout (Logic "0") ≤ +0.4V conversion complete
Vout (Logic "1") ≥ +2.4V during reset and conversion period.

Clock . . . . . Internal clock output, positive going 3 microsecond pulse. Loading up to 6 TTL loads.

PERFORMANCE

Resolution . . . . . 14 Bits (one part in 16,384)
Linearity Error . . . . . ±½ LSB max.
Temperature Coefficient of Gain . . . . . ±15ppm/°C
Temperature Coefficient of Zero Unipolar . . . . . ±10ppm/°C
Bipolar . . . . . ±10ppm/°C
Conversion Time . . . . . 50μsec. max.
Throughput Rate 20kHz
Power Requirements . . . . . ±15VDC ±0.5VDC @ 80mA max.
+5VDC ±0.25 VDC @ 200mA max.

PHYSICAL-ENVIRONMENTAL

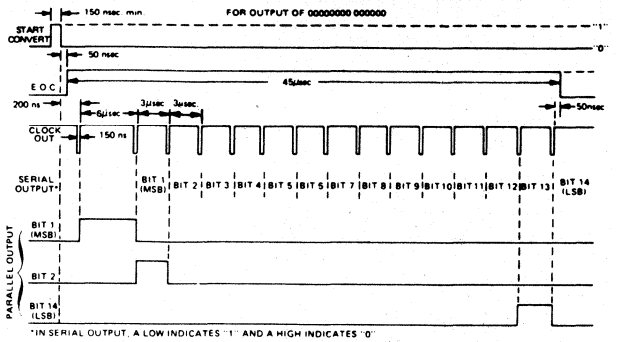
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range -55°C to +85°C
Relative Humidity . . . . . Up to 100% non-condensing
Size . . . . . 2"W×4"L×0.8" H
Pins . . . . . .020" round, gold plated, 0.250" long min.
Case Material . . . . . Black Diallyl Phthalate per MIL-M-14
Weight . . . . . 8 oz.
Mating Sockets . . . . . DILS-2, 2 required @ $6/pair

ORDERING INFORMATION — PRICE

Model ADC-149-14B

Mating Socket DILS 2 (2 per module,

TIMING FOR ADC-149-14B

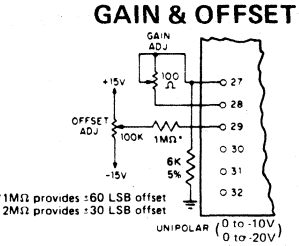


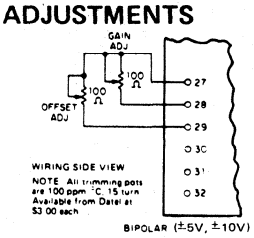
OUTPUT DIGITAL CODING

BIPOLAR						UNIPOLAR		
Analog Input Range		Offset Binary		Z's Complement (MSB Output)		Analog Input Range 0 to	Straight Binary	
±5V FS	±10V FS	MSB	LSB	MSB	LSB	-10V FS	MSB	LSB
+5.0000	+10.0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0		1 0 0 0 0 0 0 0 0 0 0 0 0 0		0 0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0	
+2.5000	+ 5.0000	0 1 0 0 0 0 0 0 0 0 0 0 0 0		1 1 0 0 0 0 0 0 0 0 0 0 0 0		0.0006	0 0 0 0 0 0 0 0 0 0 0 0 0 1	
+0.0006	+ 0.0012	0 1 1 1 1 1 1 1 1 1 1 1 1 1		1 1 1 1 1 1 1 1 1 1 1 1 1 1		-2.5000	0 1 0 0 0 0 0 0 0 0 0 0 0 0	
0.0000	0.0000	1 0 0 0 0 0 0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0 0 0 0 0 0 0		5.0000	1 0 0 0 0 0 0 0 0 0 0 0 0 0	
-2.5000	- 5.0000	1 1 0 0 0 0 0 0 0 0 0 0 0 0		0 1 0 0 0 0 0 0 0 0 0 0 0 0		-7.5000	1 1 0 0 0 0 0 0 0 0 0 0 0 0	
-4.9994	- 9.9988	1 1 1 1 1 1 1 1 1 1 1 1 1 1		0 1 1 1 1 1 1 1 1 1 1 1 1 1		-9.9994	1 1 1 1 1 1 1 1 1 1 1 1 1 1	

NOTE: *Reverse coding sense is used with the most negative analog input corresponding to full scale digital output. Normal coding sense can be obtained by using an external inverting amplifier. Or complementary binary can be used by adjusting for a 1 LSB offset.

GAIN & OFFSET ADJUSTMENTS





Adjustment Procedure — Unipolar Input

A. Connect a precision pulse generator to the "Start Convert" input terminal. See specifications for pulse width and amplitude.
B. Connect a precision voltage reference source to the appropriate analog input terminals. See I/O Connections.

Zero Offset Control

Adjust the voltage output from the reference to minus ½ LSB. Rotate the zero offset control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

Full Scale Gain Control

Adjust the output from the reference source to full scale minus 1½ LSB. Rotate the gain control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

Adjustment Procedure — Bipolar Input

A. Connect a precision pulse generator to the "Start Convert" input terminals. See specifications for pulse width and amplitude.
B. Connect a precision voltage reference source to the appropriate analog input terminals. See I/O connections.

Zero Offset Control

Adjust the voltage output from the reference source to plus full scale minus ½ LSB.
Rotate the offset control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

Gain Control

Adjust the output from the reference source to minus full scale minus 1½ LSB.
Rotate the gain control until LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

TRIMMING OF 3 MOST SIGNIFICANT BITS (INTERNAL)

The three trimming potentiometers on the side of the module are for periodic adjustment of the three most significant bits. Normally no adjustment of these trims is necessary since they are calibrated at the factory at 25°C. Should readjustment be required for optimum accuracy at a different temperature or to compensate periodically for long term drift, the following procedure should be carefully followed:

1. Adjust external offset and gain as above.
2. Readjust external gain trim and then bits 3, 2, and 1 in accordance with the table below. Adjust so that the output flickers equally between the two codes shown.
3. Readjust external zero or offset and gain.
4. Repeat steps 2 and 3 as necessary.

Input Voltage		Output Code	Adjustment
Unipolar (0 to -10V)	Bipolar (±5V)		
-0.625V -1/2 LSB (-0.62531V)	+4.375V -1/2 LSB (+4.37469V)	00010 . . . 01 00010 . . . 00	Gain Trim
-1.25V -1/2 LSB (-1.25031V)	+3.75V -1/2 LSB (+3.74969V)	00100 . . . 01 00100 . . . 00	Trim #3 (Bit 3)
-2.5V -1/2 LSB (-2.50031V)	+2.50V -1/2 LSB (+2.49969V)	01000 . . . 01 01000 . . . 00	Trim #2 (Bit 2)
-5.0V -1/2 LSB (-5.00031V)	0V -1/2 LSB (-0.00031V)	10000 . . . 01 10000 . . . 00	Trim #1 (Bit 1)

NEW

DATEL

12-Bit, High Speed Hybrid A/D Converter ADC-810, ADC-811

PRELIMINARY

FEATURES

- 2 μsec Max. Conversion Time
- 12-Bit Resolution
- Industry-Standard Pin-Out
- −55°C to +125°C Operation
- MIL-STD-883B Versions Available

GENERAL DESCRIPTION

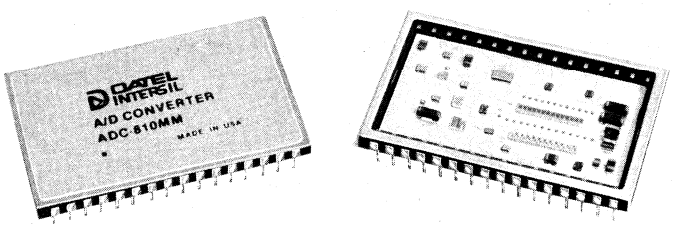
DATEL-INTERSIL's ADC-810 and ADC-811 are high speed, high performance 12-bit analog to digital converters manufactured with thin-film hybrid technology. Utilizing the successive approximation conversion technique, the ADC-810 achieves a 12-bit conversion in a maximum of only 2 μsec. Conversion time for the ADC-811 is 4 μsec maximum, this being the only difference between the two units. Both models are pin-compatible with industry standard ADC-85/87 converters, offering increased speed, high accuracy and reliability over the full military temperature range.

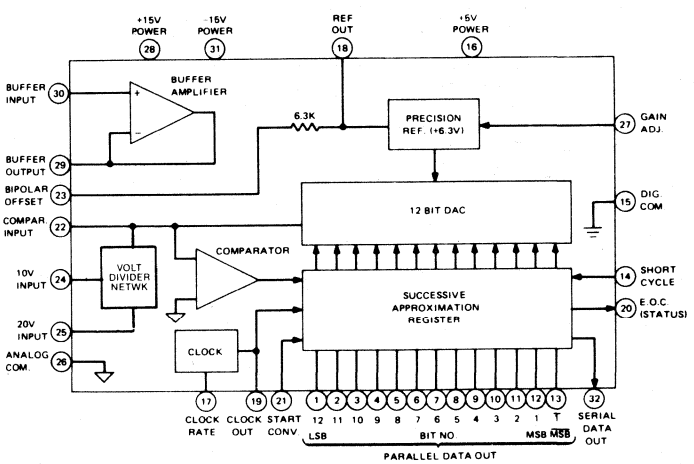
These converters feature four pin-programmable input voltage ranges: 0 to +10V, 0 to +20V, ±5V, and ±10V. A user selectable input buffer amplifier is included for applications where 100 MΩ input impedance is required. Other specifications include a maximum nonlinearity of ± ½ LSB, and a gain tempco of 25 ppm/°C maximum. The differential nonlinearity tempco is ± 2 ppm/°C maximum.

Output data is available in parallel or serial form. Output coding is complementary binary, complementary offset binary or complementary 2's complement. All digital outputs are TTL compatible.

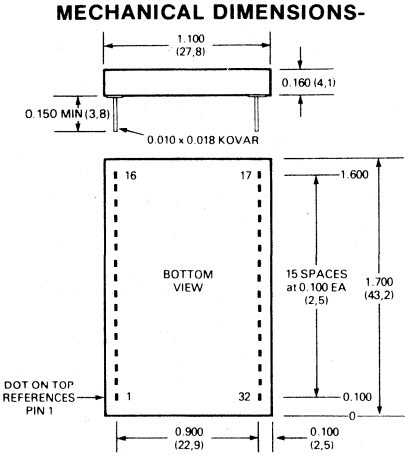
The ADC-810 and ADC-811 are a good choice for numerous commercial, industrial and military applications requiring high speed, hybrid reliability, low cost and small size. Such applications include FFT analysis, radar digitation, medical instrumentation, and high speed multiplexed data acquisition systems.

Power requirement for both converters is ±15V and +5V. Models are available for operation over the commercial, 0°C to +70°C, industrial, −25°C to +85°C and military −55°C to +125°C temperature ranges. All devices are packaged in a 32-pin, hermetically sealed, ceramic case. Versions processed to MIL-STD-883 Class B are available.





MECHANICAL DIMENSIONS-



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT
9	BIT 4 OUT	25	20V INPUT
10	BIT 3 OUT	26	ANALOG COM.
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT ($\overline{\text{MSB}}$)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM.	31	15V POWER
16	+5V POWER	32	SERIAL OUTPUT

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-810, ADC-811
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

	ADC-810	ADC-811
INPUTS		
Analog Input Ranges, unipolar[1]	0 to +10V FS, 0 to +20V FS	
Analog Input Ranges, bipolar[1]	±5V, ±10V FS	
Input Impedance	1.05 kΩ (0 to +10V, ±5V) 4.2 kΩ (0 to +20V, ±10V)	
Input Impedance with Buffer	100 Megohms	
Input Bias Current of Buffer	125 nA typ., 250 nA max.	
Input Overvoltage[2]	±15V	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 50 nsec. min. Rise and fall times < 30 nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 1 TTL load	
OUTPUTS[3]		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("0") ≥ +2.4V	
Coding, unipolar	Complementary Binary	
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding.	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V, 70 nsec. pulses. 6.66 MHz for ADC-810, and 3.33 MHz for ADC-811 (Pin 17 grounded).	
PERFORMANCE		
Resolution	12 bits (1 part in 4096)	
Nonlinearity, max.	± 1/2 LSB	
Differential Nonlinearity, max.	± 1/2 LSB	
Gain Error, max., before adjustment	±0.1%	
Zero Error, max., unipolar, before adj.	±0.1% of FSR[4]	
Offset Error, max., bipolar, before adj.	±0.1% of FSR[4]	
Temp. Coeff. of Gain, max.	±20 ppm/°C	
Temp. Coeff. of Zero, unipolar, max.	±10 ppm/°C of FSR[5]	
Temp. Coeff. of Offset, bipolar, max.	±10 ppm/°C of FSR[5]	
Diff. Nonlinearity Tempco, max.	±2 ppm/°C of FSR	
Conversion Time[4], 12 bits	2.0 μsec. max.	4.0 μsec. max.
10 bits[6]	1.7 μsec. max.	3.6 μsec. max.
8 bits[6]	1.4 μsec. max.	3.2 μsec. max.
Buffer Settling Time, 10V step	500 nsec to 0.01%	
Power Supply Rejection max.	.002% / % Supply max.	
POWER REQUIREMENTS		
Analog Supply, positive	+15 VDC ±0.5V @ 70 mA max.	
negative	−15 VDC ±0.5V @ 30 mA max.	
Logic Supply	+5 VDC ±0.25V @ 240 mA max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range, MC	0°C to +70°C	
MR	−25°C to +85°C	
MM	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Package Size	1.700 × 1.100 × 0.160 inches	
Package Type	32 pin ceramic	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.5 oz. (14g.)	

NOTES:

1. For information on models with 0 to +5V and ±2.5V input voltage ranges, please contact the Factory.
2. The input buffer cannot be used with the 0 to +20V input range.
3. All digital outputs can drive 2 TTL loads.
4. Without buffer amplifier used. ADC-810/811 may require external adjustment of clock rate.
5. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.
6. Short cycled operation.

TECHNICAL NOTES

1. Use of good high frequency circuit board layout techniques is required for rated performance. Digital common (Pin 15) and analog common (Pin 26) are not connected internally and therefore must be connected as directly as possible externally. The extensive use of a ground plane for all common connections is highly recommended. Also, it is recommended that the analog and digital supplies be externally bypassed with a .01 μF ceramic capacitor in parallel with a 1 μF electrolytic capacitor. The ±5V supply should be bypassed to ground with a 10 μF electrolytic capacitor. Additionally, Pin 27 (Gain Adjust) should be bypassed to ground with a .01 μF ceramic capacitor.

2. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/°C cermet types (such as DATEL-INTERSIL's TP Series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.

3. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting Pin 14 to the output bit following the last bit desired. For example, for an 8 bit conversion, Pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases, the clock rate is also speeded up by connecting the clock rate adjust (Pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.

4. These converters dissipate 2.8 watts of power. The case to ambient thermal resistance is approximately 20°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter. Also it is recommended that the converter be mounted directly to the circuit board (without the use of a mounting socket) and that good thermal contact be established between the case bottom and the circuit board grounded plane by use of a silicone thermal joint compound such as Wakefield type 120 or equivalent. For operation in ambient temperatures exceeding 83°C, air flow of at least 400 linear feet per minute is recommended.

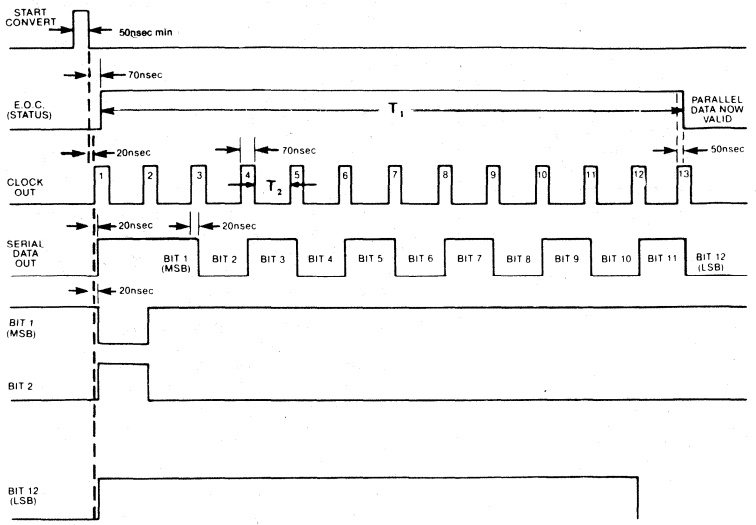
ORDERING INFORMATION

MODEL	TEMP. RANGE	PRICE (1-24)
ADC-810MC	0°C to +70°C	$
ADC-810MR	−25°C to +85°C	$
ADC-810MM	−55°C to +125°C	$
ADC-811MC	0°C to +70°C	$
ADC-811MR	−25°C to +85°C	$
ADC-811MM	−55°C to +125°C	$

Mating Socket: DILS-2 (2/converter)
Trimming Potentiometers: TP__ $

TIMING AND CONNECTION

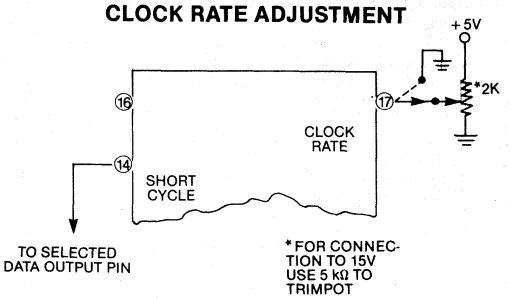
TIMING DIAGRAM FOR ADC-810, ADC-811
OUTPUT: 010101010101



TIMING DIAGRAM OPERATING PERIODS

ADC-810	ADC-811
T_1 2.0 μsec.	4.0 μsec.
T_2 98 nsec.	258 nsec.

CLOCK RATE ADJUSTMENT



CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE	
	ADC-811	ADC-810
0V	3.2 MHz	6.5 MHz
+5V	3.6 MHz	7.8 MHz
+15V	4.0 MHz	8.1 MHz

CLOCK RATE ADJUSTMENT RANGE

5V.2 kΩ TRIM POT
6.5 MHz to 7.8 MHz (ADC-810)
3.2 MHZ to 3.6 MHz (ADC-811)

15V.5 kΩ TRIM POT
6.5 MHz to 8.1 MHz (ADC-810)
3.2 MHZ to 4 MHz (ADC-811)

SHORT CYCLE OPERATION

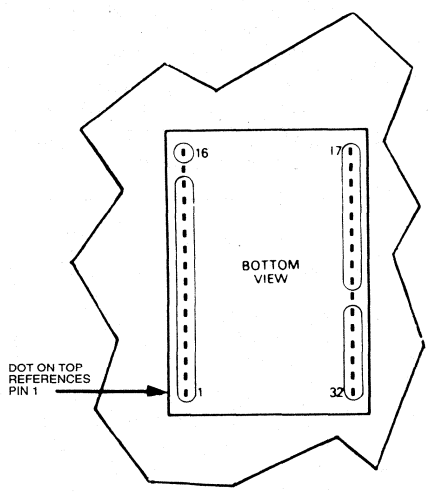
8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-810 CONV. TIME	2 μsec	1.7 μsec	1.4 μsec
ADC-811 CONV. TIME	4 μsec	3.6 μsec	3.2 μsec
CONNECT THESE	17 & 15	17 & 16	17 & 28
PINS TOGETHER	14 & 16	14 & 2	14 & 4

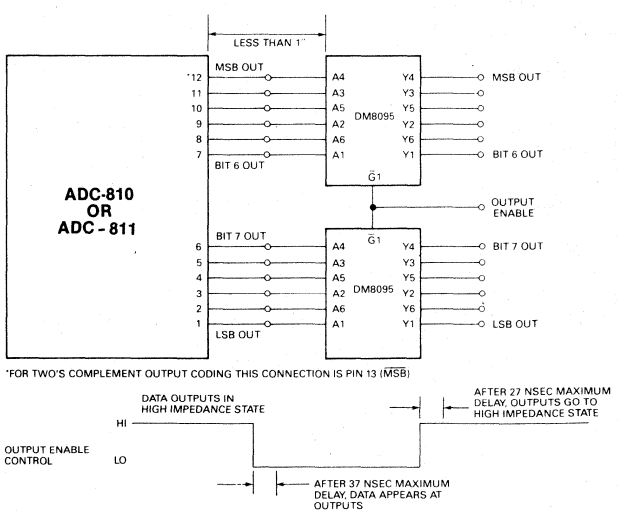
PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

GROUND PLANE LAYOUT

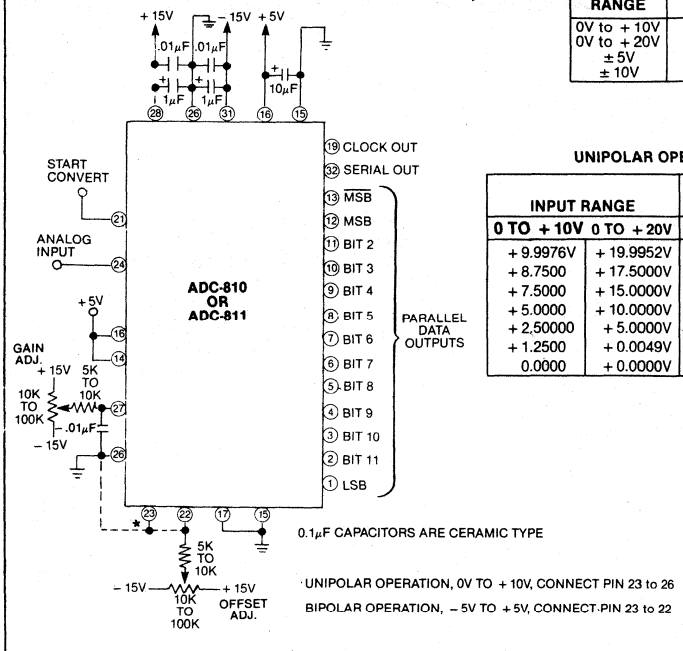


HIGH SPEED THREE-STATE OUTPUT BUFFER



TYPICAL CONNECTION AND APPLICATION

TYPICAL CONNECTIONS



INPUT CONNECTIONS

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0V to +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
0V to +20V	25	—	23 & 26	30	—	NA	NA
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 24

OUTPUT CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +20V	MSB		LSB
+9.9976V	+19.9952V	0000	0000	0000
+8.7500	+17.5000V	0001	1111	1111
+7.5000	+15.0000V	0011	1111	1111
+5.0000	+10.0000V	0111	1111	1111
+2.50000	+5.0000V	1011	1111	1111
+1.2500	+0.0049V	1111	1111	1110
0.0000	+0.0000V	1111	1111	1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE		COMP. OFFSET BINARY			COMP. TWO'S COMPLEMENT		
±10V	±5V	MSB		LSB	MSB		LSB
+9.9951V	+4.9976V	0000	0000	0000	1000	0000	0000
+7.5000	+3.7500	0001	1111	1111	1001	1111	1111
+5.500	+2.5000	0011	1111	1111	1011	1111	1111
0.0000	0.0000	0111	1111	1111	1111	1111	1111
-5.0000	-2.5000	1011	1111	1111	0011	1111	1111
-7.5000	-3.7500	1101	1111	1111	0101	1111	1111
-10.000	-5.0000	1111	1111	1111	0111	0000	0000

CALIBRATION TABLE

UNIPOLAR RANGE	+ ½ LSB	+ F.S.-1½ LSB
0 to +10V	+1.22 mV	+9.9963 V
0 to +20V	+2.44 mV	+19.9927V
BIPOLAR RANGE	**- ½ LSB**	**+ F.S.-1½ LSB**
±5V	-1.22 mV	+4.9963 V
±10V	-2.44 mV	+9.9927 V

For information on models with 0 to +5V and ±2.5V input voltage ranges please contact the factory.

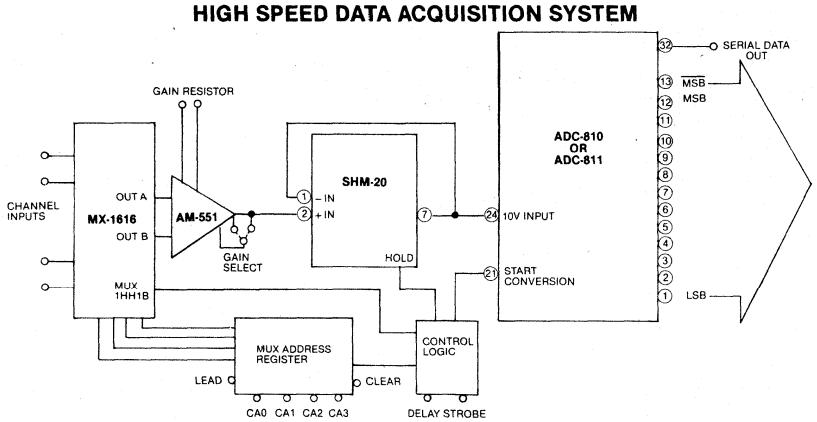
CALIBRATION PROCEDURE

1. **Connect the converter** as shown in the applicable connections diagram. A trigger pulse of 50 nsec minimum is applied to the start conversion input (pin 21) at a rate of 200 kHz.

2. **Zero and Offset Adjustments**
Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0 + ½ LSB) or the bipolar offset adjustment (0 - ½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.

3. **Full Scale Adjustment**
Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+ FS-1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

HIGH SPEED DATA ACQUISITION SYSTEM



The ADC-810/811 configured as shown with DATEL-INTERSIL's MX-1616, a high speed CMOS multiplexer, AM-551, a hybrid precision programmable gain instrumentation amplifier, and SHM-20, a 1 μS 0.01% monolithic sample-hold forms an 8 channel (differential), 12-bit, high speed data acquisition system capable of throughput rates in excess of 450 kHz.

Ultra-Fast 8 Bit A/D Converters ADC-815, ADC-825

FEATURES

- **8 Bits Resolution**
- **600 nsec. or 1 μsec. Conversion Time**
- **6 Input Ranges**
- **Parallel or Serial Outputs**
- **Logic-Controlled Bipolar Offset**
- **No Calibration Required**

GENERAL DESCRIPTION

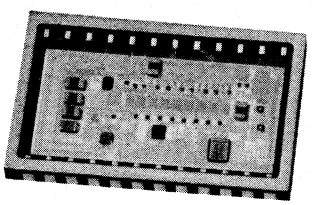
Datel-Intersil's ADC-815 and ADC-825 are very high speed 8 bit successive approximation A/D converters in miniature hybrid form. Both models have identical specifications except for conversion time. The ADC-825 has a maximum conversion time of 1 μsec., while the ultra-fast ADC-815 accomplishes an 8 bit conversion in only 600 nsec., maximum.

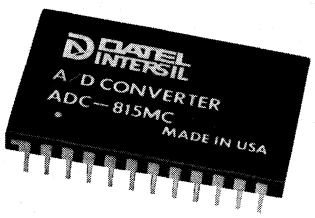
These converters feature six analog input voltage ranges: 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V and ±10V. Selection of input ranges is accomplished by simple external pin connection. Unipolar or bipolar operating mode is selected by a digital control applied to the bipolar offset input. Operation of these devices is further simplified by complete functional laser trimming, resulting in a factory-trimmed converter that requires no external adjustments.

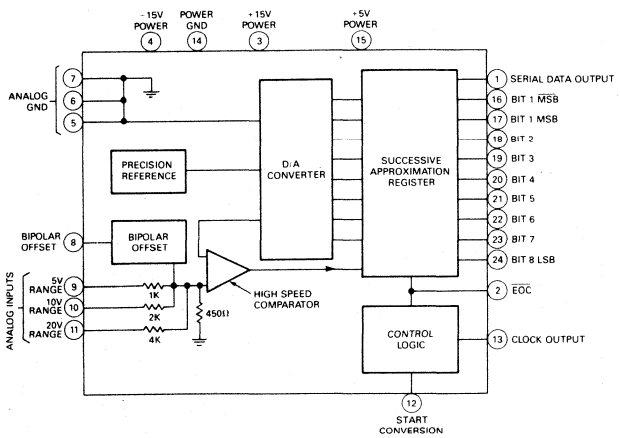
Each converter is a functionally complete unit requiring a minimum of passive external components for operation, and is packaged in a miniature, hermetically sealed 24-pin ceramic DIP.

Output data is available in parallel or serial form by external pin connection. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. Output coding in the parallel mode is accomplished by connection to either the MSB output or the $\overline{\text{MSB}}$ output. Serial output data is coded as straight binary for unipolar operation or offset binary for bipolar operation.

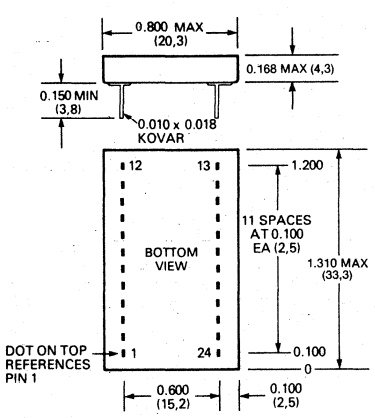
Additional specifications shared by both models include maximum nonlinearity of ±½ LSB, differential nonlinearity of ±½ LSB maximum, gain tempco of 20 ppm/°C maximum, power supply rejection of ±0.02%/% supply maximum, and long term stability of ±0.02%/year. Both models require ±15V and 5V supplies, and are available in different versions for operating temperature ranges of 0 to +70°C, −25 to +85°C, or −55 to +125°C.







MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL DATA OUTPUT	13	CLOCK OUTPUT
2	$\overline{\text{EOC}}$	14	POWER GROUND
3	+15V POWER IN	15	+5V POWER IN
4	−15V POWER IN	16	BIT 1 OUT ($\overline{\text{MSB}}$)
5	ANALOG GROUND	17	BIT 1 OUT (MSB)
6	ANALOG GROUND	18	BIT 2 OUT
7	ANALOG GROUND	19	BIT 3 OUT
8	BIPOLAR OFFSET	20	BIT 4 OUT
9	ANALOG INPUT, 5V RANGE	21	BIT 5 OUT
10	ANALOG INPUT, 10V RANGE	22	BIT 6 OUT
11	ANALOG INPUT, 20V RANGE	23	BIT 7 OUT
12	START CONVERSION	24	BIT 8 OUT (LSB)

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-815, ADC-825

Typical at 25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted.

	ADC-815	ADC-825
MAXIMUM RATINGS		
Positive Supply	+18V	
Negative Supply	−18V	
Logic Supply	+7V	
Digital Inputs	+5.5V	
Analog Inputs	±25V	
INPUTS		
Analog Input Ranges,[1] Unipolar	0 to +5V, 0 to +10V, 0 to +20V,	
Bipolar	±2.5V, ±5V, ±10V	
Input Impedance, 5V Range	1.34K	
10V Range	2.3K	
20V Range	4.27K	
Start Conversion	+2V min. to +5.5V max. Positive Pulse 50 nsec min. duration, 10 nsec. typ. rise and fall times. Positive Going Edge resets outputs to 011 . . . 1 and sets $\overline{EOC}$ HI. Negative going edge initiates conversion. Loading: 2 TTL loads.	
Bipolar Offset	Hold HI (+2.0V to +5V) for bipolar operation, hold LO ≤ +0.8V) for unipolar operation.	
OUTPUTS		
Parallel Output Data	9 parallel lines (8 binary bits plus $\overline{MSB}$) V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V Loading: 4 TTL loads	
Serial Output Data	NRZ format successive Decision pulse output at internal clock rate generated during conversion. MSB first. Loading: 4 TTL loads	
Coding, Unipolar	Straight Binary	
Bipolar	Offset Binary, Two's Complement	
$\overline{EOC}$	Conversion Status Signal. HI ≥ +2.4V during conversion and reset periods. LO ≤ +0.4V when conv. complete. Loading: 4 TTL loads	
Clock Output	Internal clock pulse train of negative going pulses[2] from +5V to 0V. Loading: 6 TTL loads	
PERFORMANCE		
Conversion Time[3], max.	700 nsec.	1 μsec.
Resolution	8 bits	
Nonlinearity	±½ LSB max.	
Differential Nonlinearity	±½ LSB max.	
Gain Error	±½ LSB max.	
Zero Error	±½ LSB max.	
Gain Tempco, 0°C to +70°C[4]	±20 ppm of FSR/°C max.[5]	
Zero Drift	±100 μV/°C max.	
Offset Tempco	±10 ppm of FSR/°C max.[5]	
Long Term Stability	±0.02% year	
No Missing Codes	Over Operating Temp. Range	
Power Supply Rejection, max,	±0.02%/% Supply	
POWER REQUIREMENT		
Analog Supply	+15V ±0.5V @ 35 mA max. −5V ±0.5V @ mA max.	
Logic Supply	+5V ±0.25V @ 100 mA max.	
Power Dissipation	1.25W max.	
PHYSICAL ENVIRONMENTAL		
Operating Temp. Range, MC	0°C to +70°C	
MR	−25°C to +85°C	
MM	−55°C to +125°C	
Storage Temp. Range	−65°C to +150°C	
Package Type	24 pin Ceramic DIP	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.2 oz. (6 g)	

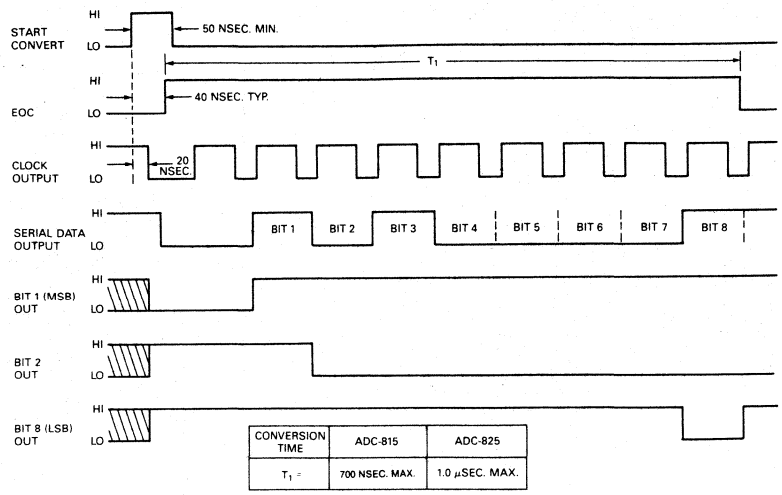
NOTES: 1. Unused analog inputs must be grounded.
2. At 15.9 MHz for the ADC-815, 9.52 MHz for the ADC-825.
3. The conversion time temperature coefficient for these converters is 0.15%/°C. This tempco is positive.
4. Doubles outside this temperature range.
5. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Use of a ground plane is particularly important with high speed data converters as it reduces high frequency noise and aids in decoupling analog signals from digital signals. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The basic configuration of the ground plane directly below the ADC-815 or ADC-825 is shown in the ground plane layout diagram. This layout should be modified after selection of analog input range to include unused analog inputs.
2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference. Unused analog inputs should be grounded.
3. **Applications of the ADC-815 and ADC-825 that require an input buffer amplifier may be satisfied by the use of DATEL-INTERSIL's AM-1435, an ultra fast hybrid device featuring a maximum settling time of 85 ms.**
4. Analog and digital supplies are internally bypassed to ground with .01 μF capacitors; however, it is recommended that the +15V, −15V and +5V supplies be additionally bypassed externally with 1 μF electrolytic capacitors as shown in the connection diagrams.
5. For bipolar operation the bipolar offset input (pin 8) is held at logic HI (+2.0V to +5V); for unipolar operation pin 8 is held at logic LO (0V to +0.8V).
6. In the bipolar mode, two's complement output coding is available by using the MSB output (pin 16); offset binary coding is obtained by using the MSB output (pin 17). Unipolar operation requires use of the MSB output (pin 17) to achieve straight binary output coding.
7. Serial output data is available at pin 1 in standard NRZ format with the MSB appearing first. Coding is straight binary for unipolar operation or offset binary for bipolar operation. Synchronization of serial output data is achieved by use of the clock output (pin 13). Each data bit is valid when the clock output is HIGH and appears in succession from the MSB at the second clock LOW to HIGH transition to the LSB at the ninth clock LOW to HIGH transition.
8. Applications of these converters that require the use of a sample-hold may be satisfied by Datel-Intersil's model SHM-HU, an ultra-fast hybrid unit featuring 25 nsec acquisition time and a ±2.5V input range.
9. These converters have a maximum power dissipation of 1.25W. The case-to-ambient thermal resistance for this package is approximately 33°C per watt. For operation in ambient temperatures exceeding 83°C, airflow of at least 400 linear feet per minute is recommended.

APPLICATIONS

TIMING DIAGRAM FOR ADC-815, ADC-825
OUTPUT: 10100001



CONVERSION TIME	ADC-815	ADC-825
T_1 =	700 NSEC. MAX.	1.0 μSEC. MAX.

CODING TABLES

UNIPOLAR OPERATION

UNIPOLAR SCALE	OUTPUT CODING* STRAIGHT BINARY	ANALOG INPUT 0 to +5V	0 to +10V	0 to +20V
F.S. - 1 LSB	1111 1111	+4.980V	+9.961V	+19.922V
¾ F.S.	1100 0000	+3.750V	+7.500V	+15.000V
½ F.S.	1000 0000	+2.500V	+5.000V	+10.000V
¼ F.S.	0100 0000	+1.250V	+2.500V	+5.000V
1 LSB	0000 0001	+0.020V	+0.039V	+0.078V
0	0000 0000	0.000V	0.000V	0.000V

*FOR PARALLEL OR SERIAL OUTPUT DATA

BIPOLAR OPERATION

BIPOLAR SCALE	OUTPUT CODING OFFSET BINARY[1]	OUTPUT CODING TWO'S COMPLEMENT[2]	INPUT VOLTAGE RANGE ±2.5V	±5V	±10V
+F.S.−1 LSB	1111 1111	0111 1111	+2.480V	+4.961V	+9.922V
+½ F.S.	1100 0000	0100 0000	+1.250V	+2.500V	+5.000V
+1 LSB	1000 0001	0000 0001	+0.020V	+0.039V	+0.078V
0	1000 0000	0000 0000	0.000V	0.000V	0.000V
−½ F.S.	0100 0000	1100 0000	−1.250V	−2.500V	−5.000V
−F.S.+1 LSB	0000 0001	1000 0001	−2.480V	−4.961V	+9.922V
−F.S.	0000 0000	1000 0000	−2.500V	−5.000V	+10.000V

NOTES: 1. FOR PARALLEL OR SERIAL OUTPUT DATA
2. FOR PARALLEL OUTPUT DATA ONLY

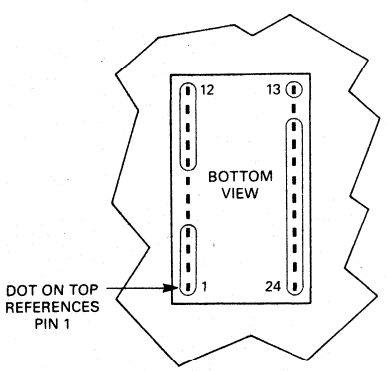
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
ADC-815MC	0°C to +70°C
ADC-815MR	−25°C to +85°C
ADC-815MM	−55°C to +125°C
ADC-825MC	0°C to +70°C
ADC-825MR	−25°C to +85°C
ADC-825MM	−55°C to +125°C

Mating Socket: DILS-3 (24-pin socket)
Trimming Potentiometers: TP-100

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

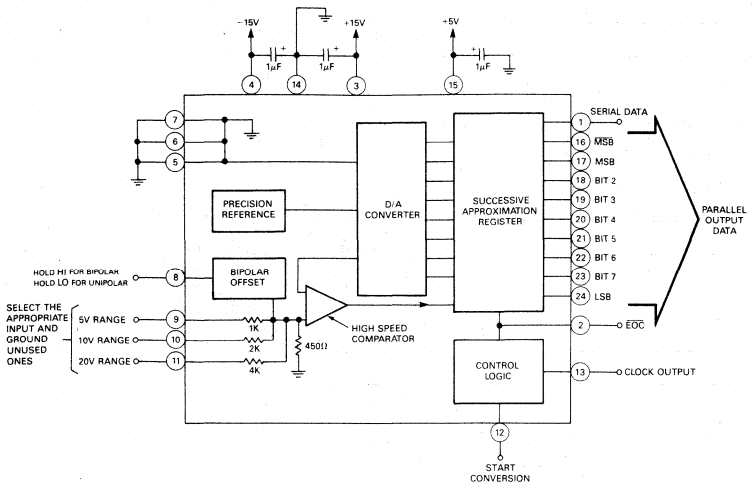
BASIC GROUND PLANE LAYOUT



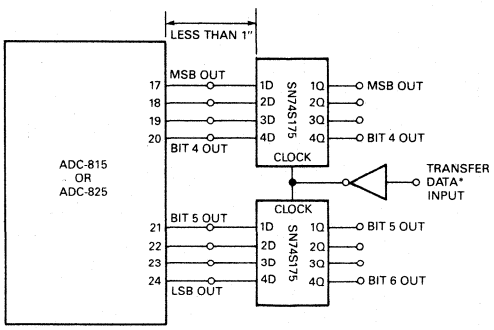
THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

CONNECTIONS

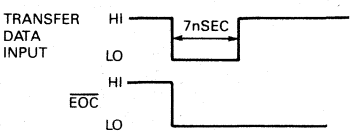
UNIPOLAR/BIPOLAR OPERATIONS



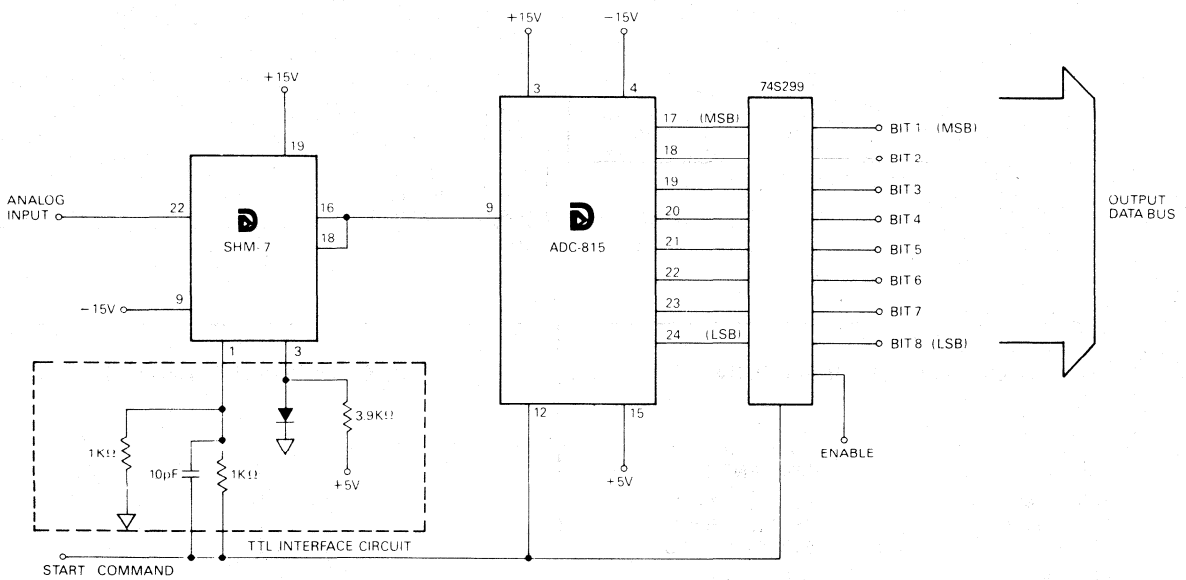
OUTPUT REGISTER



*TRANSFER DATA INPUT MAY BE TIED TO $\overline{EOC}$ OUTPUT (PIN 2) OR EXTERNALLY DRIVEN. WHEN TRANSFER DATA IS EXTERNALLY CONTROLLED TIMING OF CONTROL PULSE SHOULD BE AS SHOWN



HIGH SPEED DATA SYSTEM



A high speed data system using Datel-Intersil's ADC-815 and SHM-7, with an output register, to drive a data bus. The Start Command is a 60 nsec wide, TTL compatible, pulse with a maximum frequency of 1.5 MHz. Upon receipt of a start command, the SHM-7 will track the input voltage and the ADC-815 will reset. On the trailing edge of the start command, the SHM-7 will hold the input and the ADC-815 will begin its conversion. On the leading edge of the next start command, the output data will be clocked out of the output three-state register. The SHM-7 is a 40 nsec, 0.1% sample-hold amplifier. With this system, a ± 2.5V input step can be acquired to 0.1% accuracy in 40 nsec and held to within 80 μV while the A/D conversion takes place.

Ultra-Fast 10-Bit A/D Converters ADC-816, ADC-826

FEATURES

- **10 Bits Resolution**
- **800 nsec or 1.4 μsec Conversion Time**
- **6 Input Ranges**
- **Unipolar and Bipolar Operation**
- **Programmable Output Coding**

GENERAL DESCRIPTION

Datel-Intersil's ADC-816 and ADC-826 are very high speed 10 bit successive approximation A/D converters, realized as miniature thin-film hybrids. Both models have identical specifications except for conversion time. The ADC-826 has a maximum conversion time of 1.4 μsec. The ultra-fast ADC-816 offers a maximum conversion time of only 800 nsec, making this the fastest 10 bit A/D converter of any hybrid, monolithic, or modular unit currently available. Please note that these conversion times are specified as maximum at *full rated operating temperature!*

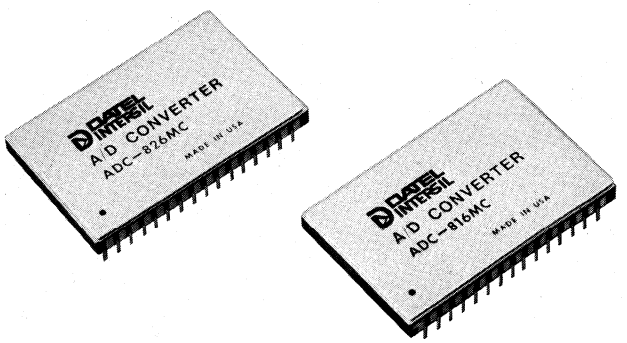
These converters feature six analog input voltage ranges: 0 to −5V, 0 to −10V, 0 to −20V, ±2.5V, ±5V and ±10V. Selection of input range is accomplished by simple external pin connection.

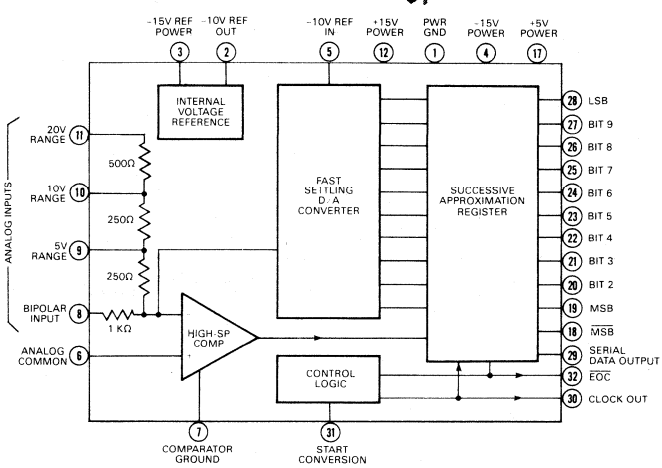
Output data is available in parallel or serial form by external connection. Data is coded as straight binary for unipolar operation and as either offset binary or Two's complement for bipolar operation. Two's complement is available in the parallel output mode only and is selected by pin connection.

Specifications shared by both models include maximum nonlinearity of ±½ LSB and differential nonlinearity of ±½ LSB maximum.

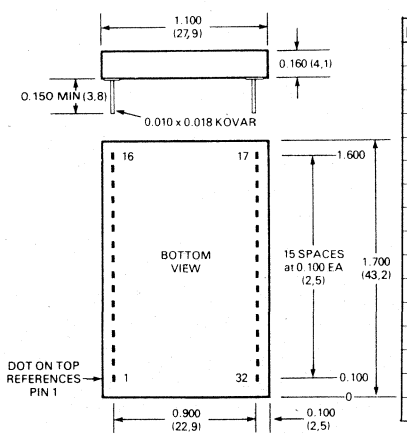
These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a high speed comparator, an ultra-fast settling D/A converter, a precision voltage reference, successive approximation register, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a miniature hermetically sealed 32 pin ceramic DIP package.

Both models require ±15 VDC and +5V supplies, and are available in versions for the 0 to 70°C, −25 to +85°C or −55 to +125°C operating temperature ranges. For information on versions certified to MIL-STD-883 Class B, contact the factory.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER COM	17	+5V POWER
2	REF OUT	18	$\overline{\text{MSB}}$ 1
3	REF POWER	19	MSB 1
4	−15V POWER	20	BIT 2
5	REF IN	21	BIT 3
6	SIG COM	22	BIT 4
7	COMPARATOR COM	23	BIT 5
8	BIP IN	24	BIT 6
9	+5V IN	25	BIT 7
10	+10V IN	26	BIT 8
11	+20V IN	27	BIT 9
12	+15V POWER	28	LSB 10
13	NC	29	SERIAL DATA OUT
14	NC	30	CLOCK OUT
15	NC	31	START
16	NC	32	$\overline{\text{EOC}}$

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617)339-9341/TWX710-346-1453/TLX951340

SPECIFICATIONS ADC-816, ADC-826
(Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted)

MAXIMUM RATINGS

Positive Supply, pin 12	+16VDC
Negative Supply, pin 4	−16 VDC
Logic Supply, pin 17	+7 VDC
Logic Inputs	+7 VDC
Analog Inputs	± Twice selected analog input range

INPUTS

Analog Input Ranges	**unipolar**[1]	0 to −5V, 0 to −10V, 0 to −20V
	bipolar	±2.5V, ±5V, ±10V
	reference	−9.5V to −10.5V
Input Impedance[2]	**5V range**	250Ω
	10V range	500Ω
	20 V range	1 KΩ
	bipolar input	1 KΩ
	reference (pin 5)	2 KΩ
Start conversion		2V min to 5.5V max. positive pulse with duration of 25 nsec min. Rise and fall times typ. 10 nsec. Logic "1" resets converter. Logic "0" initiates conversion. Loading: 1 TTL Load.

OUTPUTS

Parallel Output Data		11 Parallel lines of data (10 binary bits + $\overline{\text{MSB}}$) held until next conversion command. Vout ("0") ≤ +0.4V, Vout ("1") ≥ +2.4V. Loading: 2 TTL loads
Coding[3] **, unipolar**		Straight Binary
bipolar[4]		Offset Binary, Two's Complement
Serial Output Data		NRZ successive decision pulses out, MSB first, at internal clock frequency Loading: 4 TTL Loads.
End of Conversion ($\overline{\text{EOC}}$)		Conversion Status Signal. Output is logic HI during reset and conversion, LO when conversion is complete. Loading: 4 TTL Loads.
Clock Output		Train of positive going, 0 to +5V, 30 nsec pulses.
Clock Frequency	**ADC-816MC/MR**[5]	14.6 MHz
	ADC-826MC/MR/MM	8.1 MHz
Reference Output, Voltage		−10.00V ± 0.02V
Current		0 to +20 mA (sink only)
Impedance		10 Ω max. fo ≤ 10 MHz

PERFORMANCE

Resolution		10 Bits
Conversion Time[6] **, ADC-816MC/MR**[7]		800 nsec max.
ADC-826MC/MR/MM		1.4 μsec max.
Nonlinearity		±½ LSB max.
Differential Nonlinearity[8]		±½ LSB max.
Gain Error[9]**, before adjustment, unipolar**		±0.3% of FSR[10], max.
bipolar		±0.2% of FSR max.
Zero Error, before adjustment, unipolar		±0.2% of FSR max.
Offset Error, before adjustment, bipolar		±0.1% of FSR max.
Gain Tempco[11]**, unipolar**		±37 ppm/°C max.
bipolar		±28 ppm/°C max.
Zero Tempco , unipolar		±12 ppm/°C max.
bipolar		±23 ppm/°C max.
Conversion Time Tempco		±0.1%/°C
Reference Output Tempco		±20 ppm/°C max.
Power Supply Rejection		Effectively infinite for rated supplies
No missing codes		Over operating Temp. Range

POWER REQUIREMENTS

Analog Supply , pin 12	+15V ±0.1V @ 106mA, max.
pin 4	−15V ±0.5V @ 20mA max.
Reference Supply, pin 3	−15V ±0.5V @ 34mA max.
Logic Supply, pin 17	+5V ±0.25V @ 194mA max.
Power Dissipation	3.6W max.

PHYSICAL-ENVIRONMENTAL

Operating Temp Range	**Suffix C**	0°C to +70°C
	Suffix R	−25°C to +85°C
	Suffix M	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Package Type		32 pin hermetically sealed Ceramic DIP
Pins		0.010 × 0.018 inch gold plated Kovar
Weight		0.8 oz (23g)

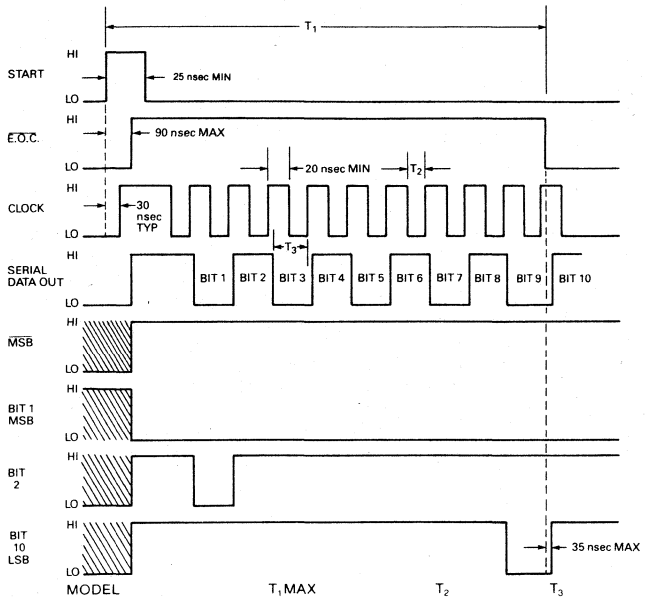
NOTES: 1. Bipolar input must be tied to ground.
2. Resistance tolerance is −30%, +50%, ±50 ppm/°C.
3. All coding is inverted analog.
4. Two's Complement Binary available for parallel output only.
5. Clock frequency for ADC-816MM is 12.1 MHz
6. Max. conversion time is specified at full rated operating temp.
7. The ADC-816MM has a maximum conversion time of 975 nsec at full rated operating temperature.
8. Tested over full rated operating temperature range.
9. Includes Zero Error.
10. FSR is Full Scale Range.
11. Includes internal reference Tempco. Given as a maximum for 5V FSR, these values improve by 10% for 10V FSR, and by 20% for 20V FSR.

TECHNICAL NOTES

1. Use of good high frequency circuit board layout techniques is required for rated performance. The power common (pin 1), comparator common (pin 7), and signal common (pin 6) are not connected internally, and therefore must be connected externally as directly as possible, through a low resistance, low inductance path. The extensive use of a ground plane for all common connections is highly recommended. Also, it is recommended that the analog and digital supplies, although they are internally bypassed with 0.033 μF capacitors, be additionally bypassed externally at the supply pins with 1 μF electrolytic capacitors.
2. The digital outputs are not buffered from their internal application and so are sensitive to unusual loading or long lines. Terminate these outputs with normal TTL inputs not more than 3 inches from the data output pin. Analog inputs must be non-reactive such that leads should be short and purely resistive. The reactive component of any analog input source, as seen at the analog input pin, should be less than 0.3% of the analog input resistance at that pin, for frequencies below 20 MHz.
3. Conversion time is measured from the rising edge of a 50 nsec start input pulse to the falling edge of the $\overline{\text{EOC}}$ output. The conversion time is factory set at +25°C for the ADC-816 MC/MR at 750 nsec, 875 nsec for the ADC-816MM, and 1.25 μsec for the ADC-826MC/MR/MM. The worst case conversion time at the maximum rated operating temperature is given as a maximum specification.
4. To use the internal reference the reference supply pin (pin 3) must be connected to the −15V supply. If the reference supply pin (pin 3) is disconnected or grounded, the internal reference will be disabled at a power saving of approximately 200 mW.
5. Serial output data is available in NRZ format successive decision pulses, MSB first, in straight binary or offset binary coding. Synchronization of the serial output data is achieved through the use of the clock output (pin 30). This same clock output also controls the output register such that at the rising edge of the output clock the previous data bit may be clocked out, however, there will be no clock edge to clock out the LSB. A Serial DATA Recovery circuit is diagrammed on the applications page that will correct this.
6. These converters have a case to ambient thermal resistance of 22°C per watt. At temperatures above +70°C an air flow of at least 400 linear feet per minute is recommended. To operate at elevated temperatures it is recommended that the converter be mounted directly to the circuit board (without the use of a mounting socket) and that good thermal contact be established between the case bottom and the circuit board ground plane by use of a silicone thermal joint compound such as Wakefield Type 120 or equivalent.
7. Applications of these converters that require the use of a sample-hold may be satisfied by Datel-Intersil's model SHM-HU, an ultra-fast hybrid unit featuring 25 nsec acquisition time and a ±2.5V input range.

APPLICATIONS

TIMING DIAGRAM FOR ADC-816, ADC-826



MODEL	T_1 MAX	T_2	T_3
ADC-816 MC/MR	800 n sec	44 n sec	23-64 n sec
ADC-816 MM	975 n sec	58 n sec	37-73 n sec
ADC-826 MC/MR/MM	1.4 μ sec	100 n sec	79-114 n sec

CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE			STRAIGHT BINARY		
0 to -20V	0 to -10V	0 to -5V	MSB		LSB
-19.9805	-9.9902	-4.9951	1111	11	1111
-17.5000	-8.7500	-4.3750	1110	00	0000
-15.0000	-7.5000	-3.7500	1100	00	0000
-10.0000	-5.0000	-2.5000	1000	00	0000
-5.0000	-2.5000	-1.2500	0100	00	0000
-2.5000	-1.2500	-0.6250	0010	00	0000
-0.0198	-0.0098	-0.0049	0000	00	0001
0.0000	0.0000	0.0000	0000	00	0000

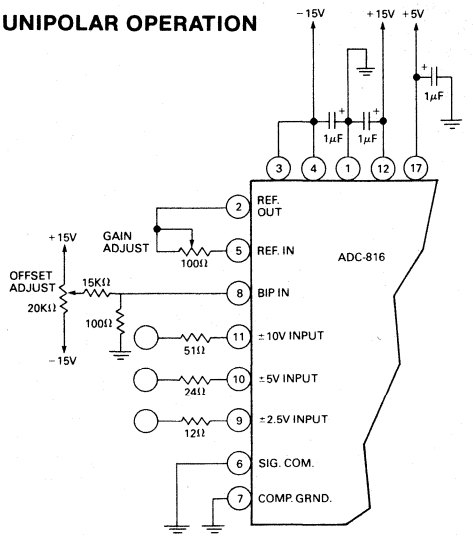
BINARY OPERATION

INPUT RANGE			OFFSET BINARY			TWO'S COMPLEMENT		
±10V	±5V	±2.5V	MSB		LSB	MSB		LSB
-9.9805	-4.9902	-2.4951	1111	11	1111	0111	11	1111
-7.5000	-3.7500	-1.8750	1110	00	0000	0110	00	0000
-5.0000	-2.5000	-1.2500	1100	00	0000	0100	00	0000
0.0000	0.0000	0.0000	1000	00	0000	0000	00	0000
+5.0000	+2.5000	+1.2500	0100	00	0000	1100	00	0000
+7.5000	+3.7500	+1.8750	0010	00	0000	1010	00	0000
+9.9805	+4.9902	+2.4951	0000	00	0001	1000	00	0001
+10.0000	+5.0000	+2.5000	0000	00	0000	1000	00	0000

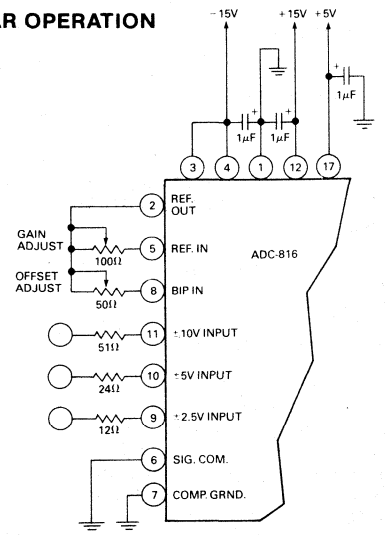
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
ADC-816MC	0°C To +70°C	
ADC-816MR	-25°C To +85°C	
ADC-816MM	-55°C To +125°C	
ADC-826MC	0°C To +70°C	
ADC-826MR	-25°C To +85°C	
ADC-826MM	-55°C To +125°C	
Mating Socket	DILS-2 (2/converter)	
Trimming Potentiometers	TP20K, TP100, TP50	

UNIPOLAR OPERATION



BIPOLAR OPERATION



CALIBRATION PROCEDURE

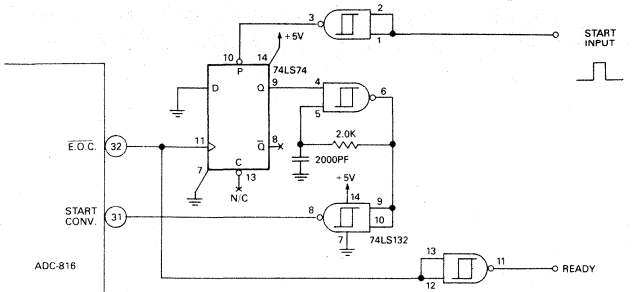
1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of between 50 nsec and 100 nsec is applied to the start conversion input (pin 31) at the rate of 200KHz.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0-1/2 LSB) or the bipolar offset adjustment (+FS-1/2 LSB). Adjust the appropriate trimming potentiometer so that the output code flickers equally between X0000 00000 and X0000 00001. The MSB, indicated by X will be 0 for straight binary and offset binary coding or 1 for two's complement output coding.
3. **Full Scale Adjustment**
   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (-FS + 1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X1111 11111 and X1111 11110. The MSB, indicated by X, will be 1 for straight binary and offset binary coding or coding or 0 for two's complement output coding.

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 To 5V	Zero	2.4mV
	Gain	4.9927V
0 To 10V	Zero	4.9mV
	Gain	9.9854V
0 to 20V	Zero	9.8mV
	Gain	19.9707 V

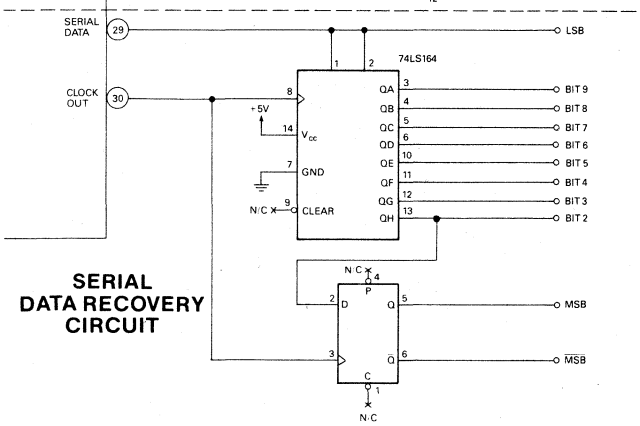
BIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
±2.5V	Offset	+2.4975V
	Gain	2.4927V
±5V	Offset	+4.9951V
	Gain	4.9854V
±10V	Offset	+9.9902V
	Gain	9.9707V

PERFORMANCE DATA

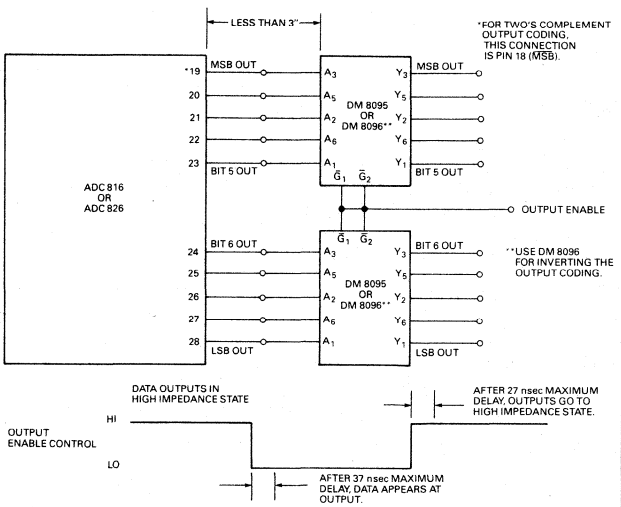
UNCONDITIONAL/START CIRCUIT



SERIAL DATA RECOVERY CIRCUIT



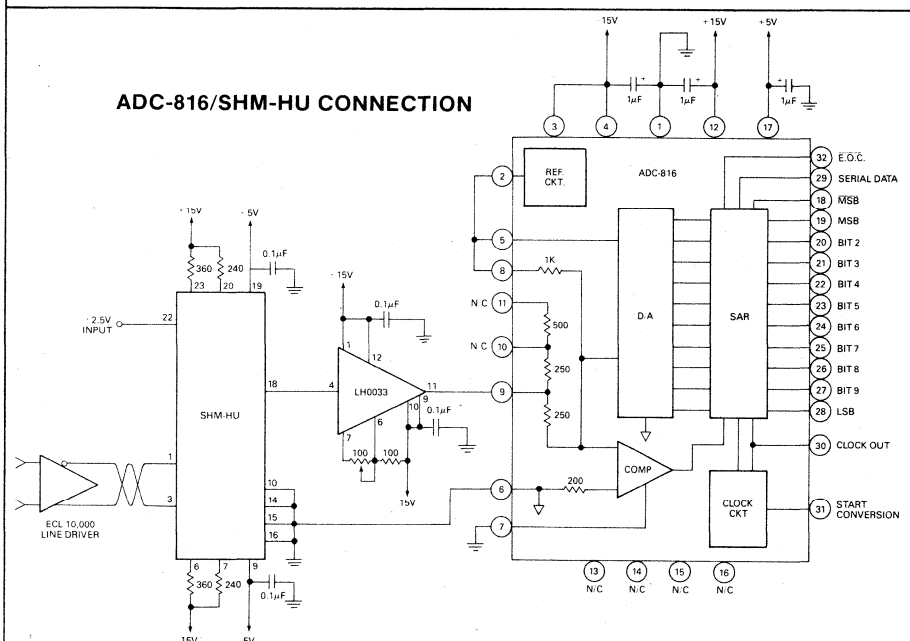
HIGH SPEED THREE-STATE OUTPUT BUFFER



The Unconditional Start Circuit, shown for the ADC-816/826 insures the initiation of a conversion cycle upon the application of one start pulse of 40 nsec minimum pulse width regardless of converter status.

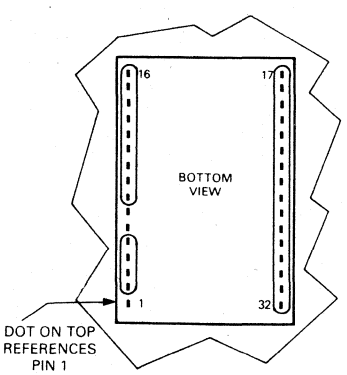
The serial data output of the ADC-816/826 is converted into parallel form, with the addition of an $\overline{MSB}$ output, by the Serial Data Recovery circuit. Users should refer to technical note No. 2 on the loading of the ADC-816/826 digital outputs when using these circuits.

ADC-816/SHM-HU CONNECTION



When the ADC-816 or ADC-826 is configured as shown here with Datel-Intersil's SHM-HU hybrid sample-hold, a ±2.5V input step can be acquired to 0.1% accuracy in 30 nsec and held to within 40 μV while the A/D conversion takes place. Use of the SHM-HU reduces the time over which the input signal is averaged to a few nanoseconds (an A/D converter without a sample-hold averages the analog input signal over the total conversion time of the A/D).

GROUND PLANE LAYOUT



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

Ultra-Fast 12 Bit A/D Converters ADC-817, ADC-827

FEATURES

- **12 Bit Resolution**
- **2 μsec or 3 μsec Conversion Times**
- **Unipolar & Bipolar Operation**
- **Short Cycle Operating Capability**
- **6 Programmable Input Ranges**
- **Parallel or Serial Data Output**

GENERAL DESCRIPTION

The ADC-817 and ADC-827 are high-speed successive approximation A/D converters in miniature hybrid form. Both Models have identical specifications except for conversion times. The ADC-827 has a maximum conversion time of 3 μsec while the ultra-fast ADC-817 accomplishes a 12 bit conversion in only 2.0 μsec., maximum.

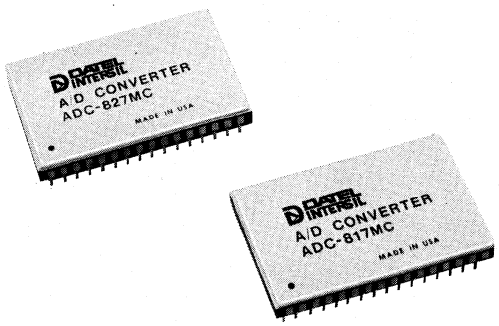
These converters feature six analog input voltage ranges: 0 to −5V, 0 to −10V, 0 to −20V, ±2.5V, ±5V, and ±10V. Selection of input range is accomplished by simple external pin connection. Both devices provide a user-selectable, fast settling precision input buffer with an input impedance of 100 MΩ, allowing them to be driven directly from a high impedance source. The input buffer may be bypassed for maximum speed applications with low impedance sources such as a sample and hold.

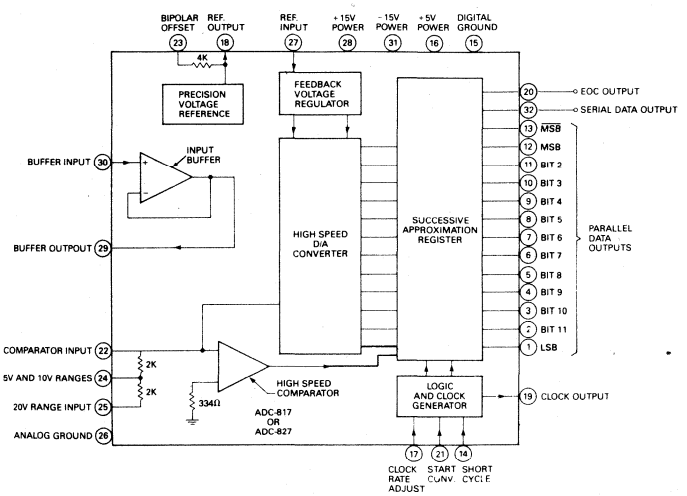
Output data is available in parallel or serial form by external connection. Data is coded as straight binary for unipolar operation and as either offset binary or two's complement for bipolar operation. Two's complement coding is available in the parallel output mode only, and is selected by pin connection.

Specifications shared by both models include maximum nonlinearity of ±1/2 LSB, differential nonlinearity of ±1/2 LSB maximum, gain tempco of 25 ppm/°C maximum, and a power supply rejection of ±0.01%/% supply maximum.

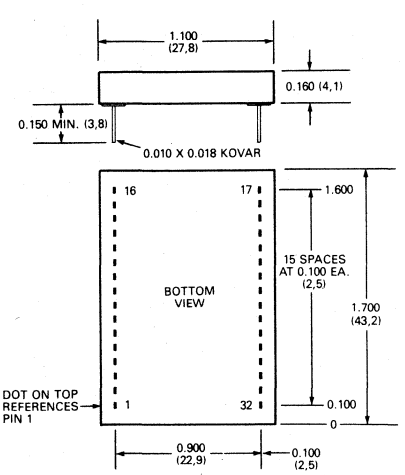
These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a fast settling precision input buffer, a high speed comparator, an ultra-fast settling D/A converter, a precision voltage reference, successive approximation register, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a miniature, hermetically sealed 32 pin ceramic DIP package.

Both models require ±15 VDC and +5V supplies, and are available in versions for the 0 to +70° C, −25 to +85° C or −25 to +125° C operating temperature ranges. For information on versions certified to MIL-STD-883 Class B, contact the factory.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STAND OFF FROM CASE

ADC-817, 827 INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REFERENCE OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	EOC OUT
5	BIT 8 OUT	21	START CONVERSION
6	BIT 7 OUT	22	COMPARATOR IN
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT RANGE
9	BIT 4 OUT	25	20V INPUT RANGE
10	BIT 3 OUT	26	ANALOG GROUND
11	BIT 2 OUT	27	REFERENCE INPUT
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT (MSB)	29	BUFFER OUT
14	SHORT CYCLE	30	BUFFER IN
15	DIGITAL GROUND	31	−15V POWER
16	+5V POWER	32	SERIAL OUT

DATEL-INTERSIL, 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-817, ADC-827

Typical at 25° C, ±15V supplies, unless otherwise noted.

	ADC-817	ADC-827
MAXIMUM RATINGS		
Positive Supply	+18V	
Negative Supply	−18V	
Logic Supply	+7V	
Digital Inputs	+5.5V	
Analog Inputs	±20V	
Buffer Amplifier Input	±15V	
INPUTS		
Analog Input Ranges Unipolar	0 to −5V, 0 to −10V, 0 to −20V	
Bipolar	±2.5V, ±5V, ±10V	
Input Impedance 5V Ranges	1 KΩ	
10V Ranges	2 KΩ	
20V Ranges	4 KΩ	
Start Conversion	+2V min. to +5.5V max. Positive Pulse 50 nsec. min. Logic "1" resets converter	
Buffer Amplifier Gain	+1	
Buffer Amplifier Input Voltage	±10.0V	
Buffer Amplifier Input Impedance	100 MΩ	
Buffer Amplifier Settling Time[1]	500 nsec. max.	
OUTPUTS		
Parallel Output Data	13 parallel lines (12 binary bits plus $\overline{MSB}$) valid from negative going edge of EOC pulse to positive going edge of START CONVERSION pulse. V_{OUT} "0" ≤ +0.4V V_{OUT} "1" ≥ +2.4V Loading: 4 TTL loads	
Serial Output Data	NRZ format, successive decision pulse output at internal clock rate generated during conversion. MSB first. Loading: 6 TTL loads	
Coding, Unipolar[2]	Straight Binary	
Bipolar[3]	Offset Binary, Two's Complement[3]	
End of Conversion (EOC)	Conversion Status Signal: 10 TTL Loads V_{OUT} "0" ≤ +0.4V for conversion complete V_{OUT} "1" ≥ +2.4V for conversion in progress	
Clock Output	Negative going pulses from +5V to 0V, gated on during conversion Loading: 6 TTL loads	
PERFORMANCE		
Resolution	12 binary bits[4]	
Nonlinearity[5]	±1/2 LSB max.	
Differential Nonlinearity[5]	±1/2 LSB max.	
Diff. Nonlinearity Tempco	±5 ppm/° C max.	
Monotonicity	Guaranteed over operating temp	
Gain Tempco[6]	±25 ppm/° C max.	
Zero Tempco, Unipolar	±150 μV/° C max.	
Offset Tempco, Biopolar[6]	±15 ppm of FSR/°C max.[7]	
Power Supply Rejection	±0.01%/% Supply, max.	
Conversion Time Over Full Temp.	2.0 μsec max.	3.0 μsec max.
POWER REQUIREMENT		
Supply Voltage	+15V ±0.5V @ 55 mA max. −15V ±0.5V @ 30 mA max. + 5V ±0.25V @ 180 mA max.	
Power Dissipation	2.2 W max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range, MC	0° C to +70° C	
MR	−25° C to +85° C	
MM	−55° C to +125° C	
Storage Temp. Range	−65° C to +125° C	
Package Type	32 pin hermetically sealed ceramic DIP	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.42 oz. (12g)	

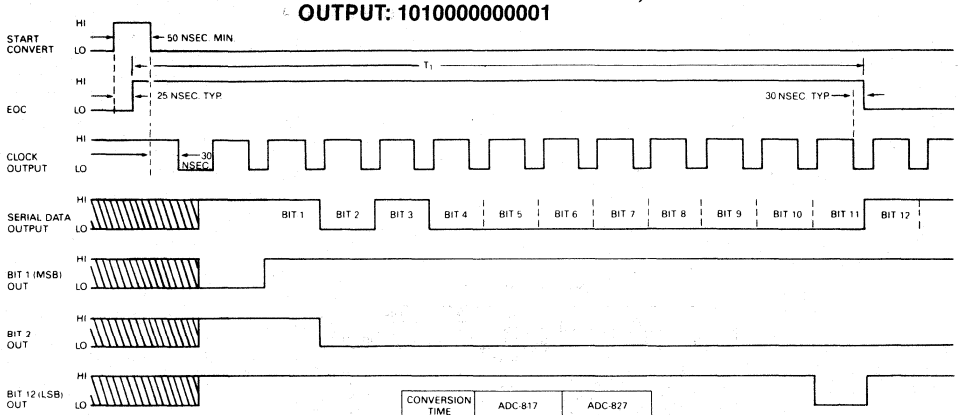
NOTES:
1. 10V step to 0.01%, 5V and 20V steps settle to 0.01% in 150 nsec and 800 nsec, respectively.
2. These converters operate with inverted analog, that is F.S. + 1LSB is encoded as 1111 1111 1111 and + FS is encoded as 0000 0000 0000 (examples given are for offset binary coding).
3. Parallel output data only is available in offset binary (uses MSB out) of two's complement coding (uses $\overline{MSB}$ out).
4. May be reduced by connection of short cycle input as shown in the Short Cycle Operation table.
5. For 0 to −10V and ±10V input voltage ranges. For guaranteed linearity specifications at other input voltage ranges see ordering information.
6. For 0°C to +70°C operation, these values double outside of this temp. range.
7. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Ground loop problems are avoided by connecting all grounds on the board to the ground plane.
2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference.
3. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between input level change, such as multiplexer channel change, and the negative going edge of the START CONVERSION pulse. If the buffer is not required its input (pin 30) should be tied to analog ground (pin 26). This will prevent the unused amplifier from introducing noise into the converter. For applications in which the internal buffer is not used, the converter must be driven from a source with an extremely low input impedance.
4. Both analog and digital supplies should be bypassed to ground with 1 μF electrolytic capacitors in parallel with 0.1 μF ceramic capacitors as shown in the connections diagrams. Bypass capacitors should be located directly adjacent to, or on, each supply pin. The −10V reference output (pin 18) should be bypassed to ground with a 2.2 μF electrolytic capacitor mounted as previously indicated.
5. In the bipolar mode, two's complement output coding is available by using the $\overline{MSB}$ output (pin 13); offset binary coding is obtained by using the MSB output (pin 12). Unipolar operation requires use of the MSB output (pin 12) to achieve straight binary output coding.
6. Serial output data is available at pin 32 in standard NRZ format with the MSB appearing first. Coding is straight binary for unipolar operation or offset binary for bipolar operation. Synchronization of serial output data is achieved by use of the clock output (pin 19). Each data bit is valid when the clock output is HIGH and appears in succession from the MSB at the second clock LOW to HIGH transition to the LSB at the thirteenth clock LOW to HIGH transition.
7. Applications of these converters that require the use of a sample-hold may be satisfied by Datel-Intersil's model SHM-6, a high-speed hybrid unit featuring 1.0 μsec acquisition time, 0.01% accuracy, programmable gains from ±1 to ±10 and a ±10V output range.
8. These converters have a maximum power dissipation of 2.2W. The case-to-ambient thermal resistance for this package is approximately 28° C per watt. For operation in ambient temperatures exceeding 70° C, care must be taken to ensure free air circulation in the vicinity of the converter.
9. Clock rate control (pin 17) is left unconnected for operation at rated conversion speed. Connect to +5V to decrease conversion time by 25-30 nsec, or to ground to increase conversion time by 25-30 nsec.

APPLICATIONS

TIMING DIAGRAM FOR ADC-817, ADC-827
OUTPUT: 1010000000001



CONVERSION TIME	ADC-817	ADC-827
T_1	2.0μSEC. MAX.	3.0μSEC. MAX.

OUTPUT CODING

UNIPOLAR SCALE	UNIPOLAR ANALOG INPUT -20V RANGE	-10V RANGE	-5V RANGE	STRAIGHT BINARY OUTPUT CODE
+FS + 1 LSB	−19.9952V	−9.9976V	−4.9988V	1111 1111 1111
+ 7/8 FS	−17.5000V	−8.7500V	−4.3750V	1110 0000 0000
+ 3/4 FS	−15.0000V	−7.5000V	−3.7500V	1100 0000 0000
+ 1/2 FS	−10.0000V	−5.0000V	−2.5000V	1000 0000 0000
+ 1/4 FS	−5.0000V	−2.5000V	−1.2500V	0100 0000 0000
+1 LSB	−0.0049V	−0.0024V	−0.0012V	0000 0000 0001
0	−0.0000V	0.0000V	0.0000V	0000 0000 0000

BIPOLAR SCALE	ANALOG INPUT ±10V RANGE	±5V RANGE	±2.5V RANGE	DATA OUTPUT CODING OFFSET BINARY	TWO's COMPLEMENT
+FS + 1 LSB	−9.9951V	−4.9976V	−2.4988V	1111 1111 1111	0111 1111 1111
+ 1/2 FS	−4.5000V	−2.5000V	−1.2500V	1100 0000 0000	0100 0000 0000
+1 LSB	−0.0049V	−0.0024V	−0.0012V	1000 0000 0001	0000 0000 0001
0	0.0000V	0.0000V	0.0000V	1000 0000 0000	0000 0000 0000
+ 1 LSB	+0.0049V	+0.0024V	+0.0012V	0111 1111 1111	1111 1111 1111
+ 1/2 FS	+4.5000V	+2.5000V	+1.2500V	0100 0000 0000	1100 0000 0000
+ FS − 1 LSB	+9.9951V	+4.9976V	+2.4988V	0000 0000 0001	1000 0000 0001
+FS	+10.0000V	+5.0000V	+2.5000V	0000 0000 0000	1000 0000 0000

SHORT CYCLE OPERATION

CONNECTION RES. (BITS)	PIN 14 TO	CONVERSION TIME ADC-817	ADC-827
1	PIN 11	300 nsec	462 nsec
2	PIN 10	462 nsec	693 nsec
3	PIN 9	615 nsec	923 nsec
4	PIN 8	770 nsec	1.15 μsec
5	PIN 7	923 nsec	1.38 μsec
6	PIN 6	1.07 μsec	1.62 μsec
7	PIN 5	1.23 μsec	1.85 μsec
8	PIN 4	1.38 μsec	2.08 μsec
9	PIN 3	1.54 μsec	2.31 μsec
10	PIN 2	1.69 μsec	2.54 μsec
11	PIN 1	1.85 μsec	2.77 μsec
12	+5V	2.0 μsec	3.0 μsec

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
ADC-817MC	0 to +70° C	
ADC-817MR	−25 to +85° C	
ADC-817MM	−55 to +125° C	
ADC-827MC	0 to +70° C	
ADC-827MR	−25 to +85° C	
ADC-827MM	−55 to +125° C	

Mating Socket: DILS-2 (2 Required Per Converter)

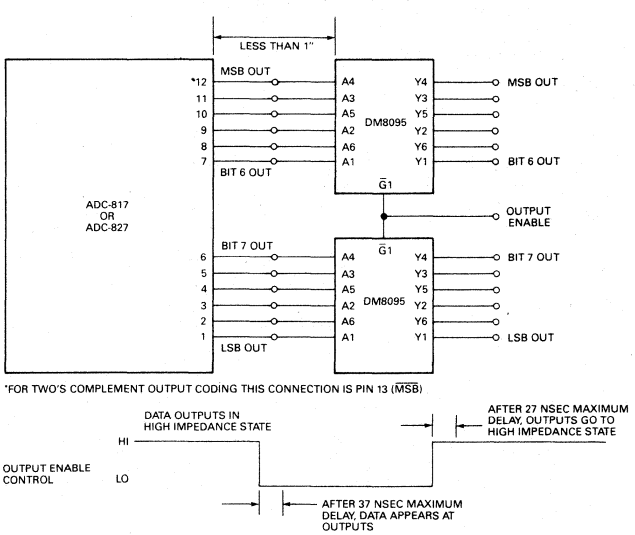
Trimming Potentiometer: TP-100

For guaranteed ± ½ LSB linearity specifications with 0 to −5V, ± 2.5V, or ±5V input voltage ranges add the following suffixes to the part number.

Input range	Suffix
0 to −5V	-7738
±2.5V	-7739
±5V	-7740

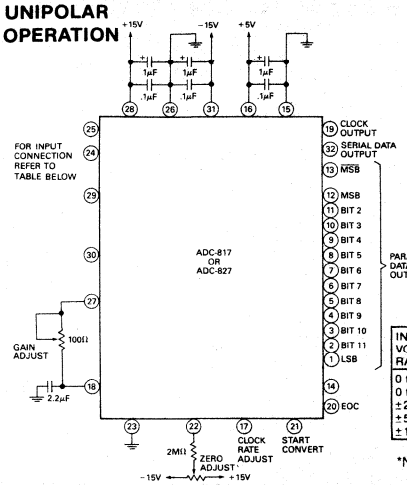
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

HIGH SPEED THREE-STATE OUTPUT BUFFER

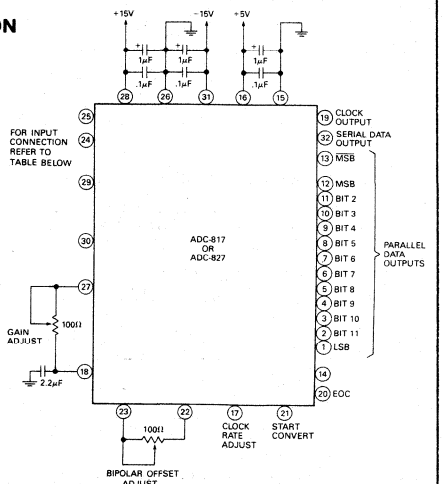


CONNECTIONS AND CALIBRATION

UNIPOLAR OPERATION



BIPOLAR OPERATION



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	* WITH INPUT BUFFER			WITHOUT INPUT BUFFER		
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER	
0 to −5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
0 to −10V	30	29 to 24	—	24	—	30 to 26
±2.5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
±5V	30	29 to 24	—	24	—	30 to 26
±10V	30	29 to 25	—	25	—	30 to 26

*NOTE: FOR 0 TO -20V RANGE INPUT BUFFER MAY NOT BE USED. ANALOG INPUT IS PIN 25

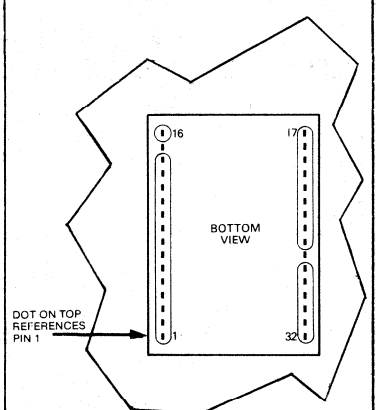
CALIBRATION PROCEDURE

1. **Connect the converter** as shown in the applicable connections diagram. A trigger pulse of 50 nsec minimum is applied to the start conversion input (pin 21) at a rate of 200 kHz.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0−1/2 LSB) or the bipolar offset adjustment (+FS −LSB). Adjust the appropriate trimming potentiometer so that the output code flickers equally between X000 0000 0000 and X000 0000 0001. The MSB, indicated by X, will be 0 for straight binary and offset binary output coding, or 1 for two's complement output coding.
3. **Full Scale Adjustment**
   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (−FS, +1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X111 1111 1111 and X111 1111 1110. The MSB, indicated by X, will be 1 for straight binary and offset binary output coding, or 0 for two's complement output coding.

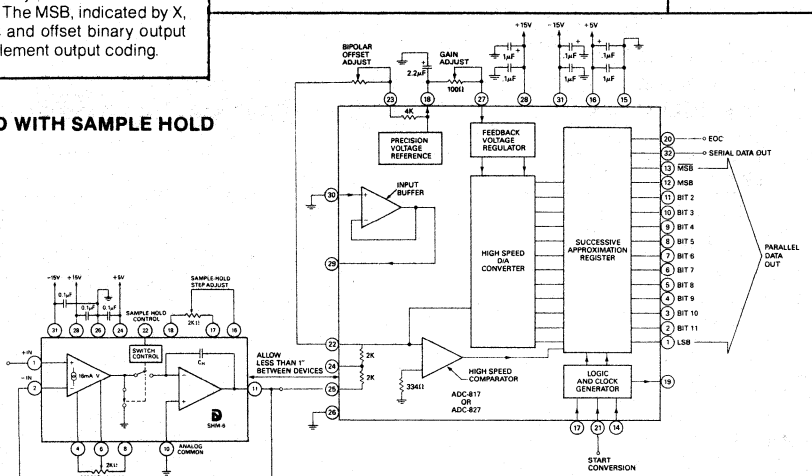
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO −5V	ZERO	−0.6 mV
	GAIN	−4.9982V
0 TO −10V	ZERO	−1.2 mV
	GAIN	−9.9963V
0 TO −20V	ZERO	−2.44mV
	GAIN	−19.9927V
BIPOLAR RANGE		
±2.5V	OFFSET	+2.4994V
	GAIN	−2.4982V
±5V	OFFSET	+4.9988V
	GAIN	−4.9963V
±10V	OFFSET	+9.9976V
	GAIN	−9.9927V

GROUND PLANE LAYOUT



ULTRA-FAST A/D WITH SAMPLE HOLD



When the ADC-817 or ADC-827 is configured as shown here with Datel-Intersil's SHM-6 hybrid sample-hold, a 10V input step can be acquired to 0.01% accuracy in 1 µsec and held to within 20 µV while the A/D conversion takes place. The SHM-6 can also be configured for inverting operation for applications with positive unipolar analog signals. Use of the SHM-6 reduces the time over which the input signal is averaged to a few nanoseconds (an A/D converter used without a samplehold averages the analog input signal over the total conversion time of the A/D).

NEW

DATEL

Microprocessor Compatible 8 Bit A/D Converter ADC-830

FEATURES

- **Microprocessor Compatible**
- **± ½ LSB Total Adjusted Error**
- **100 μsec Conversion Time**
- **Differential Analog Inputs**
- **Ratiometric Operation**
- **Single Supply Operation**

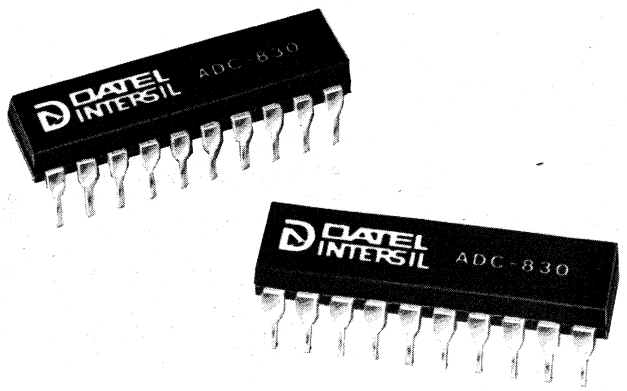
GENERAL DESCRIPTION

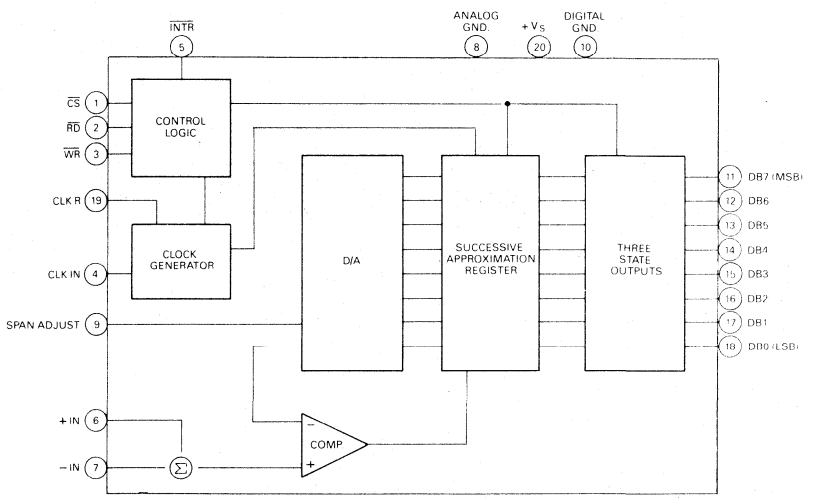
Datel-Intersil's ADC-830 is a low cost, 8 bit, CMOS A/D converter designed to operate directly with the 8080A control bus via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic. The ADC-830's digital control inputs, $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, are active low, and are available in all microprocessor memory systems. Upon completion of a conversion, an Interrupt signal is generated at the converter's output. The ADC-830 will operate as a normal A/D for non-microprocessor based applications.

Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8 bit conversion in 100 μsec with a maximum total adjusted error of only ± ½ LSB. No zero adjust is required. Also, the differential analog input allows the user to increase the common mode rejection and offset the zero value of the analog input.

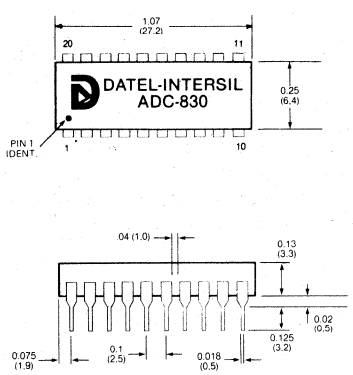
Other features include single supply operation and an internal clock generator. The clock generator requires only an external RC network or it may be driven by an external clock. The clock frequency range is 100 kHz to 1.2 MHz. In addition, the ADC-830 operates ratiometrically or with a 2.5V, 5V, or, to allow the encoding of smaller analog input voltage ranges, an analog-span-adjusted reference.

The ADC-830 is packaged in a 20 pin plastic DIP and operates over the 0°C to +70°C commercial temperature range. Power requirement is +5 VDC. With it's combination of low cost, small size, ease of digital interfacing, and versatility of analog interfacing, the ADC-830 is the ideal choice for many process control and instrumentation applications.





MECHANICAL DIMENSIONS · INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)	11	DB 7 (MSB)
2	$\overline{RD}$ (READ STROBE)	12	DB 6
3	$\overline{WR}$ (WRITE STROBE)	13	DB 5
4	CLOCK IN	14	DB 4
5	$\overline{INTERRUPT}$	15	DB 3
6	+ ANALOG IN	16	DB 2
7	- ANALOG IN	17	DB 1
8	ANALOG GROUND	18	DB 0 (LSB)
9	SPAN ADJUST	19	CLOCK RETURN
10	DIGITAL GROUND	20	+V SUPPLY

DATEL-INTERSIL, INC. 11 CABOT BOULEVARD, MANSFIELD, MA 02048 TELEPHONE (617) 339-9341/TXW 710-346-9341/TLX 951340

SPECIFICATIONS, ADC-830

Typical at +25°C, +5 VDC supply voltage, unless otherwise noted.

MAXIMUM RATINGS	
Supply Voltage	+6.5V
Digital Input Voltage	−0.3V to +18V
Analog Input Voltage	−0.3V to (V_S +0.3V)
Package Dissipation	875 mW
ANALOG INPUTS	
Analog Input Range [1]	−0.05V to $+V_S$ +0.05V
Common Mode Voltage Range	Gnd to $+V_S$
Common Mode Rejection, DC, max.	±2.44 mV
Input Resistance, Span Adjust, min.	2.5 kΩ
DIGITAL INPUTS	
Input Logic Level, Vin ("1")[2]	+2.0V min. to +15V max.
Input Logic Level, Vin ("0")[3]	+0.8V max.
Clock IN Threshold Voltage[4], Pos.	+2.7V min. to +3.5V max.
Neg.	+1.5V min. to +2.1V max.
Clock IN Hysteresis[4]	+0.6V min. to +2.0V max.
$\overline{CS}$ (Chip Select)	Active low state, enables the ADC-830 for read and write operations.
$\overline{WR}$ (Write Strobe)	Start conversion pulse. Input LO of 100 nsec min., in conjunction with a LO on $\overline{CS}$, resets S.A.R. and shift register.
$\overline{RD}$ (Read Strobe)	Output enable pulse. Input LO, in conjunction with a LO on $\overline{CS}$, enables three-state outputs. Maximum enable delay is 200 nsec.
Digital Input Capacitance, max.	7.5 pF
DIGITAL OUTPUTS	
Parallel Output Data	8 parallel lines of three-state, gateable output data.
$\overline{INT}$ (Interrupt)	Device status signal. LO when conversion complete. HI when conversion in progress and when output data enabled.
Output Logic Level, Vout ("1")[5]	+2.4V min. @ −360μA
Vout ("0")[6]	+0.4V max. @ 1.6 mA
Output Short Circuit Current, Gnd, min.	4.5 mA
Vs., min.	9.0 mA
Off-State Output Current	±3 μA
Digital Output Capacitance, max.	7.5 pF
PERFORMANCE	
Resolution	8 binary bits
Total Adjusted Error[7], max.	± ½ LSB
Conversion Time[8]	100 μsec
Conversion Rate[9], max.	8770 CPS
Clock Frequency Range[10]	100 kHz to 1.2 MHz
Output Enable Delay[11], max.	200 nsec
Three-State Control Delay[12], max.	250 nsec
Interrupt Output Delay, max.	450 nsec
Power Supply Sensitivity[13]	±2.44 mV
POWER REQUIREMENT	
Supply Voltage Range	+4.5 VDC to +6.3 VDC
Supply Current, max.	1.8 mA
PHYSICAL ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Type	20 pin plastic DIP

NOTES:

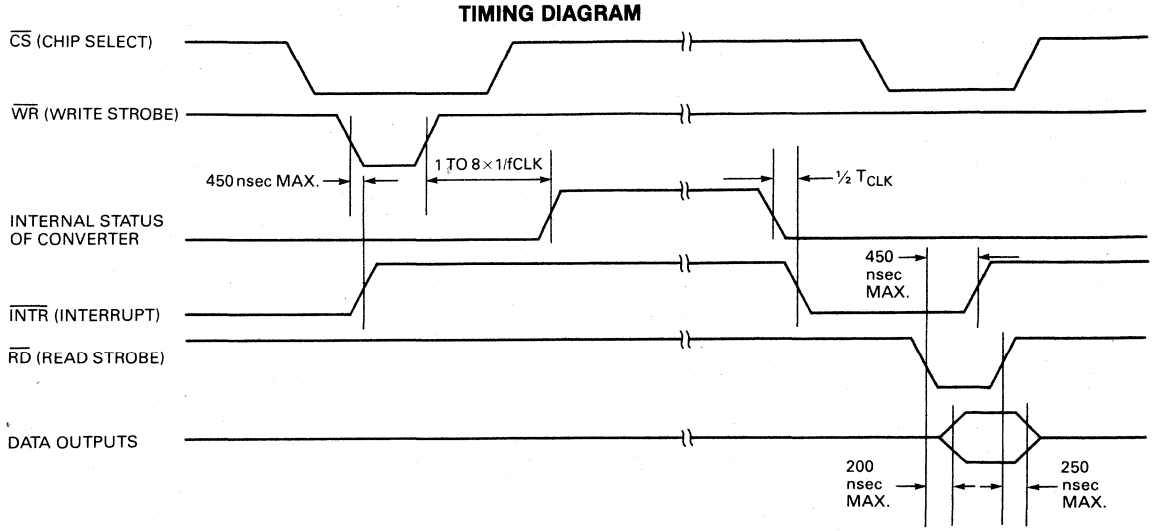
1. For Analog IN (−) ≥ Analog IN (+), the digital output code will be 0000 0000. Two internal diodes are connected to each analog input which will forward conduct for input voltages one diode drop below ground or above V_S.
2. V_S = +5.25 VDC, at V_S = +5 VDC, high level input current = 1 μA max.
3. V_S = +4.75 VDC, at V_S = +5 VDC, low level input current = 1 μA max.
4. Clock IN (Pin 4) is the input of a Schmitt Trigger circuit.
5. V_S = +4.75V. For Vout ("1") = 4.5V, high level output current = −10 μA.
6. V_S = +4.75V. Low level output current for the $\overline{Interrupt}$ Output is 1.0 mA.
7. Specified after full scale adjustment.
8. With an asynchronous start pulse, up to 8 clock periods may be required before conversion starts.
9. Conversion rate in free-running mode; $\overline{INTR}$ (Pin 5) connected to $\overline{WR}$ (Pin 3), CS (Pin 1) = OV, and f_{clk} = 740 kHz.
10. V_S = +6V. Clock frequency range at V_S = +5V is 100 kHz to 800 kHz.
11. C_L = 100 pf, use bus driver for larger C_L.
12. C_L = 10 pf, R_L = 10 KΩ.
13. V_S = +5V ±10% over full analog input range.

TECHNICAL NOTES

1. The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) are active low to allow easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (Pin 1) can be grounded and the standard A/D START function is obtained by an active low pulse on the WR input (Pin 3) and the Output ENABLE function is obtained by an active low pulse on the $\overline{RD}$ input (Pin 2).
2. The ADC-830 has a differential analog voltage input (Pins 6 & 7). The switching time between the inputs is 4.5 clock periods. The maximum error voltage due to this sampling delay is $\triangle V_e$ (max.) = $(V_P)(2\,\Pi\,f_{cm})(4.5/f_{clk})$ where: $\triangle V_e$ is the error voltage due to sampling delay, V_P is the peak value of the common-mode voltage, and f_{cm} is the common-mode frequency. Because of this internal switching action, displacement currents will flow at the analog inputs. These current transients occur at the leading edge of the internal clock, rapidly decay, and do not cause errors as the comparator is strobed at the end of the clock period. However, if the voltage source applied to Ana. IN + (Pin 6) exceeds V_S by more than 50 mV, a large current may flow through a parasitic diode to V_S. If these currents could exceed 1 mA, an external diode should be connected between Ana. IN + (Pin 6) and V_s (Pin 20).
3. The leads to the analog inputs should be kept as short as possible to prevent noise pickup. The source resistance for these inputs should be kept below 5kΩ. Input bypass capacitors should not be used as they will average the transient input switching currents of the converter causing scale errors.
4. The ADC-830 may be used with a 5V, 2.5V or adjusted voltage reference. The reference is either ½ the value of V_S or equal to a voltage applied to the span adjust pin (Pin 9). This allows for operation in either a ratiometric mode or an absolute mode. The internal gain for the span adjust input is 2.
5. The clock for the ADC-830 may be derived from the CPU or an external RC can be added to provide self clocking. A resistor (≈10KΩ) is connected between CLK Return (Pin 19) and CLOCK IN (Pin 4) and a capacitor is connected between CLOCK IN and ground. The resultant clock frequency is f_{clk} = 1/1.1 RC. Heavy capacitive or DC loading of the Clock Return pin should be avoided, a CMOS or low power TTL Buffer should be used to drive loads greater than 50pf.
6. For continuous conversion operation, the $\overline{CS}$ input (Pin 1) is grounded and the $\overline{WR}$ input (Pin 3) is connected to the INTR output (Pin 5). $\overline{WR}$ and $\overline{INTR}$ should be momentarily forced LOW following a power-up cycle to guarantee operation.
7. The ADC-830 will require a bus driver when the total capacitance of the data bus gets large. For systems with a slow CPU clock frequency, higher capacitive loads may be driven. Low power Schottky or high current bipolar bus drivers with PNP inputs are recommended.
8. The use of good circuit board layout techniques is required for rated performance. Sockets on a PC board should be used, all logic signal leads should be grouped and kept as far as possible from the analog inputs, and the analog inputs should be shielded. A single point analog ground should be used that is separate from the digital ground. V_S should be bypassed, as close to the V_S pin as possible, with a low inductance 1 μF tantalum capacitor. The V_S bypass capacitor and self-clocking capacitor (if used) should be returned to digital ground.

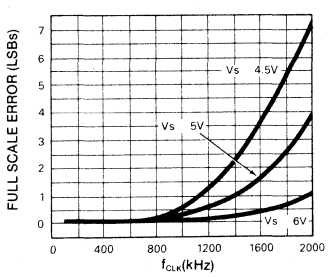
TIMING AND PERFORMANCE

TIMING DIAGRAM

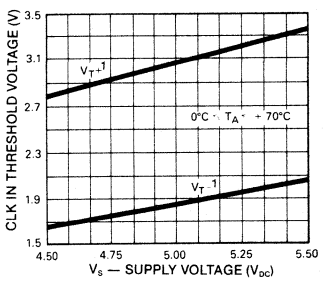


TYPICAL PERFORMANCE CHARACTERISTICS

FULL-SCALE ERROR VS f_{CLK}

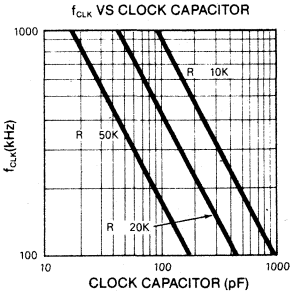


CLK IN SCHMITT TRIP LEVELS VS SUPPLY VOLTAGE

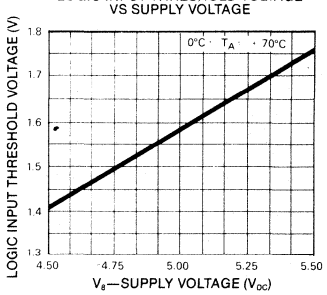


1. V_T = The positive or negative clock IN threshold voltage

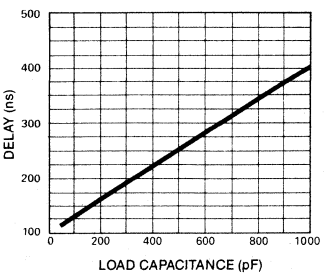
f_{CLK} VS CLOCK CAPACITOR



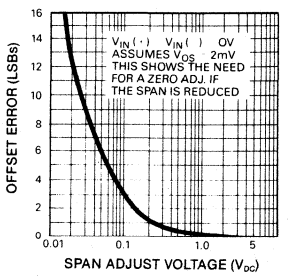
LOGIC INPUT THRESHOLD VOLTAGE VS SUPPLY VOLTAGE



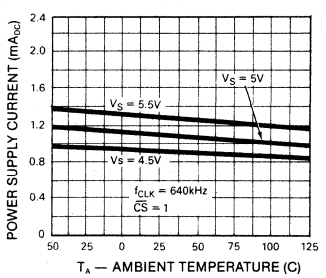
DELAY FROM FALLING EDGE OF RD TO OUTPUT DATA VALID VS LOAD CAPACITANCE



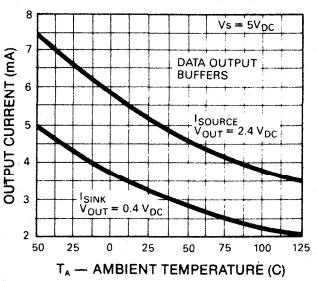
EFFECT OF UNADJUSTED OFFSET ERROR VS SPAN ADJ. VOLTAGE



POWER SUPPLY CURRENT VS TEMPERATURE



OUTPUT CURRENT VS TEMPERATURE



ORDERING INFORMATION

MODEL ADC-830C

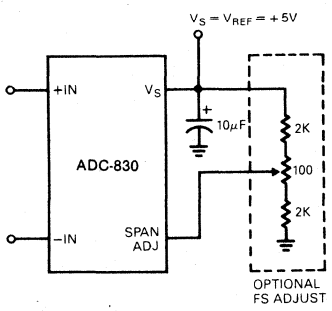
OPERATING TEMP. RANGE..... 0°C to +70°C

PRICE (1-24) .....

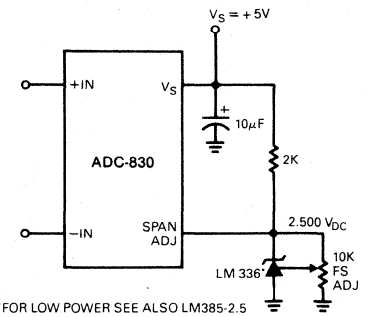
TRIMMING POTENTIOMETERS TP100, TP 10K .....

TYPICAL APPLICATIONS

ABSOLUTE WITH A +5V REFERENCE

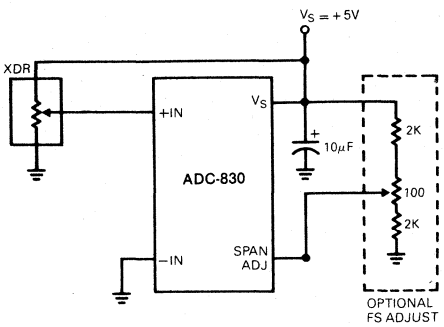


ABSOLUTE WITH A 2.500V REFERENCE

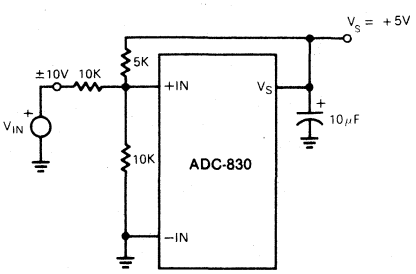


*FOR LOW POWER SEE ALSO LM385-2.5

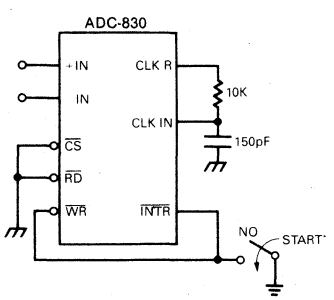
RATIOMETRIC WITH FULL SCALE ADJUST



HANDLING ± 10V ANALOG INPUTS

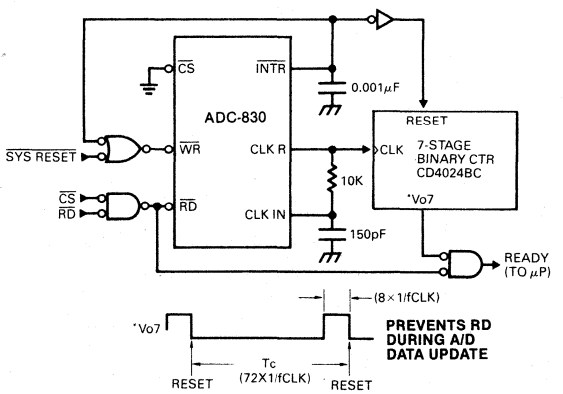


SELF—CLOCKING IN FREE-RUNNING MODE

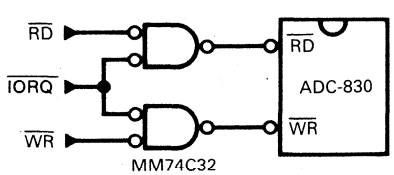


AFTER POWER-UP, A MOMENTARY GROUNDING OF THE WR INPUT IS NEEDED TO GUARANTEE OPERATION.

μP INTERFACE FOR FREE-RUNNING A/D

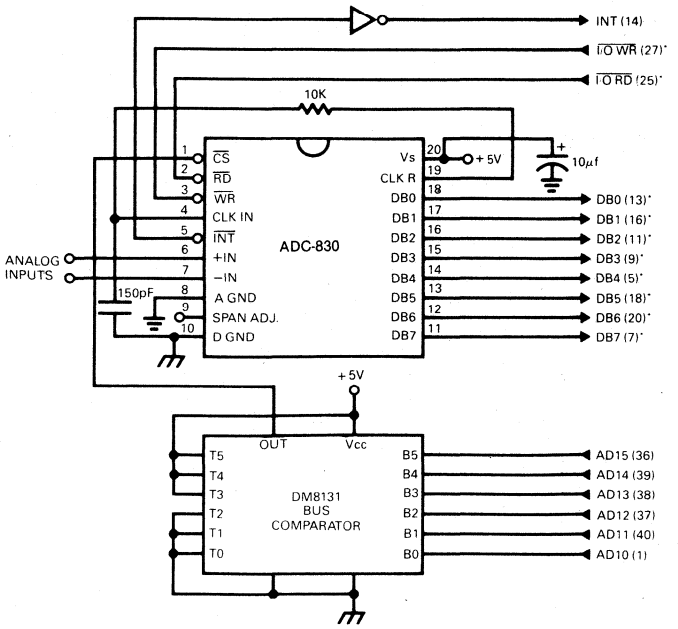


Z-80 CPU INTERFACE



The Z-80 control bus provides a memory request signal, MREQ, and I/O request signal, IOREQ, which must be combined with the general RD and WR strobes to provide the equivalent 8080A control bus signals. When operating the A/D in I/O space with the Z-80, the CPU will automatically insert one wait state (the RD and WR strobes are extended one clock period) to allow more time for the I/O devices to respond.

INS 8080A CPU INTERFACE

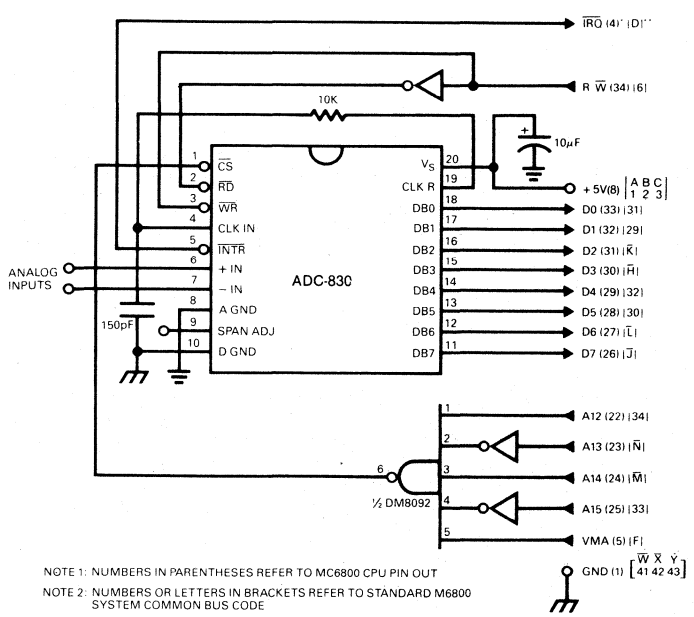


NOTE 1: *PIN NUMBERS FOR THE INS8228 SYSTEM CONTROLLER, OTHERS ARE INS8080A.

NOTE 2: PIN 23 OF THE INS8228 MUST BE TIED TO +12V THROUGH A 1K Ω RESISTOR TO GENERATE THE RST7 INSTRUCTION WHEN AN INTERRUPT IS ACKNOWLEDGED AS REQUIRED BY THE ACCOMPANYING SAMPLE PROGRAM.

The ADC-830 is designed to interface directly with derivatives of the 8080 μP. The converter can be mapped into memory space using standard memory address decoding, or it can be controlled as an I/O device by using the $\overline{I/O}$ R and $\overline{I/O}$ W strobes and decoding address bits A0 → A7 (or A8 → A15) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8 bit address decoder but the data can only be input to the accumulator. In systems where the A/D converter is 1 of 8 or less I/O mapped devices, no address decoding circuitry is required. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

MC 6800 CPU INTERFACE

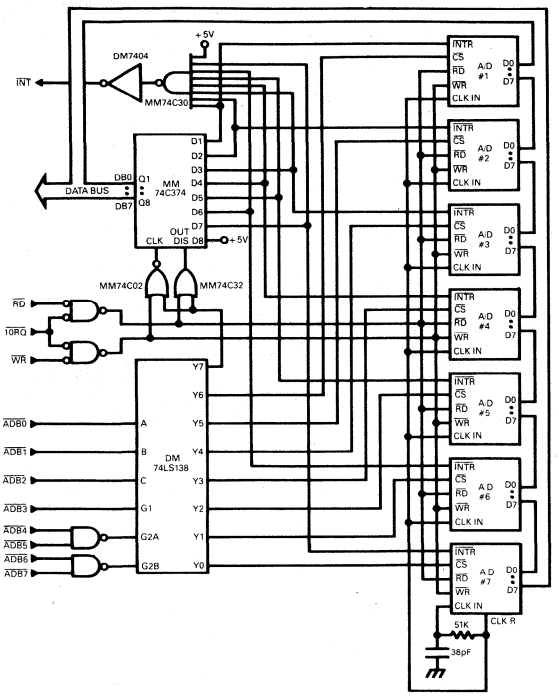


NOTE 1: NUMBERS IN PARENTHESES REFER TO MC6800 CPU PIN OUT

NOTE 2: NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD M6800 SYSTEM COMMON BUS CODE

The control bus for the 6800 μP derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the Ø2 clock. All I/O devices are memory mapped in the 6800 system and a special signal, VMA, indicates that the current address is valid. In many 6800 systems an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the ADC-830's $\overline{CS}$ pin if no other devices are addressed at Hex ADDR: 4XXX or 5XXX.

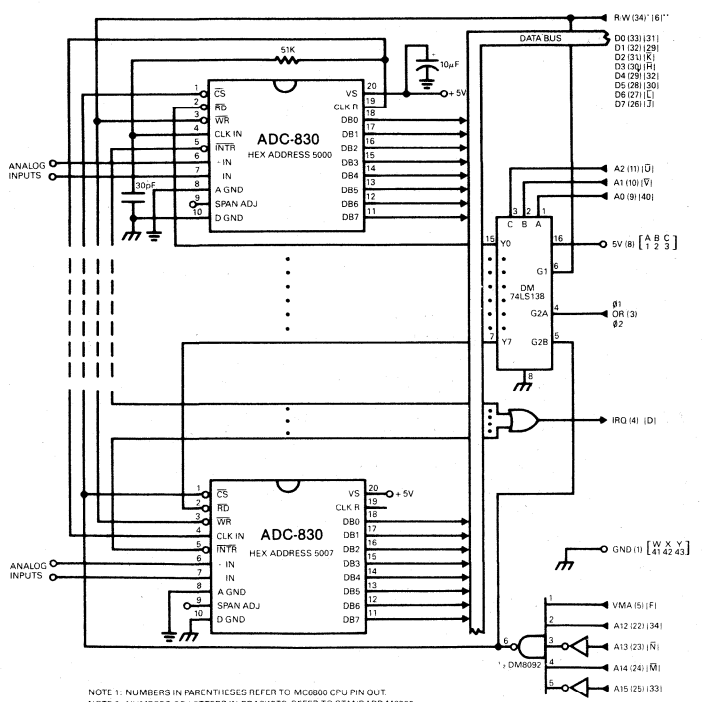
MULTIPLE ADC-830'S IN A MC6800 SYSTEM



When transferring analog data from several channels to a single μP system, a multiple converter scheme presents several advantages over the conventional multiplexer single converter approach. With the ADC-830, the differential inputs allow individual span adjust for each channel. Also, the channels are sensed simultaneously, reducing the microprocessor's total system servicing time.

In the system shown, the ADC-830's have been arbitrarily located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. The system can easily be extended to allow the interfacing of more converters.

MULTIPLE ADC-830'S IN A Z-80 INTERRUPT DRIVE MODE



NOTE 1: NUMBERS IN PARENTHESES REFER TO MC6800 CPU PIN OUT.
NOTE 2: NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD M6800 SYSTEM COMMON BUS CODE.

In data acquisition systems where more than one peripheral device will be interrupting program execution of a microprocessor, the CPU must determine which device requires servicing. The circuit shown allows the ADC-830's to be started in any sequence, but will input and store valid data with a priority sequence of A/D #1 through A/D # 7. Only the converters whose $\overline{INT}$ is asserted will be read.

NEW

DATEL

6-Bit Video Flash A/D Converter ADC-833

FEATURES

- **6 Bits at 15 MHz**
- **200 mW Power Dissipation**
- **± ½ LSB Linearity**
- **Three-State Outputs**
- **Single Supply Operation**
- **Internal Zener Reference**

GENERAL DESCRIPTION

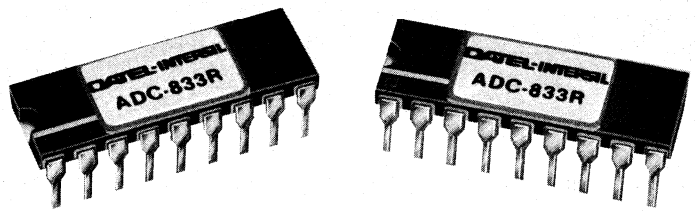
Datel-Intersil's ADC-833 is a video speed, low power, 6 bit flash A/D converter manufactured with CMOS/SOS technology. The ADC-833 is capable of digitizing an analog input signal at conversion rates up to 15 MHz while its power consumption is only 200 mW.

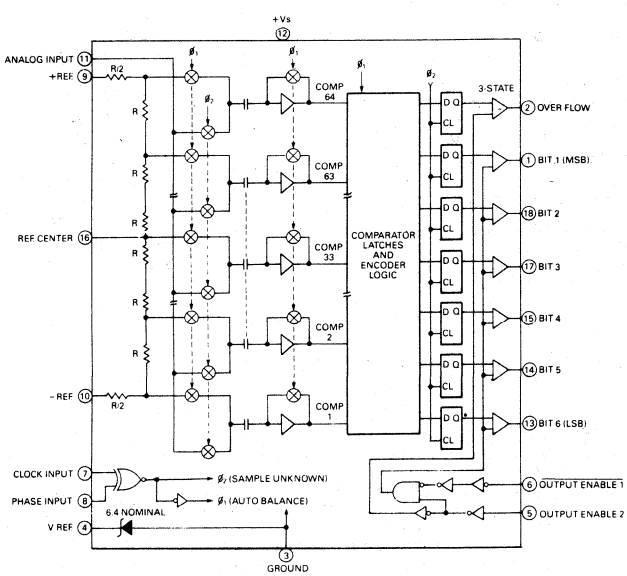
The ADC-833 consists of 64 auto-balanced comparators, a resistor ladder network, a zener reference diode, a decoder and seven buffer storage registers. A sequential parallel technique is employed to achieve the high conversion speed, making possible a complete analog to digital conversion in one clock cycle. The analog input voltage range is +2.5V to +10V, and typical differential linearity error is only ± ½ LSB. All digital inputs and outputs are TTL/CMOS compatible.

Outputs are buffered three-state and include an overflow output which allows the user to cascade two units to achieve 7-bit resolution. The buffers are controlled by two enable signals with a typical output enable delay of only 20 nsec. A phase input is provided to allow the user to effectively complement the clock and an onboard 6.4V zener diode is provided for use as a reference voltage.

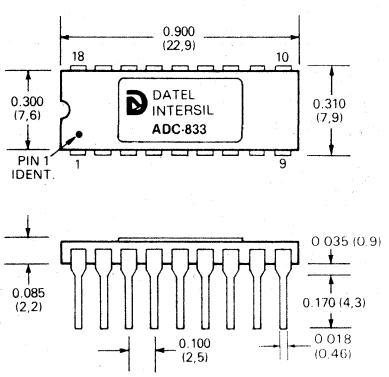
The ADC-833 is ideally suited for applications that require high-speed digitization and low power consumption. Such applications would include CRT graphics, radar pulse analysis, motion signature analysis and optical character recognition.

The ADC-833 is packaged in an 18 pin ceramic DIP and operates over the −25°C to +85°C industrial temperature range.





MECHANICAL DIMENSIONS



INPUT/OUTPUT

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB)	10	− REFERENCE
2	OVER FLOW OUT	11	ANALOG INPUT
3	GROUND	12	V SUPPLY
4	REFERENCE ZENER	13	BIT 6 OUT (LSB)
5	OUTPUT ENABLE 2	14	BIT 5 OUT
6	OUTPUT ENABLE 1	15	BIT 4 OUT
7	CLOCK INPUT	16	REFERENCE CENTER
8	PHASE INPUT	17	BIT 3 OUT
9	+ REFERENCE	18	BIT 2 OUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-833
Typical at +25°C, V_S = +5 VDC unless otherwise noted.

MAXIMUM RATINGS	
Supply Voltage	−0.5V to +10V
Analog Inputs[1]	−0.5V to (+V_S +0.5V)
Logic Inputs	−0.5V to (+V_S +0.5V)
Input Current, D.C.	±10 mA
Package Dissipation[2]	315 mW
INPUTS	
Analog Input Range	+2.5V to +10V
Analog Input Current, max.	1 mA
Ladder Impedance	1.4kΩ
Input Capacitance	50 pF
Input Logic Level, Vin ("1"), min.[3]	+3.0 V
Input Logic Level, Vin ("0"), max.[4]	+1.5 V
OUTPUTS	
Parallel Output Data	6 parallel lines of data & overflow
Output Logic Level, Vout ("1"),[5]	+4.6 V @ −0.8 mA min.
Output Logic Level, Vout ("0"),[6]	+0.4V @ 1.6 mA min.
Zener Reference, Voltage[7]	6.4 V
Impedance,[7] **max.**	30 Ω
PERFORMANCE	
Resolution	6 bits
Conversion Speed, min[8]	15 MHz
Nonlinearity, max[9]	±0.8 LSB
Differential Linearity Error, max.[9]	±0.8 LSB
Quantizing Error	±½ LSB
Aperture Time[10]	25 nsec
Output Enable Delay[10]	20 nsec
Gain Tempco[11]	25 ppm/°C
Zener Reference Tempco	±0.5 mV/°C
POWER REQUIREMENT	
Analog Supply Voltage Range	+3V to +10V
Quiescent Current,[12] V_S = +5V	7 mA
V_S = +8V	22 mA
Power Dissipation, V_S = +8V	200 mW
PHYSICAL—ENVIRONMENTAL	
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Type	18 pin ceramic DIP

NOTES:
1. All inputs except Zener Ref. (Pin 4).
2. Specified for T_A = −25°C to +55°C. For T_A = +55°C to +85°C, derate linearly at 3.3 mW/°C.
3. At V_S = +8V, the minimum Input Logic Level, V_{IN} ("1") is +5.5V.
4. At V_S = +8V, the maximum Input Logic Level, V_{IN} ("0") is +2.5V.
5. At V_S = +8V, the Output Logic Level, V_{out} ("1") is 7.5V @ −1.6 mA min.
6. At V_S = +8V, the Output Logic Level, V_{out} ("0") is 0.5V @ 3.2 mA min.
7. Specified at I_Z = 10 mA.
8. Specified at V_S = +8V. At V_S = +5V, the typical sampling rate is 12 MHz.
9. Specified at V_S = +8V, V_{ref} = +7.68V, clk = 15 MHz, with gain adjusted.
10. Specified at V_S = +8V. The aperture time specification for an A/D converter refers to the time uncertainty of the exact instant that the sample is taken at the analog input.
11. Specified at V_S = +8V, clk = 15 MHz.
12. Does not include Zener current and reference ladder current. Specified at V_S = +5V with an 11 MHz clock, at V_S = +8V with a 15 MHz clock. If the clock is held in the "Auto Zero" state, the maximum quiescent current at V_S = +5V is 16 mA, at V_S = +8V, the maximum is 40 ma.

ORDERING INFORMATION

MODEL NO	OPERATING TEMPERATURE RANGE	PRICE (1-24)
ADC-833R	−25°C to +85°C	

TECHNICAL NOTES

1. These are CMOS devices and may be damaged by electrostatic discharge. All inputs and outputs of the ADC-833 have a network for electrostatic protection, however, standard anti-static precaution should be taken to prevent possible damage. To prevent damage to the input protection circuit, input signals should not exceed V_S nor be less than the ground potential on Pin 3. Input currents must not exceed 10 mA even when the power supply is off. All unused input terminals must be grounded or connected to V_S, whichever is appropriate.

2. The ADC-833 may be operated in a pulse mode when sampling high speed nonrecurrent or transient data. The fastest method is to keep the converter in the Sample Unknown phase, Ø2 (see operating theory) during the standby state. The converter can be pulsed through the Auto Balance phase, Ø1, in as little as 33 nsec. The analog input is taken on the leading edge of Ø1 and transferred into the output registers on the trailing edge of Ø1, putting the converter back in the standby state. Another conversion can be started within 33 nsec, but no later than 10 μsec due to the eventual droop of the commutating capacitors. The larger the time ratio between Ø1 and Ø2, the lower the power consumption.

3. For most applications, the accuracy of the ADC-833 should be sufficient without external adjustment. However, where accuracy is of paramount importance, three adjustments can be made; Offset Trim, Gain Trim, and Midpoint Trim.

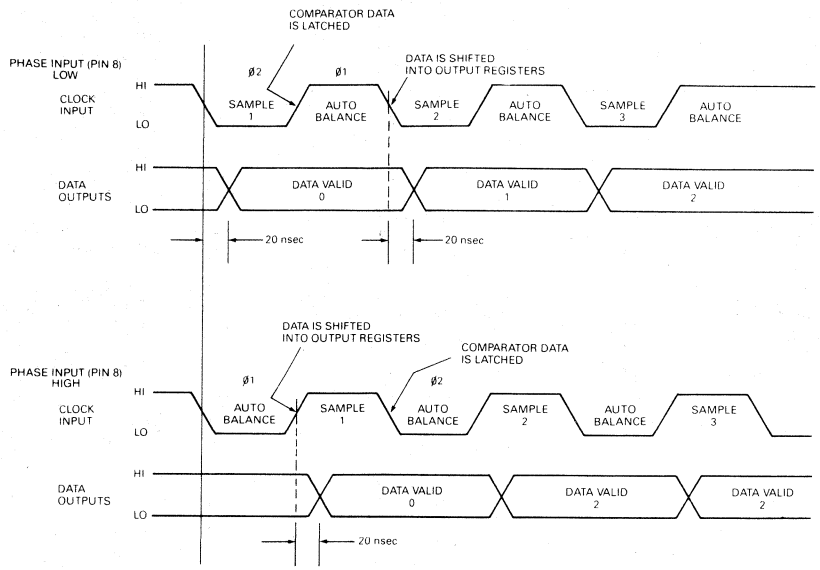
   The offset may be adjusted in the preamp circuitry by introducing a DC shift to the analog input. If this is not possible, the -Ref. pin (pin 10) can be adjusted to set the first transition at its theoretical value, -Vref/128. If the transition is lower than the theoretical, then a single turn 50Ω pot connected between -Ref. and ground will accomplish the adjustment. If the transition is greater than the theoretical, the 50Ω pot should be connected between -Ref. and a negative voltage equal to approximately two LSB's.

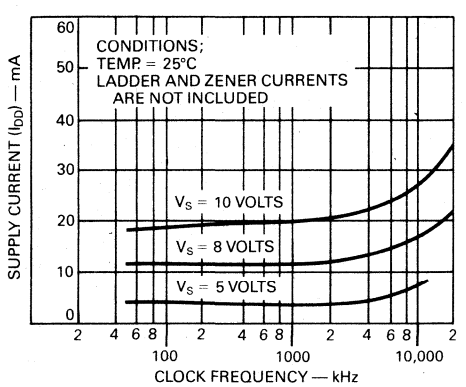
   The gain may also be adjusted in the preamp circuitry. The gain can be adjusted at the converter by making an adjustment to the reference voltage. To adjust the gain, first set the offset trim then set the input voltage to the value Vref (127/128). Now adjust Vref until that transition occurs on the output.

   The midpoint trim should be done after the gain and offset trims. The theoretical input voltage for the half scale transition is 32.5 (Vref/64). A 2 kΩ pot may be connected between + Ref (pin 9) and - Ref (pin 10) with the wiper connected to Ref. center (pin 16). Set Vin to the theoretical half scale voltage and adjust the output for that transition.

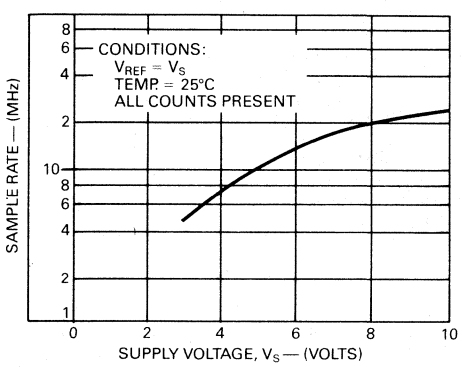
TIMING AND PERFORMANCE

TIMING DIAGRAM

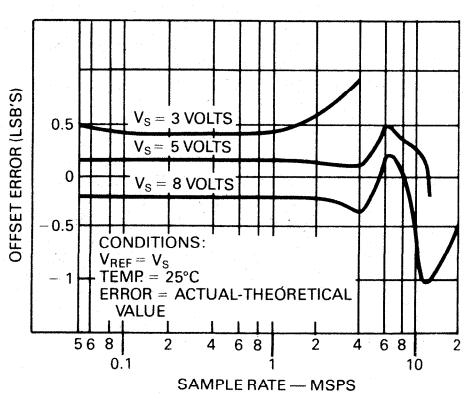




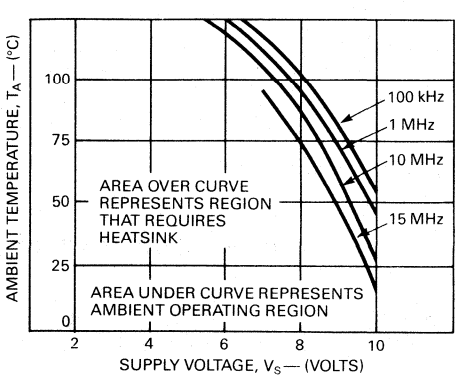
Typical current drain versus sampling rate as a function of supply voltage.



Typical maximum sample rate versus supply voltage.

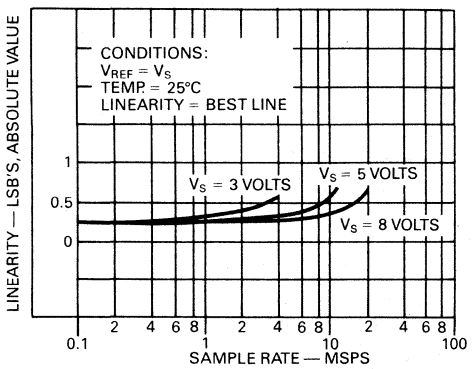


Typical offset error versus sample rate as a function of supply voltage.

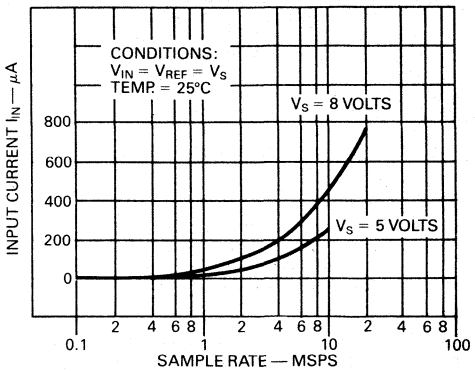


Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

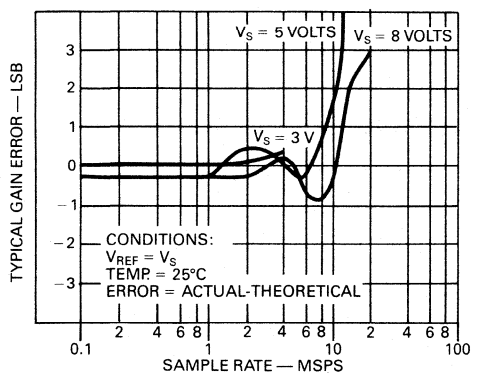
PERFORMANCE



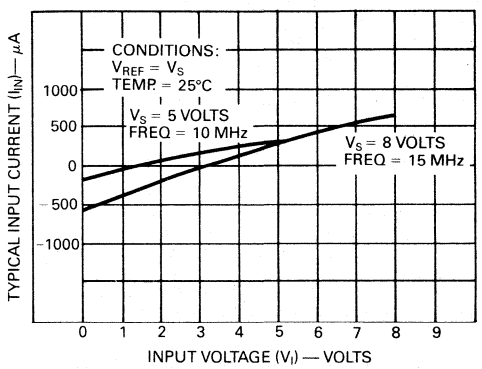
Typical linearity versus sample rate as a function of supply voltage.



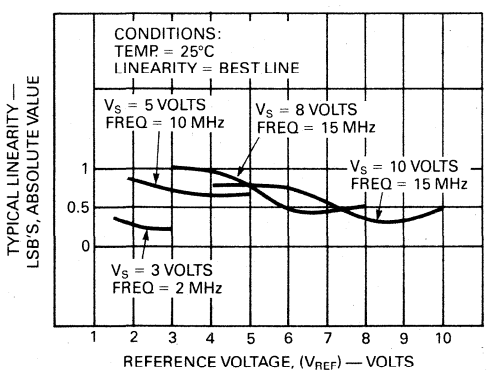
Typical input current versus sample rate as a function of supply voltage.



Typical gain error versus sample rate as a function of supply voltage.

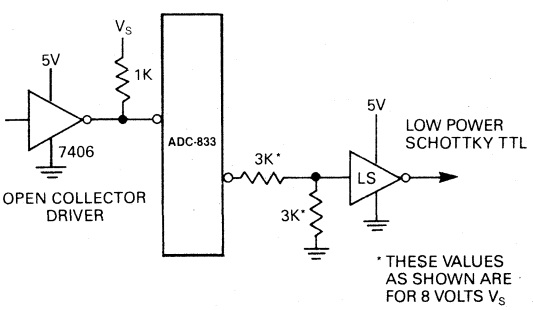


Typical input current versus input voltage as a function of supply voltage.



Typical linearity versus reference voltage as a function of supply voltage.

LOGIC INTERFACE CIRCUITS



TTL interface circuit for V_S >5.5 volts.

THEORY OF OPERATION

The ADC-833 employs a sequential parallel technique, consisting of an "Auto Balance" phase (Ø1) and a "Sample Unknown" phase (Ø2), to achieve its high speed operation. Each conversion takes one clock cycle. With the phase input low (Pin 8), "Auto Balance" (Ø1) occurs during the high period of the clock cycle, and "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, 64 commutating capacitors are connected to their associated ladder reference tap through a transmission switch. The tap voltage is equal to V_{tap} (N) = V_{ref} (2N – 1)/128, where: V_{tap} (N) equals the reference ladder tap voltage at point N; V_{ref} equals the voltage across + Ref. (Pin 9) to – Ref. (Pin 10); and N equals the tap number.

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input. The amplifier is biased at its intrinsic trip point, approximately $V_S/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, the ladder tap switches are opened, the comparator amplifiers are no longer shorted, and the analog input (Pin 11) is switched to all 64 capacitors. With the other end of the capacitor looking into what is effectively an open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparators. All comparators with tap voltages greater than the analog input will have a "low" output, comparators with a tap voltage lower than the analog input will have a "high" output.

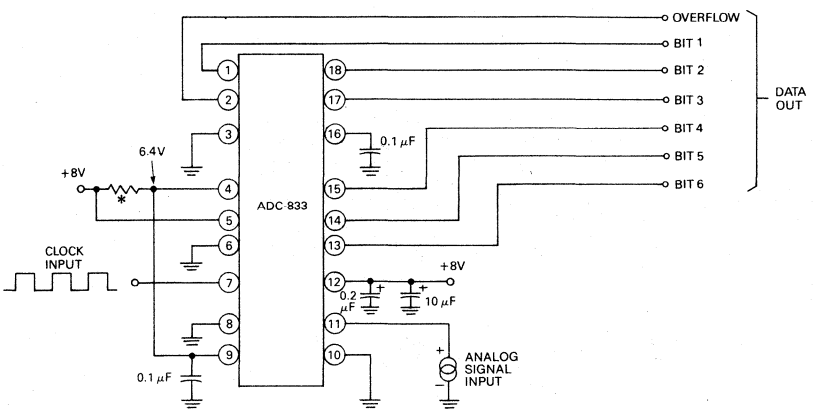
The comparator outputs are stored at the end of the "Sample Unknown" phase by secondary latching amplifiers. Once latched, the outputs are decoded by a 64 to 7 decode array and the result is clocked into a storage register on the rising edge of the next "Sample Unknown" phase.

A three-state buffer is used at the output of the storage registers. The buffer is controlled by two enable signals. Output Enable 1 (Pin 6) will disable Bit 1 through Bit 6 when it is in a high state, Output Enable 2 (Pin 5) will disable Bit 1 through Bit 6 and the overflow output when it is in a low state.

A phase input (Pin 8) is provided to allow the user to effectively complement the clock and an onboard zener is provided for use as a reference voltage.

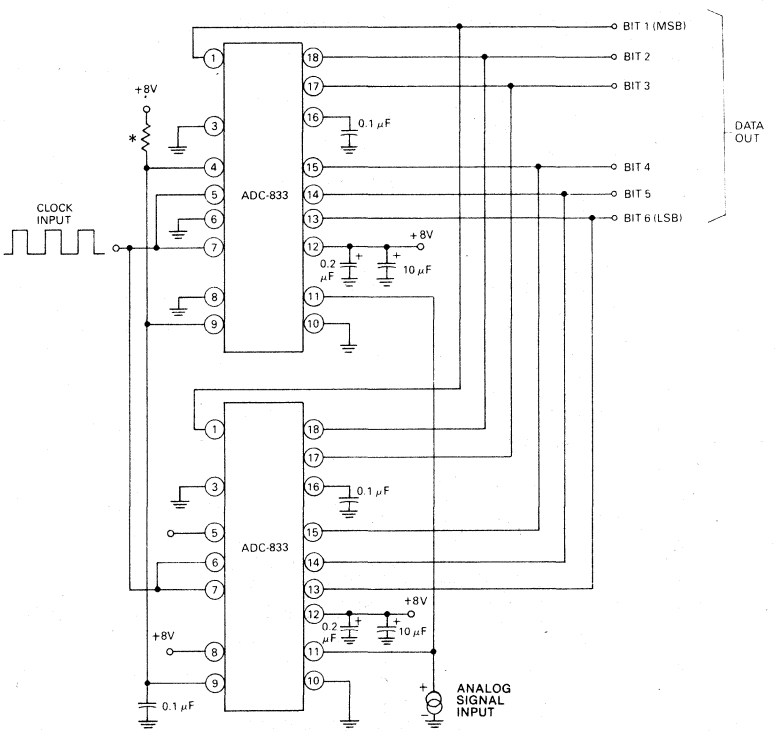
CONNECTION AND APPLICATION

TYPICAL CONNECTION - 6 BITS AT 15 MHz



* RESISTOR MUST BE SELECTED TO PROVIDE A ZENER CURRENT OF 10 mA.

TYPICAL CONNECTION - 6 BITS AT 30 MHz

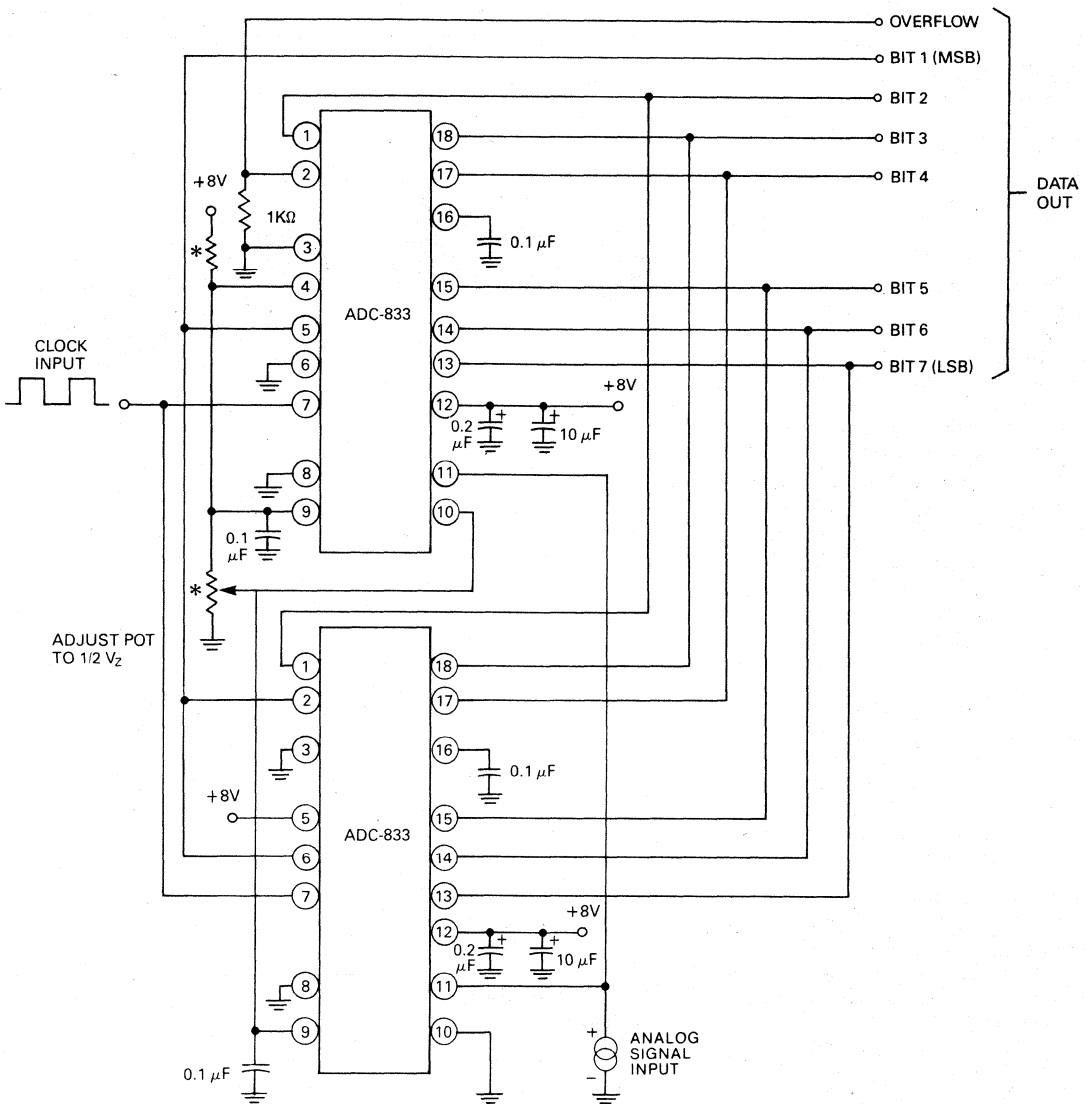


Two ADC-833's may be connected in parallel to increase the conversion speed from 15 MHz to 30 MHz.

* RESISTOR MUST BE SELECTED TO PROVIDE A ZENER CURRENT OF 10 mA.

CONNECTION AND APPLICATION

TYPICAL CONNECTION - 7 BIT RESOLUTION



*RESISTORS MUST BE SELECTED TO PROVIDE A ZENER CURRENT OF 10mA

Two ADC-833's may be connected in series to produce a high speed 7 bit converter. First, the ladder networks are totem-poled. Since the absolute resistance value of each ladder may vary, an external mid-reference voltage trim may be required. The overflow output of the lower device now becomes Bit 7. When it goes high, all counts must come from the upper device, when it goes low, all counts come from the lower device. The three-state outputs of the two devices are connected in parallel to complete the circuit.

NEW

DATEL

Microprocessor Compatible 8-Bit A/D Converter ADC-847

FEATURES

- **Microprocessor Compatible**
- **9 μsec Conversion Time**
- **8-Bit Resolution**
- **± ¼ LSB Linearity Error**
- **Ratiometric Operation**

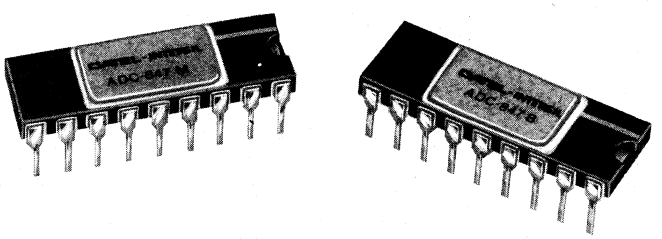
GENERAL DESCRIPTION

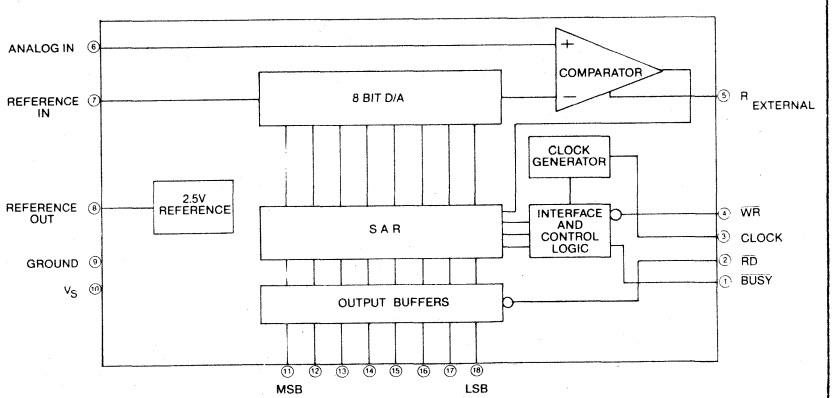
DATEL-INTERSIL's ADC-847 is a low cost, monolithic, 8-bit A/D converter designed to interface directly with a microprocessor via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus requires a minimum of interfacing logic. Using the successive approximation technique, the ADC-847 completes an 8 bit conversion in 9 μS with a maximum linearity error as low as ± ¼ LSB.

The data outputs of the ADC-847 are provided with three-state buffers to allow connection to a common data bus. The digital control lines; $\overline{WR}$, $\overline{RD}$ and $\overline{BUSY}$ are active low and are available in most microprocessor memory systems. The $\overline{BUSY}$ output uses a passive pull-up for CMOS/TTL compatibility which also allows up to four $\overline{BUSY}$ outputs to be wire-ANDed together to form a common interrupt line. The ADC-847 will operate as a normal A/D converter for non-microprocessor applications.

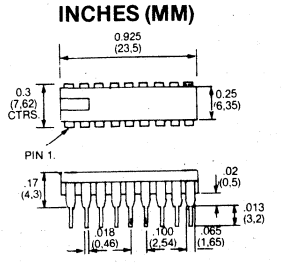
Other important features include single supply operation capability, ratiometric operation, internal reference circuit and internal clock generator. The clock generator requires only an external capacitor or the device may be driven with an external clock. The reference circuit only requires an external resistor and capacitor or an external reference voltage can be connected to the reference input (Pin 7) if required. The ADC-847 is an ideal choice for many process control and instrumentation applications.

The ADC-847 is available for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges and is packaged in either an 18 pin plastic or ceramic DIP.

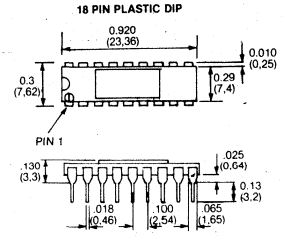




MECHANICAL DIMENSIONS INCHES (MM)



18 PIN PLASTIC DIP



18 PIN CERAMIC DIP

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	$\overline{BUSY}$ (STATUS)
2	$\overline{RD}$ (OUTPUT ENABLE)
3	CLOCK
4	$\overline{WR}$ (START CONVERSION)
5	EXTERNAL RESISTOR
6	ANALOG INPUT
7	REFERENCE INPUT
8	REFERENCE OUTPUT
9	GROUND
10	+ V SUPPLY
11	DB7 (MSB)
12	DB6
13	DB5
14	DB4
15	DB3
16	DB2
17	DB1
18	DBO (LSB)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-847

Typical at +25°C, +5 VDC supply voltage, 900 kHz clock frequency, unless otherwise noted.

	ADC-847A	ADC-847B	ADC-847M
MAXIMUM RATINGS			
Supply Voltage		+7.0V	
Digital Input Voltage		V_S	
Analog Input Voltage		V_S	
ANALOG INPUTS			
Analog Input Range		−0.5V to +3.5V	
Input Resistance		100 kΩ	
Reference Input Range		+1V to +3V	
Input Current[1]		1 μA	
DIGITAL INPUTS			
Input Logic Level, Vin ("1"), min.		2V	
Input Logic Level, Vin ("0"), max.		0.8V	
Input Logic Level, Iin ("1")[2]		300 μA	
Input Logic Level, Iin ("0")[3]		±10 μA	
Clock Input Voltage (pin 3)			
high level, min.		4.0V	
low level, max.		0.8V	
Clock Input Current, high level, max.		800 μA	
low level, max.		−500 μA	
Clock Pulse Width, min.		500 nsec	
$\overline{WR}$ (Write)		Start conversion pulse. 200 nsec minimum pulse width. Active low input.	
$\overline{RD}$ (Read)		Active low state enables 3-state outputs.	
Input Clamp Diode Voltage, max.		−1.5V	
DIGITAL OUTPUTS			
Parallel Ouput Data		8 parallel lines of three-state, gateable output data.	
Output Coding, Unipolar		Binary	
Bipolar		Offset Binary	
$\overline{BUSY}$		Active low output. HI when conversion complete. LO when conversion in progress.	
Output Logic Level, Vout ("1"), min.		2.4V	
Vout ("0"), max.		0.4V	
Output Logic Level, Iout ("1"), max.		100 μA	
Iout ("0"), max.		1.6 mA	
Off-state output leakage current, max.		2 μA	
PERFORMANCE			
Resolution		8 binary bits	
Linearity Error, max.	±1 LSB	±¼ LSB	±¼ LSB
Differential Linearity Error, max.	±1 LSB	±½LSB	±½LSB
Conversion Time		9 μsec	
Internal Clock Frequency, max.		1 MHz	
External Clock Frequency, max.		1 MHz	
Reference Output Voltage, max.[4]	2.600V	2.570V	2.570V
Reference Slope Resistance, max.		2 Ω	
Reference Voltage Tempco		50 ppm/°C	
Reference Current, max.		15 mA	
min.		4 mA	
Linearity Tempco		±3.0 ppm/°C	
Zero Tempco		±8.0 ppm/°C	
Full-Scale Tempco		±2.5 ppm/°C	
POWER REQUIREMENT			
Supply Voltage Range		+4.5 VDC to +5.5 VDC	
Supply Current, max.		40 mA	
Power Consumption		125 mW	
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range			
ADC-847 A		0°C to +70°C	
ADC-847 B		0°C to +70°C	
ADC-847 M		−55°C to +125°C	
Storage Temperature Range		−55°C to +125°C	
Package Type, 18 Pin DIP	Plastic	Plastic	Ceramic

NOTES:
1. Input voltage = +3V and Rext = 82 KΩ.
2. Input voltage = 2.4V, supply voltage = 5.5V. For $\overline{RD}$ input, Iin ("1") = −150 μA.
3. Input voltage = +0.4V, supply voltage = 5.5V For $\overline{RD}$ input, Iin ("0") = −300 μA.
4. Rref = 390Ω, Cref = 4.7 μF.

TECHNICAL NOTES

1. The internal clock generator requires an external capacitor connected between Pin 3 and ground. The oscillator frequency may be trimmed with an external trim resistor connected in series with the capacitor. For optimum accuracy and stability of the oscillator frequency without trimming, the use of a crystal or ceramic resonator connected between Pins 3 and 9 is recommended.

   An external clock signal from a TTL or CMOS gate to Pin 3 may be used if the application requires.

2. A 390Ω reference resistor (Rref) should be connected between Pins 8 and 10. This will supply a nominal reference current of 6.4 mA. Also, a 4.7 μF stabilizing/decoupling capacitor (Cref) should be connected between Pins 8 and 9. For internal reference operation, Vref OUT (Pin 8) is connected to Vref in (Pin 7).

3. An external reference may be used if required. Voltage should be in the range of +1.5 to +3.0 volts and may be connected to Vref IN. The slope of such a reference source should be less the $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

4. A continuous conversion can be accomplished by inverting the $\overline{BUSY}$ and feeding it to the convert ($\overline{WR}$) input. To ensure reliable operation, an initial start pulse is required. This can be accomplished by using a NOR gate instead of an inverter and feeding it with a positive going pulse. The pulse can be derived from a simple R.C. network that gives a single pulse when power is applied.

5. For ratiometric operation, if the output from a transducer varies with its supply, then an external reference for the A/D should be derived from the same supply. The external reference can vary from +1.5V to +3.0V. Operation with a reference voltage less than +1.5V is possible but reduced overdrive to the comparator will increase its delay and the conversion time will need to be increased.

6. The $\overline{WR}$ (start conversion pulse) can be completely asynchronous with respect to the clock, and will produce valid data between 7½ and 8½ clock pulses later depending on the timing of the clock and CONVERT signals.

7. Upon receiving a convert pulse, the A/D is reset. (The MSB is set to "1" all other bits are set to "0" and the $\overline{BUSY}$ output goes low.) The A/D will remain in this state until the convert pulse returns high. After the start conversion input goes high, the MSB decision will be made on the falling clock edge after a rising clock edge (See timing diagram). This will insure that the MSB is allowed to settle for at least half a clock period or 550 nS at maximum clock frequency.

   The START CONVERSION ($\overline{WR}$) input is not locked out during a conversion. Therefore, if pulsed low at any time, the conversion will restart.

8. The ADC-847 can be operated with a single supply. However, a negative supply voltage is required to supply the tail current of the comparator. Since this current is only 25 to 150μA and does not have to be well stabilized, it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output. (See single supply operation.)

CALIBRATION PROCEDURE

For calibration procedure, unipolar and bipolar, apply continuous convert pulses to start conversion ($\overline{WR}$) input long enough to allow a complete conversion and monitor the digital outputs.

CALIBRATION

UNIPOLAR

Zero Adjust Apply .5 LSB to the analog input and adjust the ZERO ADJUST pot until the LSB (Bit 8) just flickers between 0 and 1 with all other bits at 0.

Gain Adjust Apply FS – 1.5 LSB to the analog input and adjust the GAIN ADJUST pot until the LSB (Bit 8) output just flickers between 0 and 1 with all other bits at 1.

COMPONENT VALUES					
INPUT RANGE	TP_1	TP_2	R_1	R_2	R_3
+5V	5k	1M	5.6k	8.2k	680k
+10V	10k	1M	11k	5.6k	680k

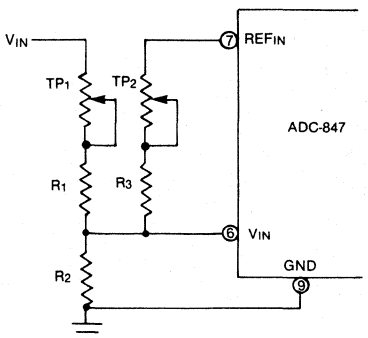
BIPOLAR

Offset Adjust Apply – (FS – .5 LSB) to the analog input and adjust the OFFSET ADJUST pot until the LSB (Bit 8) output just flickers between 0 and 1 with all other bits at 0.

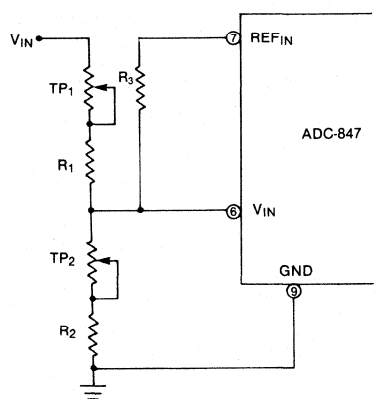
Gain Adjust Apply + (FS – 1.5 LSB) to the analog input and adjust the GAIN ADJUST pot until the LSB (Bit 8) just flickers between 0 and 1 with all other bits at 1.

After gain adjust, repeat offset adjust procedure.

COMPONENT VALUES					
INPUT RANGE	TP_1	TP_2	R_1	R_2	R_3
±5V	5k	5k	13k	13k	7.5k
±10V	10k	5k	27k	8.2k	8.2k



CONNECTION FOR UNIPOLAR OPERATION



CONNECTIONS FOR BIPOLAR OPERATION

ORDERING INFORMATION

MODEL	LINEARITY ERROR	OPERATING TEMP. RANGE	PRICE
ADC-847A	±1 LSB	0°C to +70°C	
ADC-847B	± ¼ LSB	0°C to +70°C	
ADC-847M	± ¼ LSB	–55°C to +125°C	

CODING TABLES

UNIPOLAR

DIGITAL OUTPUT	ANALOG INPUT
11111111	FS-1 LSB
11000000	.75 FS
10000000	.5 FS
01000000	.25 FS
00000000	0

$$1\ LSB = \frac{FS}{256}$$

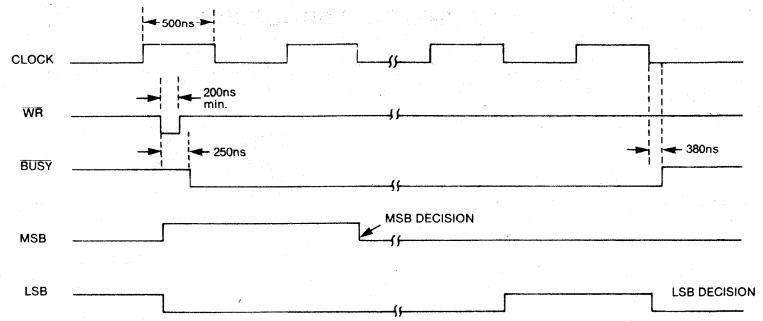
BIPOLAR

DIGITAL OUTPUT	ANALOG INPUT
11111111	+ (FS-1 LSB)
11000000	+ .5 FS
10000000	0
01000000	– .5 FS
00000000	– FS

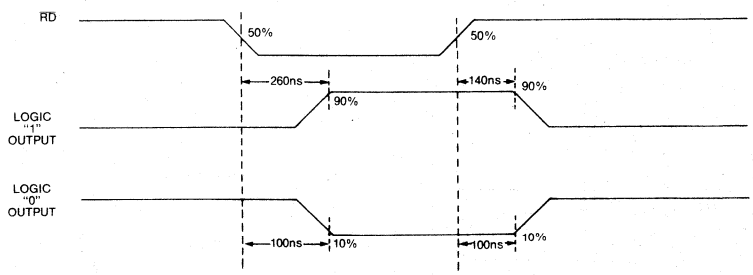
$$1\ LSB = \frac{2\ FS}{256}$$

TIMING AND CONNECTION

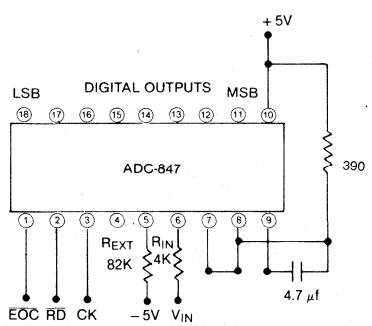
TIMING DIAGRAM



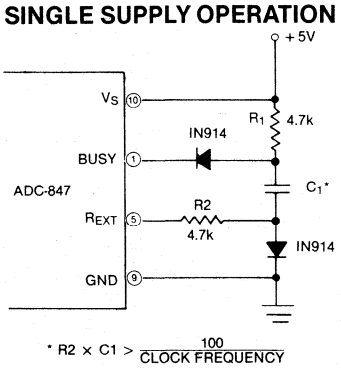
OUTPUT ENABLE/DISABLE DELAYS



TYPICAL CONNECTION



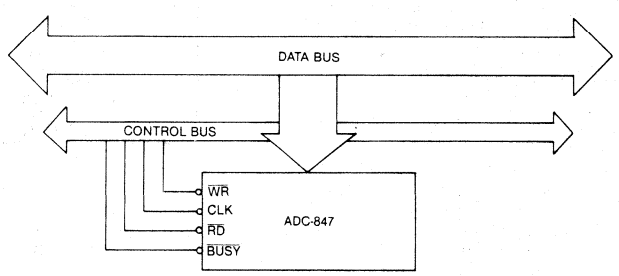
SINGLE SUPPLY OPERATION



* R2 × C1 > $\frac{100}{\text{CLOCK FREQUENCY}}$

Diode Pump circuit to Supply Comparator tail current. See Tech note 8

TYPICAL CONNECTION TO MICROPROCESSOR DATA BUS



The ADC-847 is primarily designed to interface directly to a microprocessor via three-state outputs. The device appears as a memory location or I/O peripheral to the microprocessor thus requiring a minimum of external interface logic.

Monolithic 10 Bit Tracking A/D Converter ADC-856

FEATURES

- **Continuous Tracking Operation**
- **10^6 Conversions/sec**
- **10 Bit Resolution**
- **Monotonic Over Temperature**
- **Controllable Outputs**
- **TTL/CMOS Compatible**

GENERAL DESCRIPTION

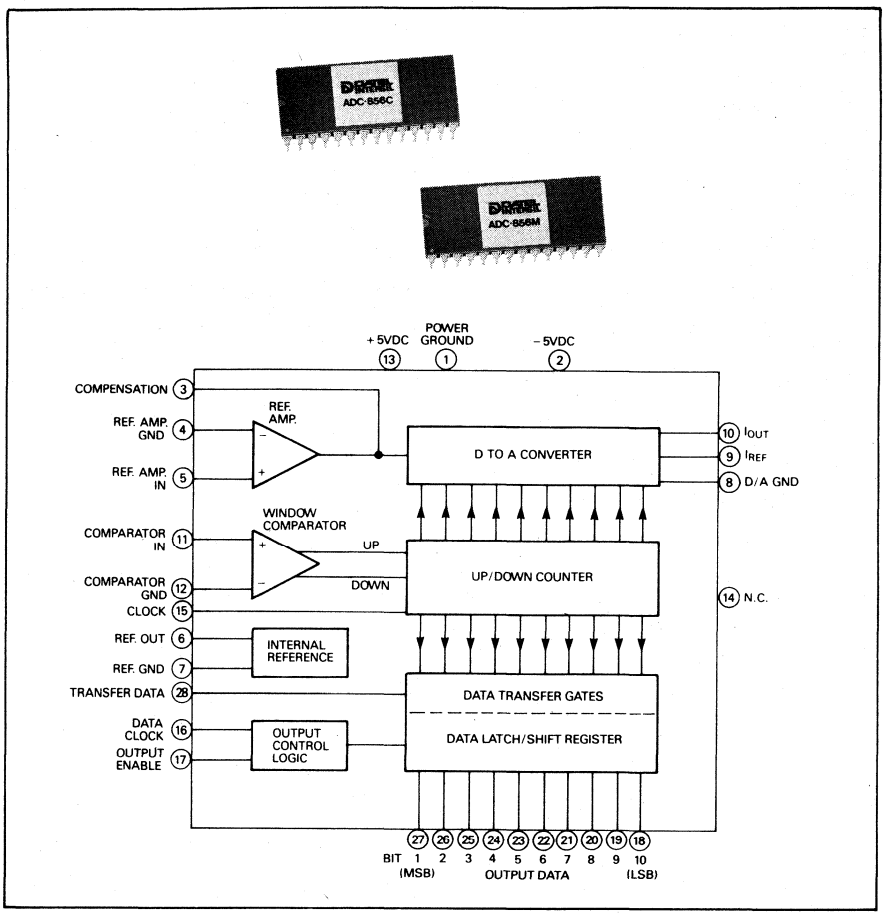
The ADC-856 is a 10 bit tracking A/D converter, capable of supplying continuously updated conversion data on full scale sinusoidal signals up to 300 Hz without the need for a sample and hold. This converter is linear to ±½ LSB min. and is monotonic over its operating temperature range. A number of innovative features give this device the flexibility for a wide range of applications.

The circuit is implemented in bipolar, monolithic form. The chip contains a fast window comparator, tracking logic, an up/down counter, a D/A converter, a precision voltage reference with amplifier, data transfer gates, and a data latch/shift register. The external parts required for operation have been held to a few passive components, and allow external programming of the analog input voltage range. Gain temperature coefficient of the circuit is ±10 ppm/°C, exclusive of reference.

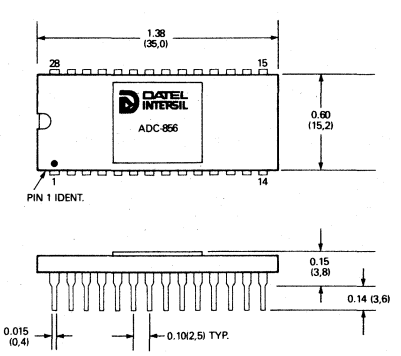
The ADC-856 is optimized for operation in a continuous tracking mode. In this conversion technique each conversion of an analog signal is based on the last converted value of that signal. For signals that do not vary faster than the converter can track, or 1 LSB/μsec, continuous tracking will provide a valid, updated conversion result every microsecond.

Logic control inputs contribute to this device's usefulness in many different applications. The data transfer gates allow selection of the rate at which the output latch/shift register is updated. The rate may vary from once every microsecond to updating only upon receipt of a command from an external controller. External control also allows selection of output data form, which may be parallel or serial (by supplying an optional clock input). The outputs may be disabled completely in either mode by holding the output enable input low.

The ADC-856 operates on ±5 VDC power at 50 mA with a power supply rejection of 0.1%/V. The device is packaged in a 28 ceramic DIP and is available in two operating temperature ranges: 0°C to +70°C and −55°C to +125°C.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER GROUND	15	CLOCK
2	−5VDC	16	DATA CLOCK
3	COMPENSATION	17	OUTPUT ENABLE
4	REF. AMP. GND.	18	BIT 10 OUT (LSB)
5	REF. AMP. IN	19	BIT 9 OUT
6	REF. OUT	20	BIT 8 OUT
7	REF. GND.	21	BIT 7 OUT
8	D/A GND.	22	BIT 6 OUT
9	I_{REF}	23	BIT 5 OUT
10	I_{OUT}	24	BIT 4 OUT
11	COMPARATOR IN	25	BIT 3 OUT
12	COMPARATOR GND.	26	BIT 2 OUT
13	+5VDC	27	BIT 1 OUT* (MSB)
14	N.C.	28	TRANSFER DATA

*Serial data output when in serial data mode

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS ADC-856
Typical at 25° C, ±5V Supply and Internal Reference, unless otherwise noted

MAXIMUM RATINGS	
Supply Voltage	±7 Volts
Logic Input Voltage	0V to $+V_{CC}$
PERFORMANCE	
Resolution	10 Bits
Linearity Error	±½ LSB max.
Differential Linearity Error	±½ LSB
No Missing Codes	Over Oper. Temp. Range
Conversion Time, 1 LSB change	1 μsec.
Conversion Time, Full Scale Change	1.024 msec[1]
Tracking Speed	1 LSB/μsec max.
Tracking Bandwidth, Full Scale	300 Hz[2]
Gain Tempco	10 ppm/° C[4]
Zero Tempco	7 ppm/° C of FSR[6]
Power Supply Rejection[4]	0.1%/V
INPUTS	
Analog Input Range[7]**, Unipolar**	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V
Reference Current	1 mA ±0.2 mA
Input Logic Level, HI ("1")	+2.0V min @ 50 μA[3]
Input Logic Level, LO ("0")	+0.8V max. @ 1 μA[3]
Clock Pulse Width	100 nsec. min.
Clock Rate	1 MHz max.
Data Transfer Input	Hold HI for 50 nsec. min. to load output latches
Output Enable Input	When LO, disables data clock and turns outputs off (HI)
Data Clock Input	When driven by clock at ≤ 1MHz with min. pulse width of 100 nsec., provides serial data ouput at Pin 27.
OUTPUTS	
Reference Voltage	2.48V ±1.5%
Reference Tempco	40 ppm/° C
Reference Load Current, max.	4 mA
D/A Output Current, Full Scale	4 mA[5]
Data Output	Parallel or Serial
Output Logic Level, HI ("1")	+2.4V min. @ −40 μA
Output Logic Level, LO ("0")	+0.4V max. @ 1.6 mA
Coding, Unipolar	Straight Binary
Coding, Bipolar	Offset Binary
POWER REQUIREMENT	
Supply Voltage Range	±4.5V to ±5.5V
Supply Current	50 mA
Power Consumption	500 mW
Operating Temperature Range	
ADC-856C	0° C to +70° C
ADC-856M	−55° C to +125° C
Storage Temperature Range	−55° C to +125° C
Package	28 Pin Ceramic DIP

NOTES:

1. Conversion time is directly dependent on the magnitude of input signal change.
2. Tracking bandwidth is inversely proportional to input signal amplitude, e.g. at half scale bandwidth is 600 Hz.
3. $V_S = \pm 5.5V$
4. Exclusive of Reference.
5. The Full Scale D/A Output Current is 4 Times I_{REF}.
6. FSR is Full Scale Range, the difference between maximum and minimum inputs.
7. Analog input range is programmed by an external resistor.

TECHNICAL NOTES

1. The transfer of conversion data to the outputs is controlled by the transfer gates. When TRANSFER DATA is held high the outputs update with each conversion. To update the outputs upon command, TRANSFER DATA is taken high for a maximum of 50 nsec., no sooner than 150 nsec. after the active (negative going) edge of the main clock. TRANSFER DATA must go low before the next main clock edge. When TRANSFER DATA is low, the data is held in the output register.

2. Conversion data appears at the outputs in parallel form. Data may be obtained in serial form by clocking DATA CLOCK at up to 1 MHz, with a minimum pulse width of 100 nsec and TRANSFER DATA low. Serial output data (MSB first) is then available at pin 27.

3. When OUTPUT ENABLE is taken low DATA CLOCK is disabled and all output transistors are turned off (all bit outputs go high).

4. The converter tracks the input signal level at a speed of 1 LSB/μsec; thus the conversion time for any input signal change is given by

$$\frac{\Delta V_{IN}}{1\ LSB} = \text{conversion time in } \mu\text{sec}$$

5. Full Scale D/A output current is four times the reference current; for optimum performance the reference current should be 1 mA. An external reference can be used which can range from .8 mA to 1.2 mA.

6. The tracking bandwidth is inversely proportional to the amplitude of the input signal, e.g., at half scale the bandwidth is 600 Hz.

7. The window comparator and tracking logic determine whether the up/down counter will count up/count down or retain the same value on the negative going edge of the clock pulse.

8. Since the gain tempco of the converter is typically 10 ppm/° C, it is recommended that 10 ppm/° C metal film resistors be used for R_3, R_4 and R_5 for best performance over temperature. The internal reference will typically add 40 ppm/° C to the gain tempco. For improved performance a high quality external reference should be used.

9. R_1 and R_2 compensate for the input bias currents of the reference amplifier and comparator whose inputs are at virtual ground. Thus $R_1 = R_3$ and R_2 = the parallel combination of R_4, R_5 and R_6. The parallel combination of R_4, R_5 and R_6 should be as close to 625Ω as possible as this determines the D/A settling time and therefore conversion time. Refer to the resistor tables for a list of typical values for these resistors.

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	PRICE (1-24)
ADC-856C	0° C to +70° C	
ADC-856M	−55° C to +125° C	

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

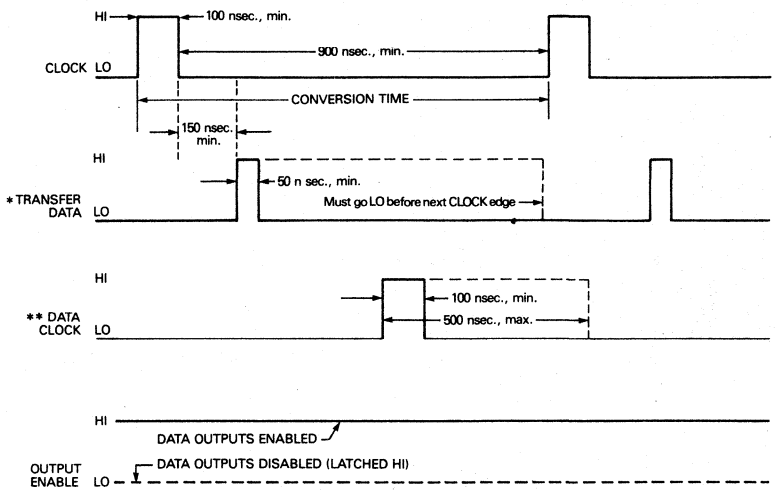
THEORY OF OPERATION

The ADC-856 converters employ a tracking conversion technique. Tracking converters are most effectively used in single channel operations on a continuous signal. In this technique each conversion is based on the previous conversion value. A fast window comparator determines whether an up/down counter increments by 1 LSB, decrements by 1 LSB or remains at its last value. The digital word in the counter controls a D/A converter with a precision reference; the analog output goes to the comparator and is compared with the analog input signal.

For signals with a rate of change less than the converter's maximum rate of change (tracking speed), each comparison represents a valid conversion and the converter is therefore tracking the signal. Tracking is not possible when the input signal varies at a rate greater than the converter's maximum or is discontinuous, as in multiplexed applications. In these cases the converter will change at its maximum rate (1 LSB/μsec) until it attains the new signal level. While this acquisition is in progress, each converter step is available to the output as data, even though it does not yet represent the input signal level. The time required to acquire a new signal level is directly proportional to its difference from the previous level; for a full scale change this period is over 1 msec. Allowance should be made for the acquisition time when a rapid signal change is introduced.

APPLICATIONS

TIMING DIAGRAM



*IF TRANSFER DATA IS HELD HI, THEN THE COUNTER OUTPUTS APPEAR DIRECTLY AT THE BIT OUTPUTS.

**DRIVEN FOR SERIAL DATA OUTPUT ONLY

CODING TABLES

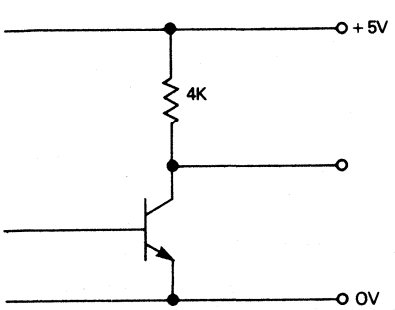
UNIPOLAR OPERATION STRAIGHT BINARY

SCALE	CODE
+FS −1 LSB	1111111111
+¾ FS	1100000000
+½ FS	1000000000
+¼ FS	0100000000
+1 LSB	0000000001
0	0000000000

BIPOLAR OPERATION OFFSET BINARY

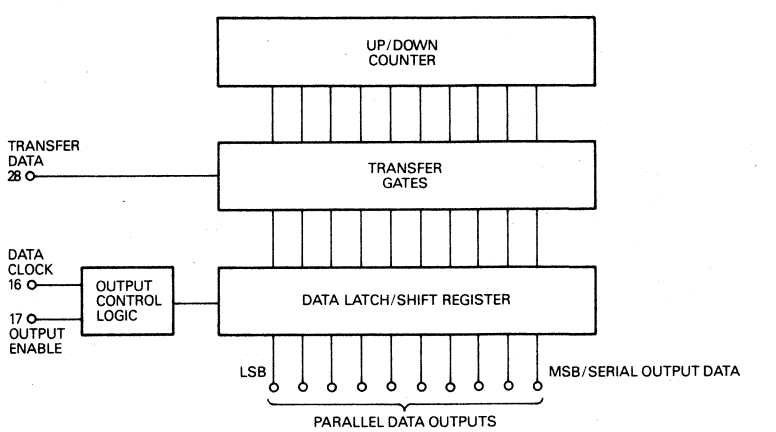
SCALE	CODE
+FS −1 LSB	1111111111
+½ FS	1100000000
+1 LSB	1000000001
0	1000000000
−1 LSB	0111111111
−½ FS	0100000000
−FS + 1 LSB	0000000001
−FS	0000000000

BIT OUTPUT DIAGRAM



IF OUTPUT ENABLE IS LO ALL OUTPUTS TRANSISTORS ARE TURNED OFF AND ALL BIT OUTPUTS ARE HI.

OUTPUT LOGIC CONTROL



TRANSFER DATA (PIN 28)

HI: Min. 50 nsec pulse transfers parallel data from the up/down counter to the data latch/shift register. May be held high for continuous data transfer

LO: Data in latches held, new data from counter not transferred to data latches

DATA CLOCK (PIN 16)

HI: Clocked at up to 1 MHz for serial data output at Pin 27, MSB first

LO: Output data in parallel format at pins 18-27

OUTPUT ENABLE (PIN 17)

HI: Data available at outputs (parallel or serial)

LO: Output transistors turned OFF, all data outputs latched HI

CONNECTION AND CALIBRATION

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram. Note that Pin 6 is connected to R_3 and R_4 only when the internal reference is used (dotted line on diagram).
2. Select R_1 through R_6 from values given in the resistor table or calculate from the equations that accompany it.
3. Drive the MAIN CLOCK input (Pin 15) with a compatible clock signal at up to 1 MHz and apply a logic HI to TRANSFER DATA (Pin 28).

UNIPOLAR OPERATION

Zero and Gain Adjustments

1. Apply an analog input voltage of zero +½ LSB.
2. Adjust the zero adjustment so that the output code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of +F.S. −1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

BIPOLAR OPERATION

Offset and Gain Adjustments

1. Apply an analog input voltage of −F.S. +½ LSB.
2. Adjust the offset adjustment (R_4) so that the output code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of +F.S. −1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

CALIBRATION RESISTOR VALUES

R_4 adjusts the offset for bipolar operations; in unipolar operations R_4 is replaced with a zero adjustment circuit shown in applications. In either mode R_3 adjusts the gain. If the predicted values of these resistors do not supply the transition points expected, their values should be recalculated. Each may be trimmed with a 100 ppm/°C trimming pot used in series with the resistor. The trim pots should be constrained to approximately 1% of the nominal value calculated.

The values of R_1 through R_6 are calculated from the following:

*$R_1 = R_3$ *R_2 = the parallel combination of R_4, R_5 and R_6.

$$R_3 = \frac{V_{REF}}{1.0\ mA} \qquad R_4 = \frac{-V_{REF} R_5}{V_{IN}min}$$

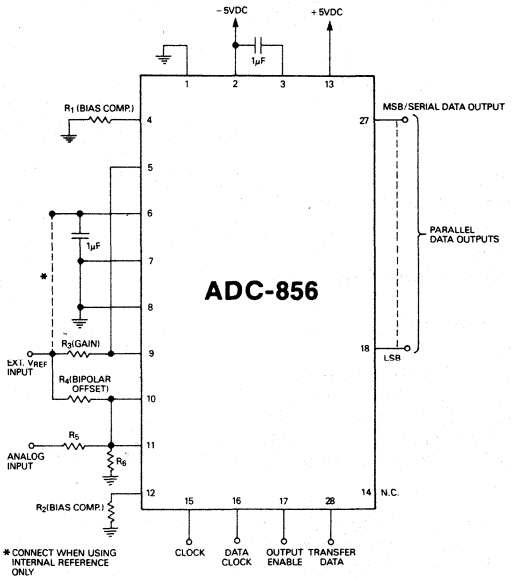
$$R_5 = \frac{FSR^{**}}{I_{OUT}(max)}$$

*R_6 is chosen so that the parallel combination of R_4, R_5 and R_6 is approximately 625Ω, this determines the D/A time constant and hence conversion time.

*The nearest preferred value may be used for these resistors.

**F.S.R. is Full Scale Range, the difference between maximum input voltage and minimum input voltage.

CONNECTION & CALIBRATION DIAGRAM

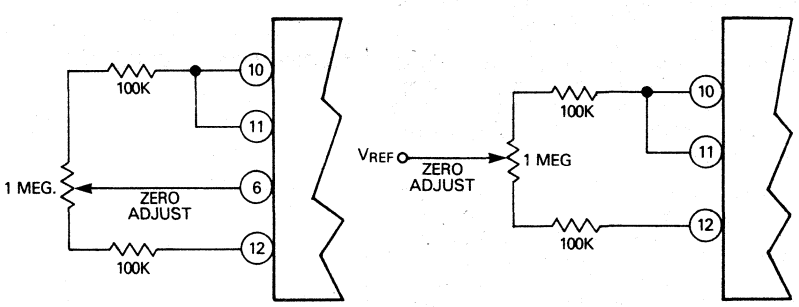


RESISTOR TABLES

ANALOG INPUT RANGE	V_{REF}[2]	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
0 to +2.5V	2.5V	2.5K	625Ω	2.5K	∞	625Ω	∞
0 to +5.0V	2.5V	2.5K	625Ω	2.5K	∞	1.25K	1.25K
±2.5V	2.5V	2.5K	625Ω	2.5K	1.25K	1.25K	∞
0 to +10V	2.5V	2.5K	625Ω	2.5K	∞	2.5K	835Ω
±5V	2.5V	2.5K	625Ω	2.5K	1.25K	2.5K	2.5K
±10V	2.5V	2.5K	625Ω	2.5K	1.25K	5K	1.67K

NOTES: 1. The nearest preferred value may be used for R_1, R_2 and R_6.
2. For external reference set $R_1 = V_{REF}$ (Kohms)

UNIPOLAR ZERO



FOR UNIPOLAR OPERATION WHERE R_4 APPROACHES ∞ AND A ZERO ADJUSTMENT IS REQUIRED, THIS CIRCUIT MAY BE USED TO REPLACE R_4

NEW

DATEL

Ultra High Speed 12 Bit Modular A/D Converter ADC-868

PRELIMINARY

FEATURES

- 12 Bit Resolution
- 500 nsec (max) Conversion Time
- 3– State Output
- ± ½ LSB Linearity
- On Board Offset & Gain Adjustments

GENERAL DESCRIPTION

DATEL-INTERSIL's ADC-868 is an ultra-high speed, 12 bit, modular A/D converter. With a conversion time of 500 nsec maximum, over the 0°C to + 70°C temperature range no missing codes is guaranteed.

Standard input ranges are 0V to + 5V for unipolar operation and ± 2.5V for bipolar operation. Extended input ranges of 0V to + 10V and ± 5V can be implemented by the addition of 2 external resistors. A low input impedance of 1K allows for maximum speed applications with low impedance sources such as a sample and hold amplifier.

Output data is available through a 3-state output register, as 12 parallel lines with 2 enable inputs providing accurate data transferal. Data is coded as straight binary for unipolar operation and offset binary for bipolar operation.

The ADC-868 is comprised of a fast settling precision input buffer, flash converter, high speed DAC, high speed comparator, precision voltage reference, clock generator and control logic circuits, requiring few external components with offset and gain adjustments on board.

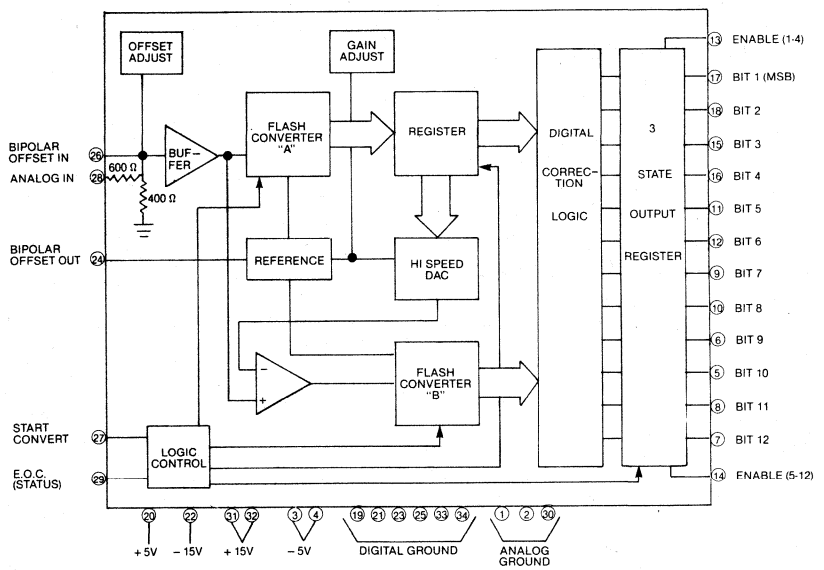
Excellent specifications include a maximum tempco at ± 30 ppm/°C, output enable delay of 28 nsec, maximum, a conversion rate of 2 MHz and guaranteed monotonicity.

The combined use of a high speed A/D with "state-of-the-art" flash conversion techniques, makes the ADC-868 an ideal selection for high speed data acquisition, real time waveform analysis, radar signal processing and analytic instrumentation.

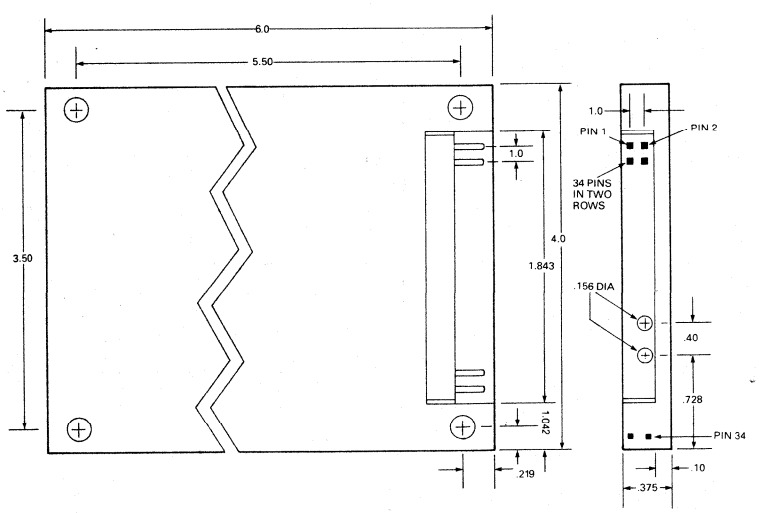
This module is packaged in a 4 × 6 × .375 inch black enameled CR steel case with a 34 pin male connector located at one end.

Power requirements are ± 15 VDC and ± 5 VDC with a total current drain of 1120 mA, max.

BLOCK DIAGRAM



MECHANICAL DIMENSIONS



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS — ADC-868
Typical at 25°C, ± 15V and ± 5V supplies, unless otherwise noted.

	MIN.	TYP.	MAX.
MAXIMUM RATINGS			
Positive Supply		+ 16 VDC	
Negative Supply		− 16 VDC	
Logic Supply		± 7 VDC	
Logic Inputs		+ 5.5V	
Analog Inputs		± 6.25V	
ANALOG INPUTS[1]			
Unipolar		0V to + 5V	
Bipolar		± 2.5V	
Impedance		1 kΩ (with pin 26 grounded)	1.01 KΩ
DIGITAL INPUTS			
Start Conversion		A 2V (min) to 5V (max) positive pulse with a 50 nsec (min) duration. Positive going edge intitiates conversion	
Loading		2 TTL Loads	
Enable 1-4		Logic low "0" enables bits 1 (MSB) thru 4	
Enable 5-12		Logic low "0" enables bits 5 thru 12 (LSB)	
Loading		1 TTL Load	
OUPUTS			
Unipolar Coding		Straight Binary	
Bipolar Coding		Offset Binary	
Output Data		12 Parallel lines	
End of Conversion		2V (min) to 5V (max) positive going pulse, 500 nsec (max) width. Negative going edge indicates conversion complete.	
Loading		10 TTL Loads	
Output Logic Levels (enable lines low)			
Vout "0"		+ 0.25V	+ 0.4V
Vout "1"	+ 2.4V	+ 3.1V	
Loading		7 TTL Loads	
PERFORMANCE			
Resolution			12-bits
Conversion Time		450 nsec	500 nsec
Conversion Rate			2 MHz
Differential Linearity Error			± ½ LSB
No Missing Codes		0°C to + 70°C	
Gain Tempco			± 30 ppm/°C
Zero Drift			± 100 µV/°C
Offset Tempco			± 15 ppm/°C
Long Term Stability			± 0.25%/year
Output Enable Delay		20 nsec	28 nsec
POWER SUPPLY SENSITIVITY			
± 15 VDC			± 0.01%/% Supply
± 5 VDC			± 0.01%/% Supply
POWER REQUIREMENTS			
Supply Voltage: Analog	± 14.5 VDC	± 15 VDC	± 18 VDC
Logic	± 4.75 VDC	± 5 VDC	± 5.5 VDC
Supply Current: + 15V			210 mA
− 15V			150 mA
+ 5V			500 mA
− 5V			260 mA
Power Dissipation			9.5 watts
PHYSICAL-ENVIRONMENTAL			
Operating Temperature		0°C to + 70°C	
Storage Temperature		− 25°C to + 85°C	
M.T.B.F.		> 125,000 hrs.	
Package Type		4 × 6 × .375 inch black enameled 25 gauge CR steel, with a 34 pin male connector at one end.	

NOTES:
1. See Technical Note #1 for extended input ranges.

TECHNICAL NOTES

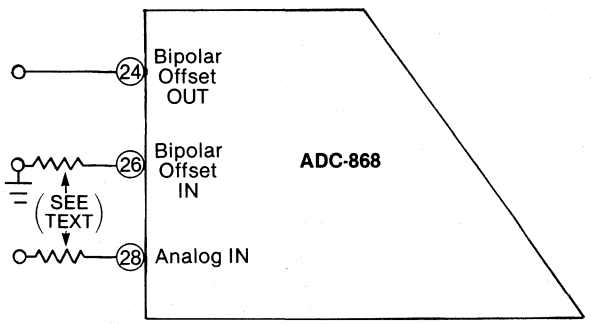
1. Analog input ranges may be extended to 0V to + 10V unipolar and ± 5V bipolar by the addition of two precision resistors. See EXTENDED INPUT CONFIGURATION.
2. The high operating speed of these converters requires that good high frequency board layout techniques be used.
   Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference and digital crosstalk.
3. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL-INTERSIL's model SHM-4860, a high-speed hybrid unit featuring 200 nS acquisition time to 0.1% accuracy. See SAMPLE—HOLD DIAGRAM.
4. These converters have a maximum power dissipation of 9.5W. The case-to-ambient thermal resistance for this package is approximately 40°C max. For operation in ambient temperatures exceeding 70°C (EX-, EXX-HS models only), care must be taken to ensure free air circulation in the vicinity of the converter.
5. For TTL operation, tie both enable inputs to digital ground.
6. Logic and analog supply lines are internally bypassed so that external bypass capacitors are not necessary.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG GROUND	18	BIT 2
2	ANALOG GROUND	19	DIGITAL GROUND
3	− 5 VDC	20	+ 15 VDC
4	− 5 VDC	21	DIGITAL GROUND
5	BIT 10	22	− 15 VDC
6	BIT 9	23	DIGITAL GROUND
7	BIT 12 (LSB)	24	BIPOLAR OFFSET OUT
8	BIT 11	25	DIGITAL GROUND
9	BIT 7	26	BIPOLAR OFFSET IN
10	BIT 8	27	START CONVERT
11	BIT 5	28	ANALOG IN
12	BIT 6	29	E.O.C. (STATUS)
13	ENABLE BITS 1-4	30	ANALOG GROUND
14	ENABLE BITS 5-12	31	+ 5 VDC
15	BIT 3	32	+ 5 VDC
16	BIT 4	33	DIGITAL GROUND
17	BIT 1 (MSB)	34	DIGITAL GROUND

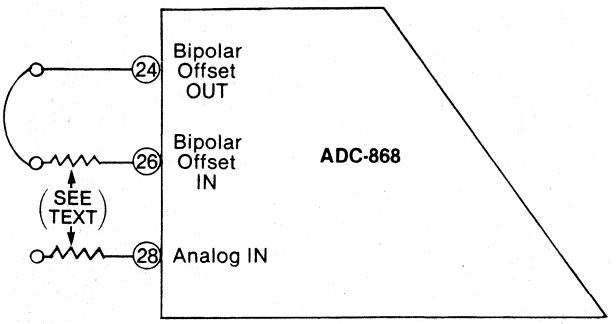
EXTENDED INPUT CONFIGURATION

UNIPOLAR



Extended Input
Unipolar Configuration

BIPOLAR



Extended Input
Bipolar Configuration

An extended unipolar input range of 0 to 10V can be achieved by the termination of the bipolar OFFSET IN (pin 26) to ground through a 1.02 kΩ, .1% resistor and connecting a 1.10 kΩ, .1% resistor in series with the ANALOG IN (pin 28).

An extended bipolar input range of ±5V can be attained by strapping the bipolar OFFSET OUT (pin 24) to the bipolar OFFSET IN (pin 26) through a 1.02 kΩ, .1% resistor and connecting a 1.10 kΩ, 1% resistor in series with the ANALOG IN (pin 28).

GAIN AND OFFSET ADJUSTMENTS

UNIPOLAR OPERATION (For extended input range operation, see EXTENDED INPUT CONFIGURATION)

1. Apply start convert pulses to pin 27. (Pin 26 grounded)
2. Connect a precision voltage reference of + ½ LSB (+ 0.61 mV or + 1.22 mV for extended input range operation) to the analog input. Adjust the offset potentiometer so that the LSB is flickering at 0000 0000 000X.
3. Connect a precision voltage reference of + F.S. – 1½ LSB (+ 4.9982V or + 6.34V for extended range input operation) to the analog input. Adjust the gain potentiometer so that the LSB is flickering at 1111 1111 111X.

BIPOLAR OPERATION (For extended input range operation, see EXTENDED INPUT CONFIGURATION)

1. Apply START CONVERT PULSES to Pin 27. (Pin 26 connected to Pin 24).
2. Connect a precision voltage reference of – F.S. + ½ LSB (– 2.4994V or – 4.9988V for extended input range operation) to the analog input. Adjust the offset potentiometer so that the LSB is flickering at 0000 0000 000X.
3. Connect a precision voltage reference of + FS – 1½ LSB (+ 2.4982V or + 4.9963V for extended input range operation) to the analog input. Adjust the gain potentiometer so that the LSB is flickering at 1111 1111 111X.

OUTPUT CODING

UNIPOLAR SCALE	10V RANGE	5V RANGE	STRAIGHT BINARY
+ FS – 1 LSB	+ 9.9976V	+ 4.9988V	1111 1111 1111
+ ⅞ FS	+ 8.7500V	+ 4.3750V	1110 0000 0000
+ ¾ FS	+ 7.5000V	+ 3.7500V	1100 0000 0000
+ ½ FS	+ 5.0000V	+ 2.5000V	1000 0000 0000
+ ¼ FS	+ 2.5000V	+ 1.2500V	0100 0000 0000
+ 1 LSB	+ 0.0024V	+ 0.0012V	0000 0000 0001
0	0.0000V	0.0000V	0000 0000 0000

BIPOLAR SCALE	± 5V RANGE	± 2.5V RANGE	OFFSET BINARY
+ FS – 1 LSB	+ 4.9976V	+ 2.4988V	1111 1111 1111
+ ¾ FS	+ 3.7500V	+ 1.8750V	1110 0000 0000
+ ½ FS	+ 2.5000V	+ 1.2500V	1100 0000 0000
0	0.0000V	0.0000V	1000 0000 0000
– ½ FS	– 2.5000V	– 1.2500V	0100 0000 0000
– ¾ FS	– 3.7500V	– 1.8750V	0010 0000 0000
– FS + 1 LSB	– 4.9976V	2.4988V	0000 0000 0001
– FS	– 5.0000V	– 2.5000V	0000 0000 0000

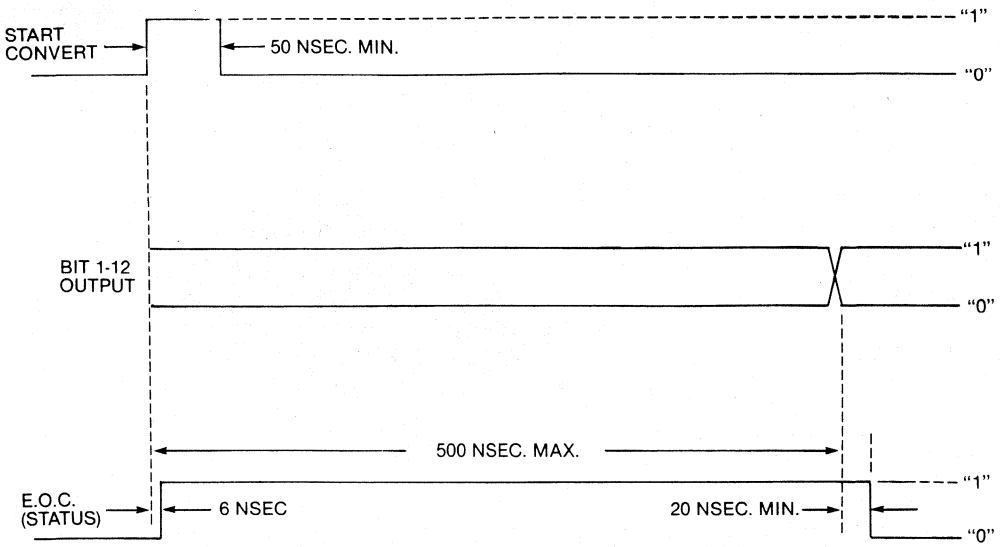
ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-868	500 nsec, 12 bit A/D Converter
Mating Connector	34 Pin AMP #1-86063-3

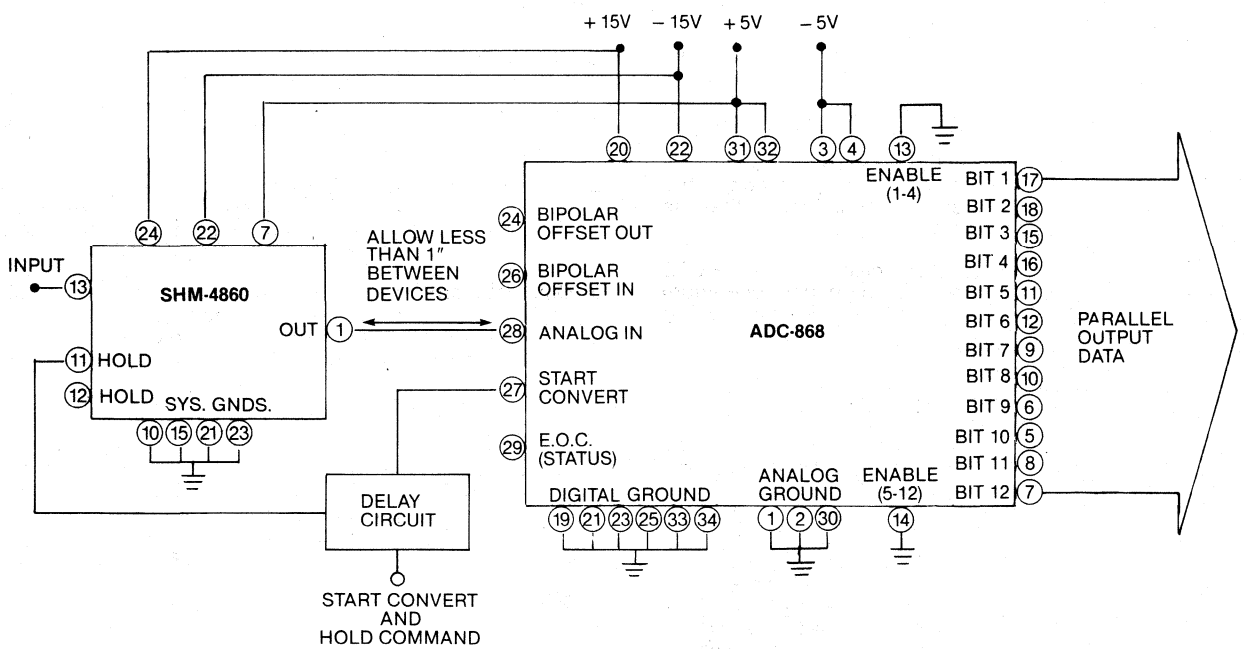
For information on extended temperature range versions, consult factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

ADC-868
TIMING DIAGRAM



ULTRA HIGH SPEED A/D WITH SAMPLE/HOLD



When DATEL's ultra-high speed ADC-868 is used in conjunction with a high speed sample-hold amplifier, such as Datel's SHM-4860, a throughput rate of 1.25 MHz can be achieved.

Ultra-Linear 8 Bit A/D Converter ADC-881

FEATURES

- **8 Bit Resolution**
- **Statistically Linearized Conversion**
- **12½ Bit Linearity**
- **±15V Input Range**
- **1.5 μsec Conversion Time**
- **Out of Range Indication**

GENERAL DESCRIPTION

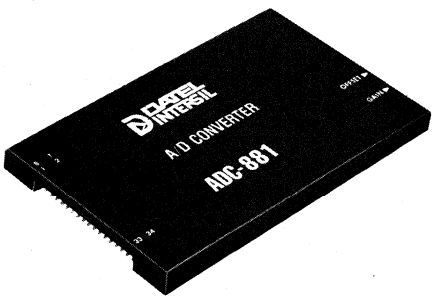
The ADC-881 is an 8 bit analog to digital converter with an internal sample-hold. This converter employs a stochastic distributional technique to enhance the statistical (average) linearity by a factor of 11.2, thus achieving a linearity error of only .0087%. Systematic nonlinearities are scattered in a pseudorandom fashion over the range of the converter, thus appearing as noise rather than nonlinearities. This result is particularly desirable in applications that use the digital output of an A/D converter to compile a histogram. The fundamental properties of any non-distributive A/D converter cause class widths within the histogram to vary from the ideal, thereby artificially increasing or decreasing the frequency within discrete class widths.

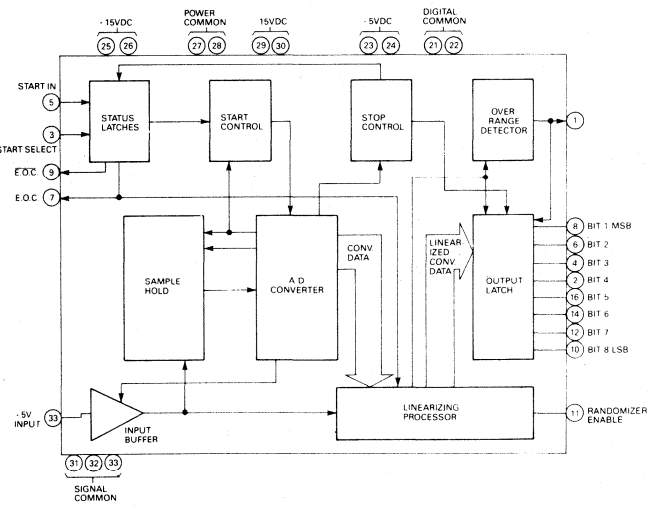
This ultra-linear A/D has a wide range of applications in spectrum analysis, nuclear research, vibration analysis, geological research, sonar digitizing, medical imaging systems, industrial testing and other signal analysis applications.

The ADC-881 has an analog input range of ±5V and will accomplish an eight bit sample and conversion in 1.5 μsec maximum. Output data is coded as offset binary with an over range output to indicate analog values out of the converter's range.

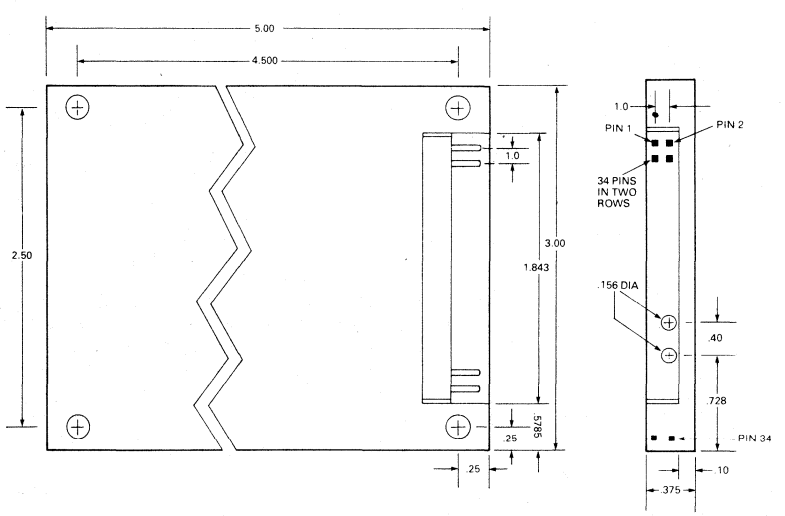
Additional specifications include a gain tempco of 30 ppm/°C maximum, offset tempco of 25 ppm/°C maximum, zero crossing tempco of 10 ppm/°C maximum and long term stability of ±0.02%/year.

Each converter is a functionally complete unit requiring only ±15 Vdc and +5V power supplies for operation. The device is packaged in a compact 5" x 3" x 0.375" black enameled steel module. For information on extended temperature range versions contact the factory.





MECHANICAL DIMENSIONS INCHES



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

PRELIMINARY SPECIFICATIONS, ADC-881

(Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted)

MAXIMUM RATINGS

Positive Supply	+18V
Negative Supply	−18V
Logic Supply	+7V
Digital Supply	+5.5V

INPUTS

Analog Input Range	±5V
Analog Input Impedance	14 KΩ
Start Conversion	A pulse[1] 20 nsec to 80 nsec duration with rise and fall times less than 10 nsec. Logic "0" = 0V to +0.8V. Logic "1" +2.0 to +5.5V. Conversion commences on the leading edge of the pulse. Loading: 1 LSTTL load.
Start Select	For positive start input pulses, set Start Select to a Logic "1". For negative start input pulses, set Start Select to a Logic "0" or ground.
Randomizer Reset	Hold high for randomizing operations[2]

OUTPUTS

Parallel Output Data	8 parallel latched data lines - 8 bits binary. V out "0"≤+0.4V, V out "1"≥+2.4V. Loading: 5TTL loads
Coding	Offset Binary
EOC	Conversion Status Signal: High (V out "1" ≥+2.4V) from 32 nsec typical after leading edge of Start Convert to 14 nsec typical after all data outputs are valid. V out "0"≤+0.4V. Loading: 5 TTL loads.
$\overline{\text{EOC}}$	Conversion Status Signal. Complement of $\overline{\text{EOC}}$. Loading: 5 TTL loads
$\overline{\text{Over Range}}$[3]	Out of Range Signal. High (Vout "1"≥+2.4V) for all Signal Input values within ±5V, Low (V out "0"≤+0.4V for all Signal Input values beyond ±5V.

PERFORMANCE

Conversion time[4], max.	1.5 μsec
Resolution	8 Bits
Integral Linearity Error[4]	0.0087% of FSR
Differential Linearity Error[5]	0.0087% of FSR
Noise (RMS)[6]	0.2% of FSR
Gain Error	Adjustable to zero
Offset Error	Adjustable to zero
Gain Tempco, max.	±30 ppm of FSR/°C
Offset Tempco, max.	±25 ppm of FSR/°C
Zero Crossing Tempco, max.	±10 ppm of FSR/<C
Long Term Stability	±0.02% / year

POWER REQUIREMENTS

Analog Supply	+15V ± 0.5V @ 130mA max. −15V ± 0.5V @ 148mA max.
Logic Supply	+5V ±0.25V @ 481mA max.
Power Dissipation, max.	6.58 Watts.

PHYSICAL ENVIRONMENTAL

Operating Temperature Range	
ADC-881	0°C to +70°C
ADC-881-EX	−25°C to +85°C
ADC-881-EXX-HS	−25°C to +85°C Hermetic Sealed Semiconductors
Storage Temperature Range	−55°C to +125°C
Package Type	Black enameled 25 gauge CR steel. 5 × 3 × 0.375 in. (127 × 76 × 10mm).
Weight	6.5 oz. (184g).
Connector	.025" square pins, gold plated phosphor bronze. Mating connector — supplied — is similar to AMP # 1-85930-1.

NOTES:

1. An alternate method for generating Start Input pulses is to drive the Start Input with a rising edge and the Start Select with a falling edge delayed 20 nsec to 80 nsec.
2. Pin 11 should be kept at logic HIGH for normal (randomizing) operation. A LOW state disables the PRSG, this may be used as a PRSG reset, as the PRSG returns to its initial state when disabled.
3. When the Signal Input is less than −5V, the Data Output lines are all "0". When the Signal Input is greater than +5V, the Data Output lines are all "1".
4. Conversion Time is measured from the leading edge of the Start Conversion input to the trailing edge of the $\overline{\text{EOC}}$ output.
5. The Linearity Error is the systematic error which remains after a sufficient number of samples have been averaged to suppress the noise.
6. The RMS noise value is reduced by the second root of the number of samples that have been averaged.

THEORY OF OPERATION

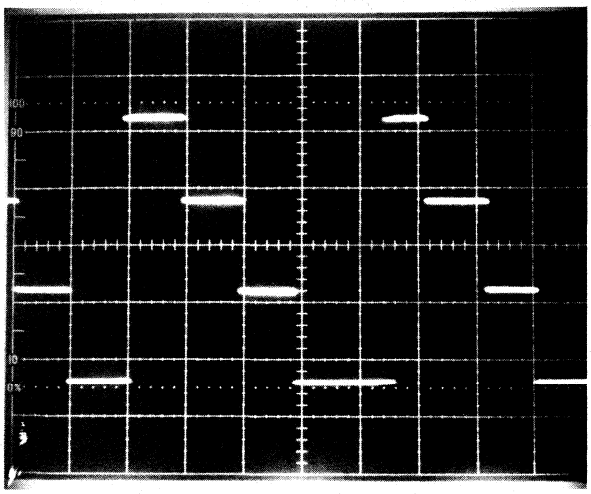


Fig.1 The output of a non-linearized 8 bit A/D converter is shown above. The display shows the 4 least significant bits at the major carry transition, demonstrating differential nonlinearity. This is a property of all non-linearized A/D converters. (The unit used for this example is a typical non-linearized A/D with ±½ LSB of integral linearity and ±½ LSB of differential nonlinearity).

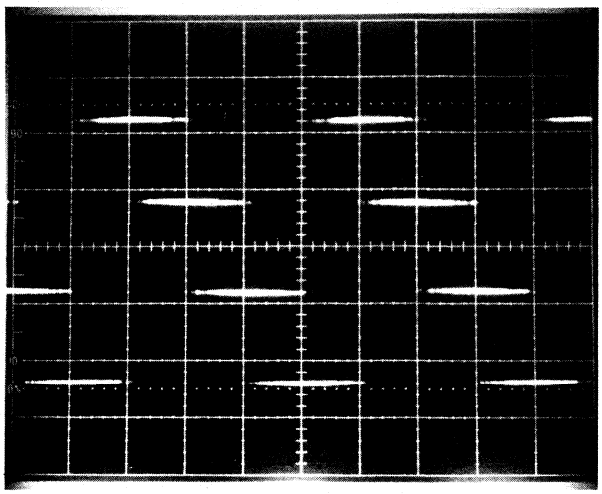


Fig. 2 The output of a linearized 8 bit A/D shown for the 4 least significant bits at the major carry. Notice the improvement in differential nonlinearity. This photo shows the effect of averaging multiple conversions performed with the linearizing technique employed in the ADC-881.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{OVER RANGE}}$	18	Do Not Connect
2	BIT 4	19	Do Not Connect
3	START SELECT	20	Do Not Connect
4	BIT 3	21	Digital Common
5	START in	22	Digital Common
6	BIT 2	23	+5VDC
7	EOC	24	+5VDC
8	BIT 1 (MSB)	25	+15VDC
9	$\overline{\text{EOC}}$	26	+15VDC
10	BIT 8 (MSB)	27	Power Common
11	Random. Enable	28	Power Common
12	BIT 7	29	−15VDC
13	NC	30	−15VDC
14	BIT 6	31	Signal Common
15	NC	32	Signal Common
16	BIT 5	33	Analog Input
17	Do Not Connect	34	Signal Common

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PRICE (I-24)
ADC-881	0 to +70°C	

For information on extended temperature range and high reliability versions of this product, contact factory.

THIS PRODUCT IS COVERED BY GSA CONTRACT.

The ADC-881 employs a statistically linearized conversion technique that yields unique advantages in many applications. This technique uses a fundamental property of all A/D converters, differential nonlinearity, in a pseudo-random distributional technique to yield a converter with an "ideal" transfer function. This technique scatters the effects of systematic nonlinearities over the full range of the A/D in pseudo-random (a random sequency of finite length) fashion. The average transfer function, taken over the full range of the pseudo-random sequence, has extremely good integral linearity and minimal differential non-linearity. The trade-off appears here as "noisy" codes, this is the result of distributing systemic non-linearities over a wide range. Noise may be suppressed by repeated sampling of the data since the average value of true random noise is zero. The RMS noise value of the data is reduced by the second root of the number of samples less one that have been averaged.

Since this converter's extreme linearity is realized in an average transfer function, it follows that averaging a larger number of conversions will improve linearity. This is true, with maximal linearity resulting as an average of all values within the pseudo-random sequence (127 random values). Since the ADC-881 has conversion times of 1.3 μsec typical and 1.5 μsec maximum, this averaging procedure will require between 165 and 191 μsec (127 conversions x conversion time). In applications where repeated sampling is employed to reduce noise, this converter yields optimal linearity when the number of samples averaged is an integral multiple of 127 (this is inherent in the stochastic distributional technique used).

The largest group of applications for this class of converters is in areas in which recurring systematic nonlinearities have an adverse effect on the distribution of acquired data values. This is particularly of interest in situations where data is required to compile a histogram (a frequency distribution of sample data into discrete categories). The effects of converter nonlinearities cause some categories to be artificially "widened" while others are "narrowed", thus increasing and decreasing, respectively, the frequence of occurrence of data values within these categories. This effect causes a non-linearized converter to yield a "converter distorted" histogram. Until now many users had to resort to extensive computational processing of digitized data simply to minimize the effects of "converter distortion". The architecture of the ADC-881 obviates the need for this, allowing statistically valid processing of analog data in real-time. Thus we see that the ADC-881 is ideally suited for applications in spectrum analysis, particle event monitors, fast signal processing, vibration analysis, sonar digitizing, and a whole spectrum of imaging applications, from medical imaging to industrial non-destructive testing.

CONNECTION AND CALIBRATION

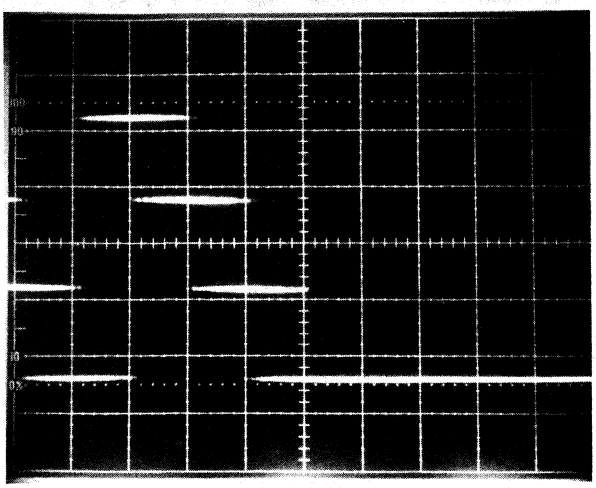


Fig. 3

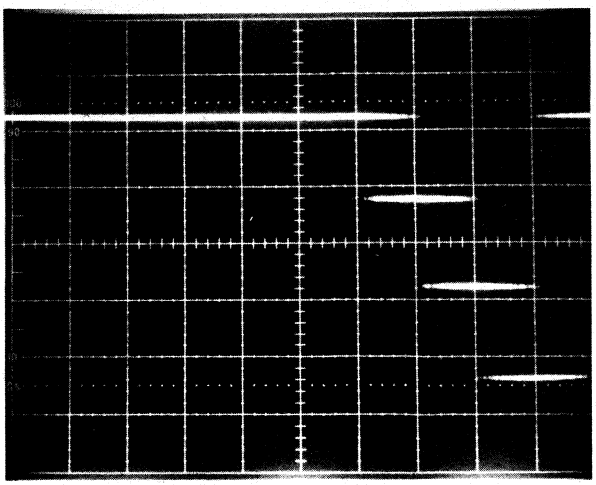
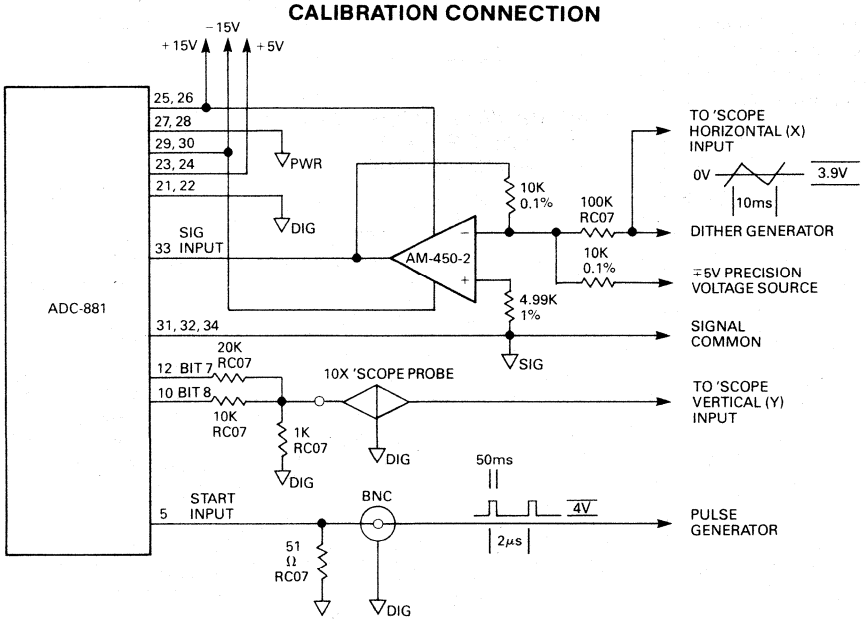


Fig. 4

OFFSET AND GAIN CALIBRATION PROCEDURE

1. Connect A/D to external test circuitry shown in "Calibration Connection" diagram with no power applied.
2. Apply power to the A/D converter and test circuitry and allow them to reach operating temperature.
3. Observe A/D output as a crossplot on the oscilloscope. Calibrate the axis gain for one cm per step and adjust crossplot dither amplitude for 10 cm. Calibrate Y axis for an easily read cross plot.
4. Apply a precision voltage reference set to −5V to the analog input (pin 33). Observe cross plot as shown in figure 3. The last step should be centered on the vertical grid line one cm to the left of center. Adjust offset potentiometer as necessary to achieve this positioning.
5. Set the precision voltage reference to +5V. Observe the cross plot as shown in figure 4. The last step should be centered on the vertical grid line two cm to the right of center. Adjust gain potentiometer as necessary to achieve this position.
6. Repeat steps 4 and 5 until no further adjustment is required. Repetition is necessary, as the offset and gain adjustments interact. The following technique will minimize the number of adjustments. After the initial adjustment outlined in steps 4 and 5, repeat step 4. At this point repeat step 5 but over adjust the gain potentiometer so that the error displayed maintains its initial magnitude but occurs in a direction opposite from its original one, i.e., if the crossplot is 1.5 cm to the left of its desired position, adjust the gain potentiometer so that the crossplot is 1.5 cm to the right of its desired position. Repeat steps 4 and 5, the crossplot should now show perfect position.

CALIBRATION CONNECTION



NEW

DATEL

Adjustment-Free 8 Bit A/D Converter ADC-5101

FEATURES

- 900 nsec Max. Conversion Time
- Adjustment-Free Operation
- Industry Standard Converter
- −55 °C to +125 °C Version
- MIL STD-883B Versions Available

GENERAL DESCRIPTION

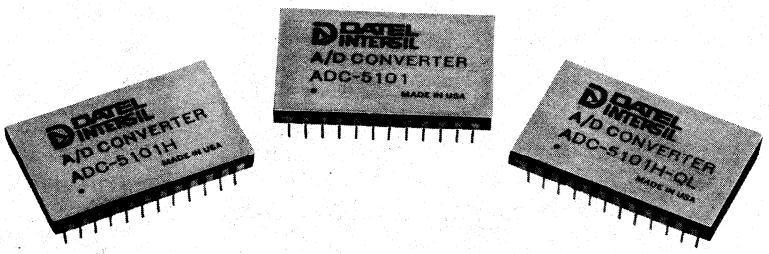
Datel-Intersil's ADC-5101 is a high speed, adjustment-free, 8 bit analog to digital converter. Pin compatible with standard ADC-5101 converters, these devices offer high speed and high accuracy with a full military temperature range version available.

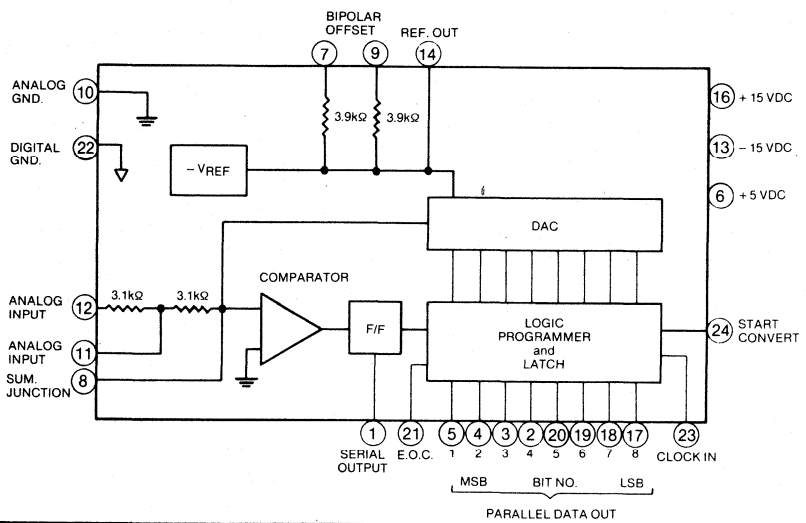
Using the successive approximation method, the ADC-5101 achieves a conversion time of only 900 nsec maximum, making it an ideal choice for high speed, multiplexed data acquisition systems. Active laser trimming of highly stable thin-film resistor networks eliminates the need for external gain or offset adjustments. Overall full scale absolute accuracy is only ± ½ LSB at +25 °C and only ±2 LSB over the full military operating temperture range.

Output coding is straight binary for unipolar operation and offset binary for bipolar operations with both parallel and serial outputs brought out. Digital outputs are TTL compatible and can drive 5 TTL loads. Nine analog input voltage ranges are programmable by external pin connection.

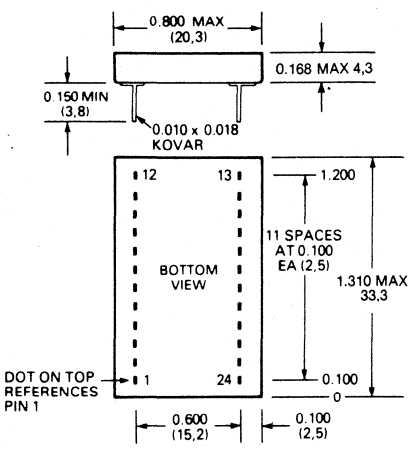
The ADC-5101H is specified for operation over the full military operating temperature range of −55 °C to +125 °C. Versions of this model, screened to MIL STD-883 Class B by Datel-Intersil's stringent QL program, are available. Other models are specified for operation over the commercial, 0 °C to +70 °C, and industrial, −25 °C to +85 °C, operating temperature ranges.

All models require ±15 VDC and +5 VDC for operation and are packaged in a 24 pin, hermetically sealed, ceramic package.





MECHANICAL DIMENSIONS INCHES (MM) 24-PIN CERAMIC



NOTE PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL DATA OUT	13	− 15V POWER
2	BIT 4 OUT	14	REF. OUT
3	BIT 3 OUT	15	N/C
4	BIT 2 OUT	16	+ 15V POWER
5	BIT 1 OUT (MSB)	17	BIT 8 OUT (LSB)
6	+ 5V POWER	18	BIT 7 OUT
7	BIPOLAR OFF.	19	BIT 6 OUT
8	SUM JUNCTION	20	BIT 5 OUT
9	BIPOLAR OFF.	21	E.O.C. (STATUS)
10	ANALOG GND.	22	DIGITAL GND.
11	ANALOG INPUT	23	CLOCK INPUT
12	ANALOG INPUT	24	START CONVERT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617)339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATION, ADC-5101
(Typical at + 25 °C, ± 15 VDC and + 5 VDC supplies, unless otherwise noted)

MAXIMUM RATINGS	
Analog Supply	±0.5V to ±18V
Logic Supply	−0.5V to +7V
Analog Input	±25V
Digital Inputs	−0.5V to +5.5V
INPUTS	
Analog Input Ranges, unipolar	0 to −5V, 0 to −10V, 0 to −20V
	0 to +5V, 0 to +10V, 0 to +20V
bipolar	±2.5V, ±5V, ±10V
Input Impedance, 5V range	1.5 kΩ
10V range	3.0 kΩ
20V range	6.0 kΩ
Input Logic Levels, Logic "1", min.	+2.0V
Logic "0", max.	+0.8V
Start Conversion	Negative going pulse with duration of 25 nsec minimum. Loading:[2] 2 TTL loads
Clock Input, Pulse width High, min.	20 nsec
Pulse width Low, min.	46 nsec.
OUTPUTS	
Parallel Output Data	8 parallel lines of data held until next conversion command.
Output Logic Levels	
Logic "1", min.	+2.4V
Logic "0", max.	+0.4V
Fanout	5 TTL loads
Coding, unipolar	Straight binary
bipolar	Offset binary
Serial Output Data	NRZ successive decision pulses out, MSB first, at the clock frequency.
End of Conversion (E.O.C.)[4]	Conversion Status Signal. Output is high during reset and conversion, LO when conversion is complete
Reference Output, Voltage	−6.4V
PERFORMANCE	
Resolution	8 Bits
Conversion Time, max.	900 nsec
Nonlinearity, max.	± ½ LSB
Differential Nonlinearity, max.	± ½ LSB
Absolute Accuracy, max.[5]	± ½ LSB
Absolute Accuracy vs. temperature	
0 to +70°C, max.	±1 LSB
−25 to +85°C, max.	±1½ LSB
−55 to +125°C, max.	±2 LSB
Reference Output Tempco, max.	5 ppm/°C
Power Supply Rejection	
Positive Supply	±0.01% FSR[6]/% Supply
Negative Supply	±0.03% FSR / % Supply
Logic Supply	±0.01% FSR / % Supply
No Missing Codes	Over operating temperature range
POWER REQUIREMENTS	
Analog Supply, Pin 16	+15V ±0.45V @ 35 mA max.
Pin 13	−15V ±0.45V @ 35 mA max.
Logic Supply, Pin 6	+5V ±0.25V @ 100 mA max.
Power Dissipation, max.	1.55W
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range, ADC-5101	0°C to +70°C
ADC-5101E	−25°C to +85°C
ADC-5101H	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Type	24 pin hermetically sealed ceramic

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for optimimum performance. The analog common (Pin 10) and digital common (Pin 22) are not connected internally and therefore should be connected externally as close to the package as possible. For best results, this common connection should be a large ground plane running under the device package.

2. Both analog and digital supplies should be bypassed to ground with 1.0 μF electrolytic capacitors in parallel with 0.1 μF disc ceramic capacitors. Bypass capacitors should be located directly adjacent to, or on, each supply pin.

3. The absolute accuracy error of an A/D converter is defined as the difference between the theoretical analog input voltage required to produce a given digital output and the unadjusted analog input voltage actually required to produce that same code. Because this error is measured and specified without adjustment, it includes all factors that may effect the devices accuracy at the point of measurement: offset error, linearity error, gain error, and noise error.

4. The ADC-5101 should be driven from low impedance sources capable of high frequency current variations. Datel-Intersil's AM-452, a wide bandwidth, fast settling, monolithic op. amp. is recommended for use as a driving amplifier.

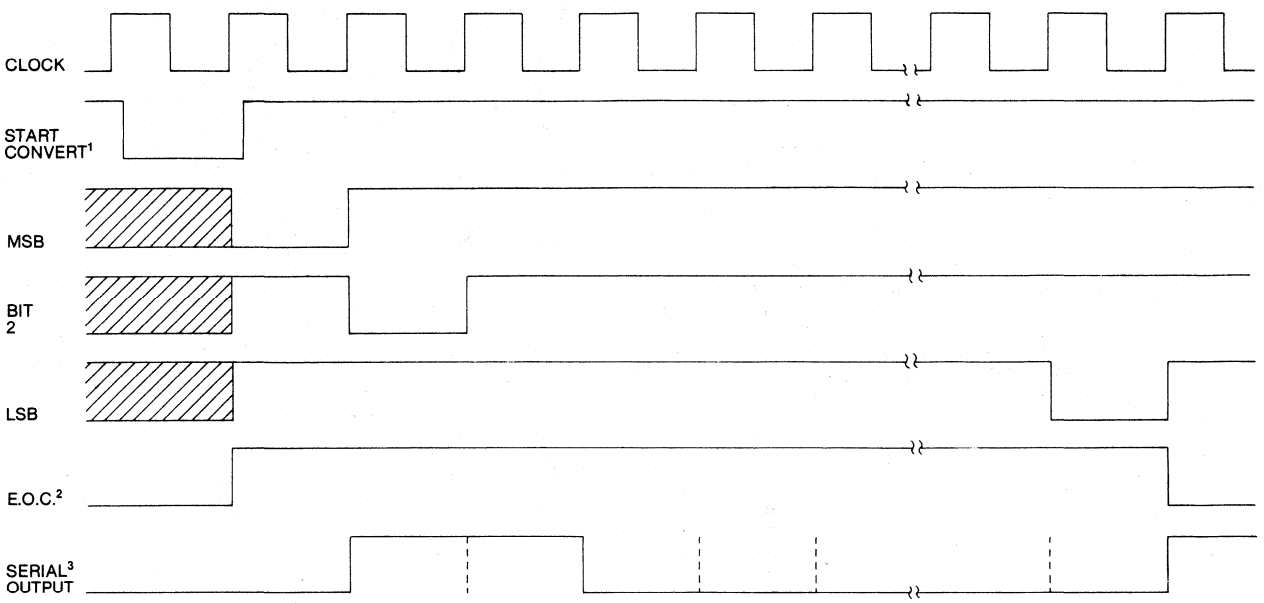
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
ADC-5101	0°C to +70°C	
ADC-5101E	−25°C to +85°C	
ADC-5101H	−55°C to +125°C	

NOTES:
1. Converter will reset on the first edge of the clock after START CONVERT goes low and will convert the MSB on the next rising edge of the clock. If the START CONVERT is held low, the converter will be reset but will not convert the MSB until the first rising edge of clock after the START CONVERT returns high.
2. One TTL load is defined as 40 μA at logic "1" and — 1.6 mA at Logic "0".
3. Clock input loading is 1 TTL load.
4. At the end of the conversion, the E.O.C. signal will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. signal is low.
5. Absolute accuracy includes offset, gain, linearity, and all other errors. See Technical Note #3.
6. FSR is full scale range.

TIMING AND CONNECTION

TIMING DIAGRAM



NOTES:

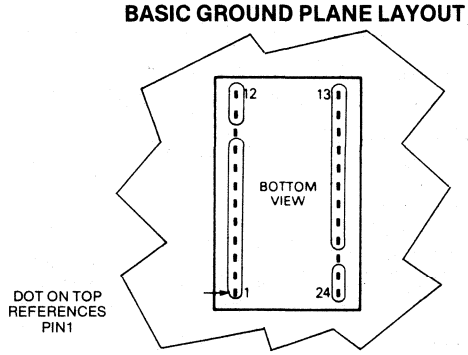
1. The converter is reset by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nsec prior to the clock transition. After the START is again set high, the conversion will begin on the next rising clock edge. The START CONVERT may be set low at any time during a conversion to reset and begin again.
2. At the end of conversion, the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
3. The serial output is non-return to zero.

OUTPUT CODING AND RANGE SELECTION

DIGITAL OUTPUT	ANALOG INPUT — UNIPOLAR RANGES					
	0 TO −5V	0 TO −10V	0 TO −20V	0 TO +5V	0 TO +10V	0 TO +20V
0000 0000	0.000V	0.000V	0.000V	+4.981V	+9.961V	+19.922V
0000 0001	−0.019V	−0.039V	−0.078V	+4.961V	+9.922V	+19.844V
0111 1111	−2.481V	−4.961V	−9.922V	+2.500V	+5.000V	+10.000V
1000 0000	−2.500V	−5.000V	−10.000V	+2.481V	+4.961V	+9.922V
1111 1110	−4.961V	−9.922V	−19.844V	+0.019V	+0.039V	+0.078V
1111 1111	−4.981V	−9.961V	−19.922V	0.000V	0.000V	0.000V

DIGITAL OUTPUT	ANALOG INPUT — BIPOLAR RANGES		
	±2.5V	±5.0V	±10.0V
0000 0000	+2.500V	+5.00V	+10.000V
0000 0001	+2.481V	+4.961V	+9.922V
0111 1111	+0.019V	+0.039V	+0.078V
1000 0000	0.000V	0.000V	0.000V
1111 1110	−2.461V	−4.922V	−9.844V
1111 1111	−2.481V	−4.961V	−9.922V

BASIC GROUND PLANE LAYOUT

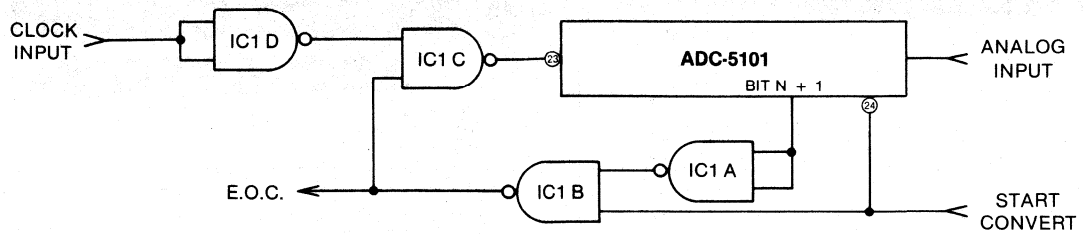


THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

INPUT RANGE SELECTION

INPUT VOLTAGE RANGE	CONNECT ANALOG INPUT TO PIN	CONNECT PIN 8 TO PIN	CONNECT PIN 10 TO PIN
0 to −5V	11	12	7,9
0 to −10V	11	—	7,9
0 to −20V	12	—	7,9
0 to +5V	11	7,9,12	—
0 to +10V	11	7,9	—
0 to +20V	12	7,9	—
±2.5V	11	9,12	7
±5V	11	9	7
±10V	12	9	7

SHORT CYCLE OPERATION



IC1 SN7400N QUAD NAND GATE

When less than 8 bit resolution is required, the ADC-5101 may be operated at higher conversion speeds by truncating the conversion when the desired number of bits have been converted. Connect the converter as shown in the logic diagram. The bit output used to drive gate "A" should be one more than the number of bits to be converted, for example; for 6 bits resolution, connect this gate to the bit 7 output.

MAXIMUM CONVERSION SPEEDS

BITS	CONVERSION SPEED
7	750 nsec
6	650 nsec
5	500 nsec
4	400 nsec

MIL-STD-883B PROCESSING QL PROGRAM

Military and Aerospace programs require high reliability devices subjected to rigorous screening procedures. To meet this need, Datel-Intersil has developed its QL program, a high level of screening, strictly in accordance with MIL-STD-883, method 5008, class B. All devices in this program are hermetically sealed and designated with the suffix "QL". The ADC-5101 is available with 100% screening to Datel-Intersil's QL program. The following chart briefly summarizes the test procedures followed by the QL program in conformance with MIL-STD-883B.

TEST	METHOD	PURPOSE
HIGH TEMPERATURE STORAGE	Method 1008, Test condition C, 24 hrs @ +150°C	Eliminates device failure due to storage at elevated temperatures.
INTERNAL VISUAL (PRECAP)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical or thermal stress.
SEAL, FINE AND GROSS	Method 1014, test condition A (fine), 5×10^{-7} cc/sec., test condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
THERMAL SHOCK[1]	Method 5011, test condition A, 15 cycles @ 0°C to +100°C.	Determines resistance of device to sudden exposure to extreme temperate changes. Removes potential failures due to thermal stress on bonds, etc.
TEMPERATURE CYCLING	Method 1010, test condition C, −65°C to +150°C	
CONSTANT ACCELERATION	Method 2001, test condition A, Y_1 AXIS, 5 Kg.	Eliminates potential failures due to structural or mechanical weaknesses not detected in shock or vibration tests.
BURN-IN TEST	Method 1015, test condition B, 160 hrs @ +125°C.	Stresses device at or above maximum rated operating temperature in order to eliminate infant mortality failures.
FINAL ELECTRICAL TESTS	Performed at +25°C, and at maximum & minimum operating temperatures.	Verifies that device still meets specified data sheet parameters.
EXTERNAL VISUAL	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

1. Per MIL-STD-883B, Thermal shock may be substituted for temperature cycling.

NEW

DATEL

Adjustment-Free 12 Bit A/D Converters ADC-5210 Series

FEATURES

- 13 μsec Max. Conversion Time
- Totally Adjustment Free
- Industry Standard Converter
- MIL-STD-883 Versions Available
- Low Power Consumption

GENERAL DESCRIPTION

Datel-Intersil's ADC-5210 series are high performance, hybrid, 12 bit successive approximation A/D converters. These devices combine high speed with extreme accuracy to provide the best possible performance in systems that require low power consumption, adjustment free operation, and miniature size.

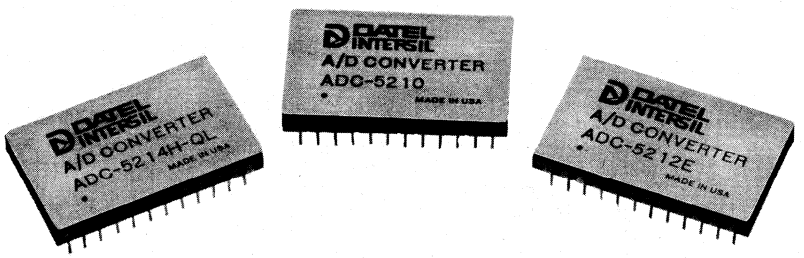
Active laser trimming of highly stable thin-film resistor networks eliminates the need for external adjustment circuits. Full scale absolute accuracy error is ±0.05% FSR maximum at +25°C and only ±0.2% FSR maximum over the full operating temperature range. Zero error is a maximum of only ±0.025% FSR. Conversion Time is 13 μsec maximum, allowing full accuracy with a 1 MHz clock.

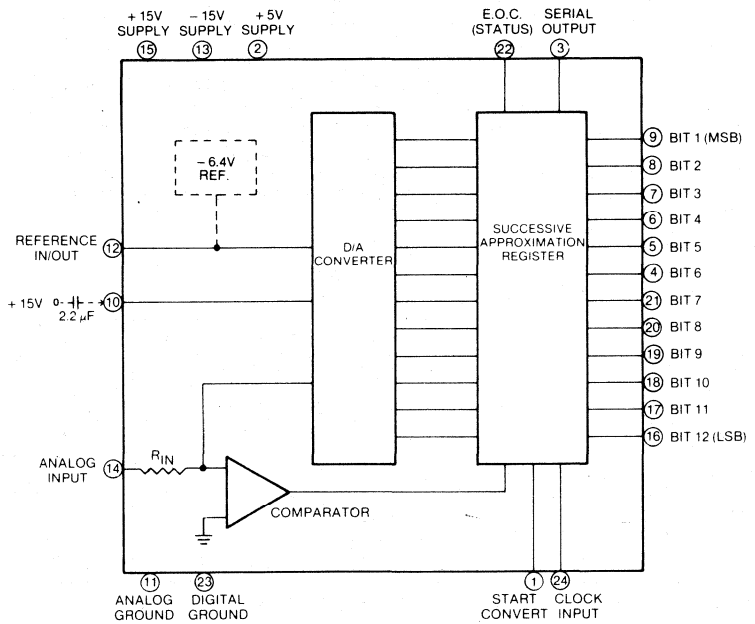
These devices are available in four, factory set, input ranges: 0 to −10V, ±5V, ±10V and 0 to +10V. Models are available with an internal reference, or, for improved overall accuracy, requiring an external reference. For each model, ±½ LSB linearity is guaranteed over the full operating temperature range.

Other significant features include serial or parallel output data, 915 mW maximum power consumption, and a 10 ppm/°C Gain Tempco. Digital outputs are TTL compatible and output coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation.

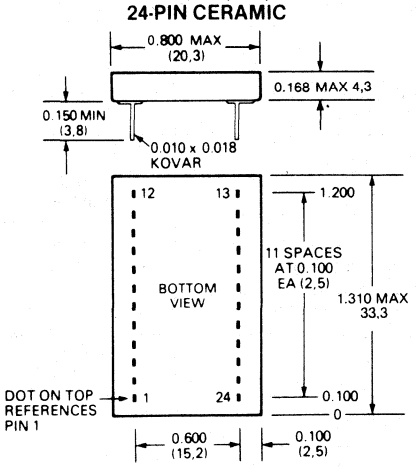
Models are available specified over the full military operating temperature range of −55°C to +125°C, the industrial, −25°C to +85°C, and commercial, 0°C to +70°C, operating temperature ranges. Devices subjected to high reliability processing, screening, and qualification according to Method 5008 of MIL-STD-883 Class B are also available.

All models require ±15 VDC and +5VDC for operation and are packaged in a 24 pin, hermetically sealed, ceramic package.





MECHANICAL DIMENSIONS INCHES (MM) 24-PIN CERAMIC



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	13	−15V SUPPLY
2	+5V SUPPLY	14	ANALOG INPUT
3	SERIAL OUTPUT	15	+15V SUPPLY
4	BIT 6 OUT	16	BIT 12 OUT (LSB)
5	BIT 5 OUT	17	BIT 11 OUT
6	BIT 4 OUT	18	BIT 10 OUT
7	BIT 3 OUT	19	BIT 9 OUT
8	BIT 2 OUT	20	BIT 8 OUT
9	BIT 1 OUT (MSB)	21	BIT 7 OUT
10	2.2 μF to +15V	22	E.O.C. (STATUS)
11	ANALOG GROUND	23	DIGITAL GROUND
12	REF. IN/OUT*	24	CLOCK INPUT

*The ADC-5210, 5211, 5212, and 5216 have an internal reference. The ADC-5213, 5214 and 5215 require an external reference.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-5210 SERIES

Typical at + 25°C, ± 15 VDC and + 5 VDC supplies, V_{REF} = − 10.000V, unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature Range:				
ADC-521X	0°C to +70°C			
ADC-521XE	−25°C to +85°C			
ADC-521XH	−55°C to +125°C			
Storage Temperature Range	−65°C to +150°C			
Positive Supply, Pin 15	+18V			
Negative Supply, Pin 13	−18V			
Logic Supply, Pin 2	−0.5V to +7V			
Analog Input, Pin 14	25V			
Digital Inputs, Pins 1, 24	−0.5V to +5.5V			
Digital Ouputs	Logic Supply			
Reference Input[1]	0 to −15V			
ANALOG INPUTS[2]	**MODEL NUMBER[1]**		**MODEL NUMBER[1]**	
Input Range (Input Impedance)				
0 to −10V (6.7 kΩ)	ADC-5210 ADC-5211 ADC-5212 ADC-5216		ADC-5213 ADC-5214 ADC-5215	
−5V to +5V (6.7 kΩ)				
−10V to +10V (13.4 kΩ)				
0 to +10V (6.7 kΩ)				
TRANSFER CHARACTERISTICS	**TYP.**	**MAX.**	**TYP.**	**MAX.**
Linearity Error: +25°C	± ¼ LSB	± ½ LSB	± ¼ LSB	± ½ LSB
0°C to +70°C	± ¼ LSB	± ½ LSB	± ¼ LSB	± ½ LSB
−55°C to +125°C		± ½ LSB		± ½ LSB
Differential Linearity Error	± ½ LSB		± ½ LSB	
No Missing Codes	Guaranteed over temperature			
Full scale Absolute Accuracy Error[3]				
+25°C	±0.025% FSR	±0.05% FSR	±0.025% FSR	±0.05% FSR
0°C to +70°C	±0.1% FSR	±0.2% FSR	±0.05% FSR	±0.1% FSR
−55°C to +125°C		±0.2% FSR		±0.1% FSR
Zero Error: +25°C	±0.01% FSR	±0.025% FSR	±0.01% FSR	±0.025% FSR
0°C to +70°C	±0.025% FSR	±0.05% FSR	±0.025% FSR	±0.05% FSR
−55°C to +125°C		±0.05% FSR		±0.05% FSR
Gain Error	±0.025%		±0.025%	
Gain Drift	±10 ppm/°C		±3 ppm/°C	
Conversion Time[5]		13 μsec		13 μsec
POWER SUPPLIES				
Power Supply Range: ±15 V supplies		±3%		±3%
+5V supply		±5%		±5%
Power Supply Rejection[6]: +15V supply	±0.005%FSR/%V_S	±0.02%FSR/%V_S	±0.005%FSR/%V_S	±0.02%FSR/V_S
−15V supply	±0.01%FSR/%V_S	±0.05%FSR/%V_S	±0.005%FSR/%V_S	±0.02%FSR/V_S
Current Drain: +15V supply	23 mA	28 mA	23 mA	28 mA
−15V supply	−15 mA	−19 mA	−5 mA	−6.3 mA
+5V supply	25 mA	42 mA	25 mA	42 mA
−10V reference[1]			−1.5 mA	−2 mA
Power Consumption	695 mW	915 mW	567 mW	744 mW

DIGITAL INPUTS (All Models)	**MINIMUM**	**TYPICAL**	**MAXIMUM**
Logic Levels: Logic "1"	2.0V		
Logic "0"			0.7V
Clock Input: Pulse Width High	125 nsec		
Pulse Width Low	175 nsec		
Loading High (V_{IN} = 2.4V)		2 μA	20 μA
Loading Low (V_{IN} = 0.3V)		−0.25 mA	−0.4 mA
Frequency			1 MHz
Start Convert Input:			
Loading High (V_{IN} = 2.4V)		4 μA	40 μA
Loading Low (V_{IN} = 0.3V)		−0.25 mA	−0.4 mA
Set-up Time Start Low to Clock[8]	25 nsec		
DIGITAL OUTPUTS (All Models)			
Logic Coding[9]: Unipolar ranges	Complementary Straight Binary		
Bipolar ranges	Complementary Offset Binary		
Logic Levels: Logic "1"	+2.4V	+3.6V	
Logic "0"		+0.15V	+0.3V
Output Drive Capability, All Outputs[10]:			
Logic "1"	8 TTL Loads		
Logic "0"	2 TTL Loads		
REFERENCE INPUT/OUTPUT[1]			
Internal Reference: Voltage		−6.4V	
Accuracy		±2%	
Tempco of Drift		±5 ppm/°C	
Max. External Current			100 μA
External Reference: Voltage		−10.000V	
Loading			−2 mA

ORDERING INFORMATION

MODEL NUMBER	INPUT VOLT. RANGE	REFERENCE	OPERATING TEMP. RANGE	PRICE (1-24)
ADC-5210	0 to −10V	Internal	0 to +70°C	$
ADC-5210E	0 to −10V	Internal	−25 to +85°C	$
ADC-5210H	0 to −10V	Internal	−55 to +125°C	$
ADC-5211	±5V	Internal	0 to +70°C	$
ADC-5211E	±5V	Internal	−25 to +85°C	$
ADC-5211H	±5V	Internal	−55 to +125°C	$
ADC-5212	±10V	Internal	0 to +70°C	$
ADC-5212E	±10V	Internal	−25 to +85°C	$
ADC-5212H	±10V	Internal	−55 to +125°C	$
ADC-5216	0 to +10V	Internal	0 to +70°C	$
ADC-5216E	0 to +10V	Internal	−25 to +85°C	$
ADC-5216H	0 to +10V	Internal	−55 to +125°C	$
ADC-5213	0 to −10V	External	0 to +70°C	$
ADC-5213E	0 to −10V	External	−25 to +85°C	$
ADC-5213H	0 to −10V	External	−55 to +125°C	$
ADC-5214	±5V	External	0 to +70°C	$
ADC-5214E	±5V	External	−25 to +85°C	$
ADC-5214H	±5V	External	−55 to +125°C	$
ADC-5215	±10V	External	0 to +70°C	$
ADC-5215E	±10V	External	−25 to +85°C	$
ADC-5215H	±10V	External	−55 to +125°C	$

SPECIFICATION NOTES:

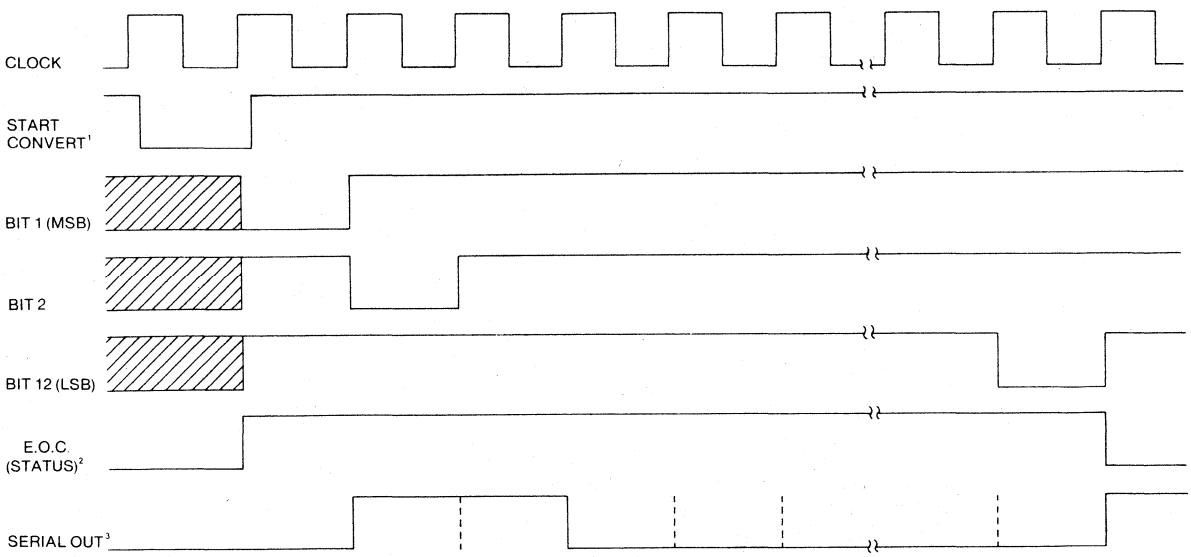
1. The ADC-5210, 5211, 5212, and 5216 include a −6.4V internal reference. The ADC-5213, 5214, and 5215 require an external − 10.000V reference for specified operation.
2. Analog input ranges are internally set at the factory.
3. Absolute Accuracy Error includes offset, gain, linearity and all other errors. See Technical Notes for further information.
4. FSR stands for Full Scale Range and is equal to the peak voltage of the selected analog input range.
5. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. The ADC-5210 Series will meet all specifications with clock frequencies up to 1 MHz. A 1 MHz clock gives a STATUS pulse that is 12 μsec wide, however, unless careful timing precautions are taken, it will usually take 13 μsec to update digital output data.
6. Power Supply rejection is guaranteed over the ±15V ±3% range.
7. The clock may be asymmetrical with minimum positive or negative pulse width.
8. In order to reset the converter, START CONVERT must be brought low at least 25 nsec prior to a high to low clock transition. See Timing Diagram.
9. Serial and Parallel output data have the same coding. Serial data is NRZ successive decision pulses out, MSB first, at the clock frequency. Both serial and parallel output data become valid on the same rising clock edge. Serial data is valid on subsequent falling edges, and these edges can be used to clock serial data into receiving registers.
10. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.

TECHNICAL NOTES

1. The use of proper layout and decoupling techniques are required to obtain rated performance. The ground pins (pins 11 & 23) are not connected internally, and therefore must be connected externally as directed as possible. They should be connected to the system analog ground, preferably through a large ground plane underneath the package. Power supplies should be bypassed to ground at the supply pins with 1 μF electrolytic capacitors in parallel with 0.01 F ceramic capacitors. A 2.2 μF (25V) nonpolarized capacitor must be connected between Pin 10 and +15V.
2. These converters can be made to continuously convert by tying the E.O.C. output (Pin 22) to the start convert input (Pin 1). When connected in this manner, the E.O.C. (START CONVERT) will go low at the end of conversion and the next rising edge of the clock will reset the converter and bring the E.O.C. (START CONVERT) high again. The MSB will be set on the next rising clock edge. The E.O.C. (status) will be low for approximately one clock period following each conversion.
3. The absolute accuracy error of an A/D converter is defined as the difference between the theoretical analog input voltage required to produce a given digital output and the unadjusted analog input voltage actually required to produce that same code. Because this error is measured and specified without adjustment, it includes all factors that may affect the devices accuracy at the point of measurement: offset error, linearity error, gain error, and noise error.
4. Because of propagation delays, the LSB of any given conversion may not be valid until a maximum of 30 nsec after the E.O.C. (status) output has returned low. If the E.O.C. is used to strobe latches holding output data, adequate delays must be provided. Gate delays may be employed or the E.O.C. can be made the input of a D flip flop whose clock input is the same as the converter clock. Connected in this manner, the Q output will change one clock period after the E.O.C. changes. If the converter is connected in the continuous mode, the E.O.C. can be NORed with the converter clock to produce a positive strobe pulse ½ period wide, ½ period after the E.O.C. output has gone low. The rising edge of the pulse can be used to latch data after each conversion.
5. Applications of these converters that require the use of sample-hold may be satisfied by Datel-Intersil's SHM-6, a high speed hybrid unit featuring 1.0 sec acquisition time, 0.01% accuracy, programmable gains from ±1 to ±10 and a ±10V output range.

TIMING & CONNECTION

TIMING DIAGRAM



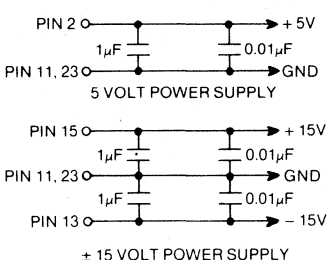
NOTES:

1. The converter is reset by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nsec prior to the clock transition. After the START is again set high, the conversion will begin on the next rising clock edge. The START CONVERT may be set low at any time during a conversion to reset and begin again.
2. At the end of conversion, the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
3. The serial output is non-return to zero.

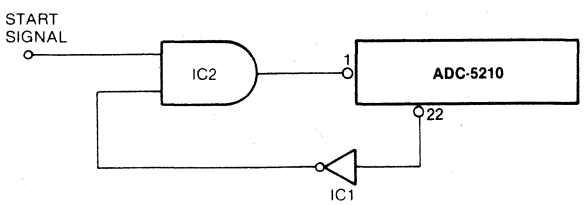
DIGITAL OUTPUT CODING

DIGITAL OUTPUT	ANALOG INPUT VOLTAGE			
	0 TO +10V ADC-5216	0 TO −10V ADC-5210, 5213	±5V ADC-5211, 5214	±10V ADC-5212, 5215
0000 0000 0000	+10.0000V	0.0000V	+5.0000V	+10.0000V
0000 0000 0001	+ 9.9976V	− 0.0024V	+4.9976V	+ 9.9951V
0111 1111 1111	+ 5.0024V	− 4.9976V	+0.0024V	+ 0.0049V
1000 0000 0000	+ 5.0000V	− 5.0000V	0.0000V	0.0000V
1111 1111 1110	+ 0.0024V	− 9.9976V	−4.9976V	− 9.9951V
1111 1111 1111	0.0000V	−10.0000V	−5.0000V	−10.0000V

POWER SUPPLY DECOUPLING



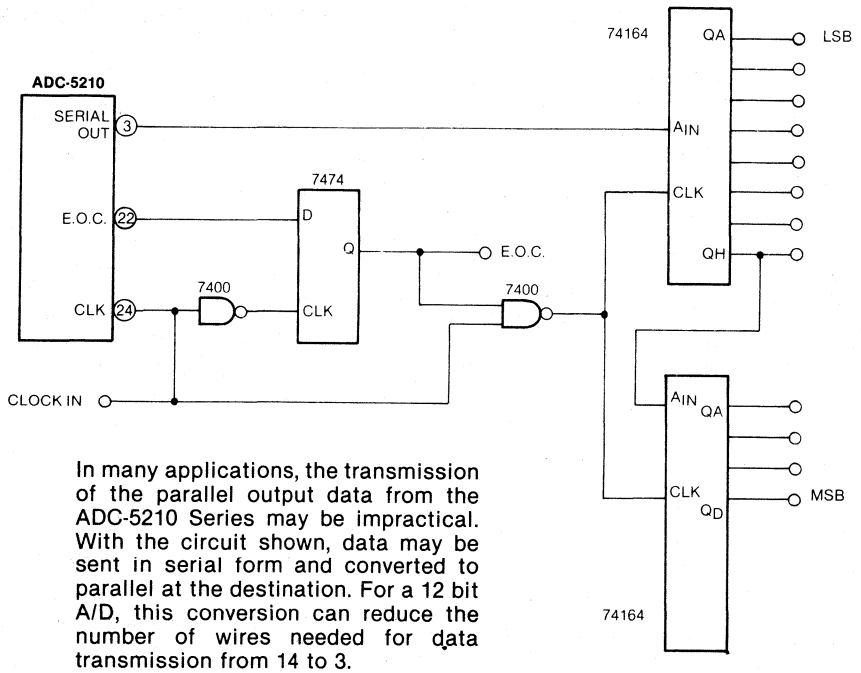
TRIGGERING WITH A POSITIVE EDGE



The ADC-5210 Series A/D's may be made to start converting on a positive going edge by employing the circuit shown. The rising edge of the start signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. When the converter resets, the status output (pin 22) goes high, the output of IC1 goes low; and since the start signal is still high, the output of IC2 goes high allowing the conversion to continue immediately. The start signal should be brought low before the conversion is complete.

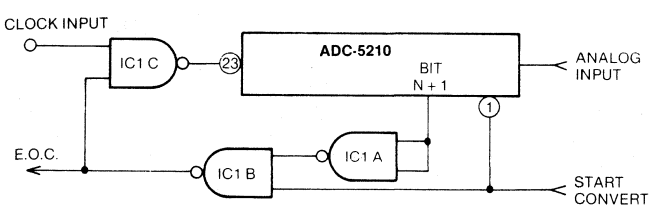
APPLICATIONS

SERIAL TO PARALLEL CONVERSION



In many applications, the transmission of the parallel output data from the ADC-5210 Series may be impractical. With the circuit shown, data may be sent in serial form and converted to parallel at the destination. For a 12 bit A/D, this conversion can reduce the number of wires needed for data transmission from 14 to 3.

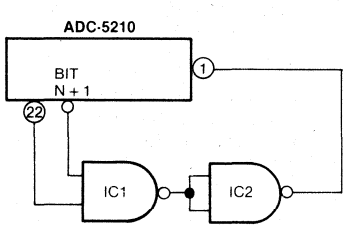
SHORT CYCLE OPERATION



IC1 SN7400N QUAD NAND GATE

If an application requires less than 12 bits resolution, the ADC-5210 series may be truncated to the desired number of bits, with a proportionate decrease in conversion time, by using the circuit shown. With this circuit the start convert and E.O.C. signals function normally.

SHORT CYCLE — CONTINUOUS CONVERTING

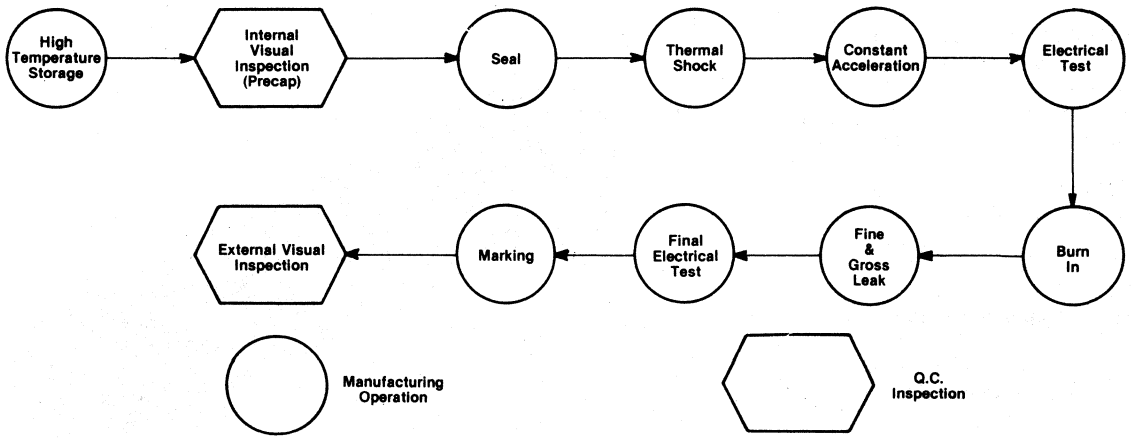


IC = 7400

To continuously convert at N bits, the the circuit shown may be used. The output of bit (N + 1) acts like a status when one converts at N bits. The START CONVERT input is made the AND function of bit (N + 1) and the STATUS output to prevent the possibility of a lock up condition at power-on.

MIL-STD-883B PROCESSING QL PROGRAM

Military and Aerospace programs require high reliability devices subjected to rigorous screening procedures. To meet this need Datel-Intersil has developed its QL program, a high level of screening, strictly in accordance with MIL-STD-883, method 5008, Class B. All devices in this program are hermetically sealed and designated with the suffix "QL". All models in the ADC-5210 series are available with 100% screening to Datel-Intersil's QL program. The following flow diagram and chart briefly summarize the test procedures followed by the QL program in conformance with MIL-STD-883B. For more complete information, contact your nearest sales office for Datel-Intersil's brochure "HIGH RELIABILITY HYBRID MICROCIRCUITS FOR DATA ACQUISITION".



TEST	METHOD	PURPOSE
HIGH TEMPERATURE STORAGE	Method 1008, Test condition C, 24 hrs @ +150°C	Eliminates device failure due to storage at elevated temperatures.
INTERNAL VISUAL (PRECAP)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical or thermal stress.
SEAL, FINE AND GROSS	Method 1014, test condition A (fine), 5×10^{-7} cc/sec., test condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
THERMAL SHOCK[1]	Method 5011, test condition A, 15 cycles @ 0°C to +100°C.	Determines resistance of device to sudden exposure to extreme temperate changes. Removes potential failures due to thermal stress on bonds, etc.
TEMPERATURE CYCLING	Method 1010, test condition C, −65°C to +150°C	
CONSTANT ACCELERATION	Method 2001, test condition A, Y_1 AXIS, 5 Kg.	Eliminates potential failures due to structural or mechanical weaknesses not detected in shock or vibration tests.
BURN-IN TEST	Method 1015, test condition B, 160 hrs @ +125°C.	Stresses device at or above maximum rated operating temperature in order to eliminate infant mortality failures.
FINAL ELECTRICAL TESTS	Performed at +25°C, and at maximum & minimum operating temperatures.	Verifies that device still meets specified data sheet parameters.
EXTERNAL VISUAL	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

1. Per MIL-STD-883B, Thermal shock may be substituted for temperature cycling.

NEW

DATEL

12 Bit Binary A/D Converter for Microprocessor Interfaces
ADC-7109

FEATURES

- 12 bits with Plus Sign and overrange indication
- Sign Magnitude Coding Format
- True Differential Signal and Reference Inputs
- Single or Two Byte μP Bus Interface
- TTL Compatible Byte organized three-state outputs
- UART Control Signals
- Direct bus connection for 8 or 16-bit bus
- Internal Oscillator
- Auto Zero
- Differential Analog Input and Reference
- Low Noise — typically 15 μV P-P
- 1 pA Typical Input Current
- Low Power — 20 mW

GENERAL DESCRIPTION

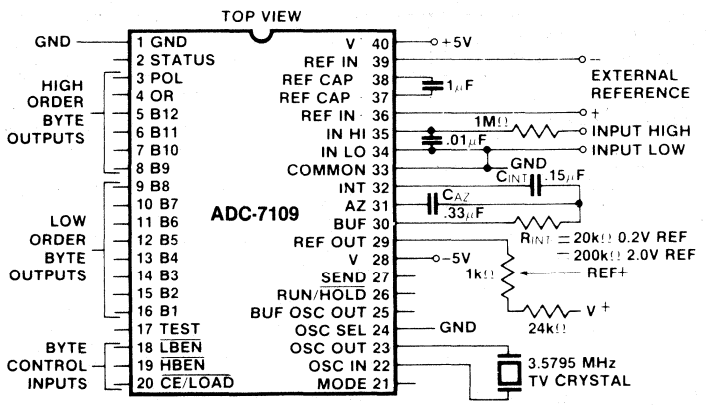
DATEL-INTERSIL's ADC-7109 is a 12 bit, high performance, low power, integrating A/D converter. All the active circuitry required for μP interface is included within the device.

The output data may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. In the handshake mode, the ADC-7109 will operate with industry standard UARTs in controlling serial data transmission. The RUN/$\overline{\text{HOLD}}$ input and STATUS output allow monitoring and control of conversion timing.

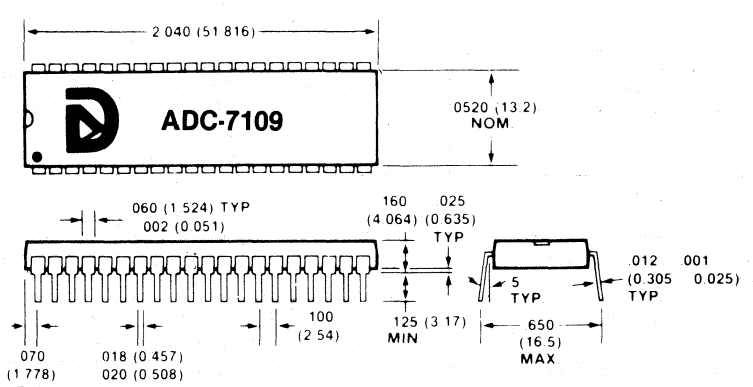
Other features of the ADC-7109 include typical input bias current of 1 pA, zero drift of less than 1 μV/°C, input noise typically 15 μV P-P and auto-zero. True differential input and reference allow the measurement of bridge-type transducers such as, strain gauges and temperature transducers. These features, in combination with high accuracy, low noise, low drift, versatility and low cost, make the ADC-7109 an ideal per-channel alternative to analog multiplexing for many data acquisition applications.

The ADC-7109 is available for operation over the commercial, 0°C to +70°C temperature range and is packaged in a 40 pin plastic DIP.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.



MECHANICAL DIMENSIONS
INCHES (mm)



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+)	+6.2V
Negative Supply Voltage (GND to V^-)	−9V
Analog Input Voltage (Lo or Hi) (Note 1)	V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1)	V^+ to V^-
Digital Input Voltage (Pins 2-27) (Note 2)	$V^+ + 0.3V$ GND −0.3V
Power Dissipation (Note 3)	500mW @ 70°C
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Lead Temperature (soldering, 60 sec)	300°C

Absolute maximum ratings define stress limitations which if exceeded may permanently damage the device. These ratings are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE I OPERATING CHARACTERISTICS

All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.
Test circuit as shown on page 1.

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} 0.0V Full scale = 409.6mV	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		V_{IN} V_{REF} V_{REF} 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full scale 409.6mV or 4.096V	1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale.			1	±.2	+1	Counts
Common Mode Rejection Ratio		V_{CM} ± 1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Common Mode Rejection Ratio	CMRR	V_{CM} ± 1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Lo, Common	V− +1.5		V+ −1.0	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Noise (p-p value not exceeded 95% of time)		V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage Current at Input		V_{IN} = 0V		1	10	pA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV => 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I_{DL}	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{DA}			700	1500	μA
Ref Out Voltage		Referred to V^+, 25kΩ between V^+ and REF OUT	−2.4	−2.8	−3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	V^- +1.5	V+ −0.5 to V^- +1.0	V^+ −1.0	V

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage		V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current			Pins 18, 19, 20 V_{OUT} = V^+ −3V MODE input at GND		5		μA
Control I/O Loading			$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
Input High Voltage		V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			Pins 26, 27 V_{OUT} = V^+ −3V		5		μA
Input Pull-up Current			Pins 17, 24 V_{OUT} = V^+ −3V		25		μA
Input Pull-down Current			Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High	O_{OH}	V_{OUT} = 2.5V		1		mA
	Low	O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High	BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low	BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width		t_W		50			ns

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ADC-7109 before its power supply is established, and that in multiple supply systems the supply to the ADC-7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

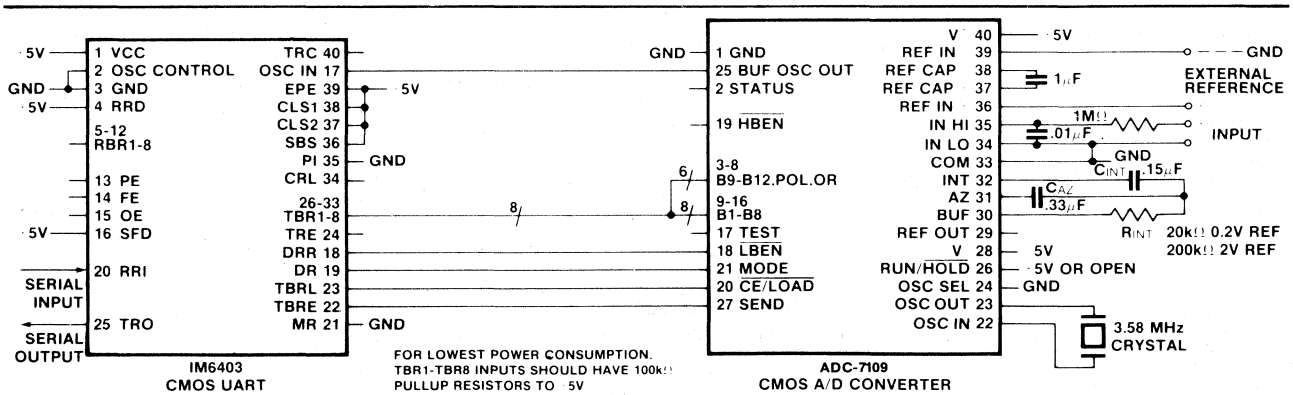


Figure 1A. To transmit latest result, send any word to UART.

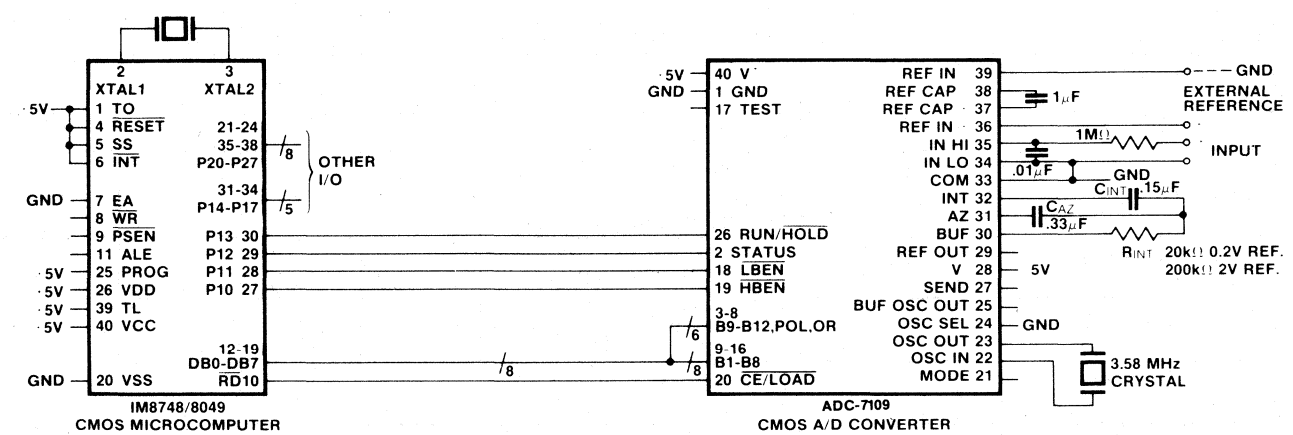


Figure 1B. Typical Connection Diagram Parallel Interface With 8748/8048 Microcomputer

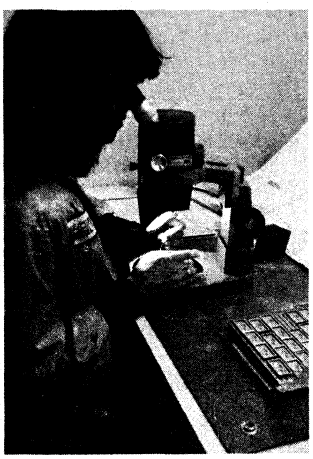
TABLE 2 - Pin Assignment and Function Description

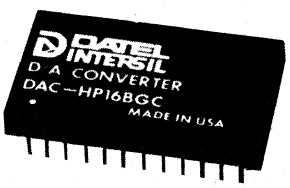
PIN	SYMBOL	DESCRIPTION
1	GND	Digital Ground. 0V. Ground return for all digital logic
2	STATUS	Output - High during integrate and deintegrate until data is latched. - Low when analog section is in Auto-Zero configuration.
3	POL	Polarity. Three-State Output
4	OR	Over-range. Three-State Output
5	B12	Bit 12 (Most Significant Bit)
6	B11	Bit 11
7	B10	Bit 10
8	B9	Bit 9
9	B8	Bit 8
10	B7	Bit 7
11	B6	Bit 6 — Data Bits. Three-State Output
12	B5	Bit 5
13	B4	Bit 4
14	B3	Bit 3
15	B2	Bit 2
16	B1	Bit 1 (Least Significant Bit)
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only.
18	$\overline{\text{LBEN}}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. - With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	$\overline{\text{HBEN}}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. - With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.
20	$\overline{\text{CE LOAD}}$	Chip Enable Load - With Mode (Pin 21) low, $\overline{\text{CE LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. - With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.

PIN	SYMBOL	DESCRIPTION
21	MODE	Input Low - Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. - Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1.58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN $\overline{\text{HOLD}}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data.
28	V⁻	Analog Negative Supply - Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V⁺ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN	Differential Reference Input Positive
37	REF CAP	Reference Capacitor Positive
38	REF CAP	Reference Capacitor Negative
39	REF IN	Differential Reference Input Negative
40	V⁺	Positive Supply Voltage - Nominally +5V with respect to GND Pin 1

ORDERING INFORMATION

MODEL ADC-7109
OPERATING TEMP. RANGE ..... 0°C to +70°C
PRICE (1-24) ..... $
TRIMMING POTENTIOMETER TP1K ..... $

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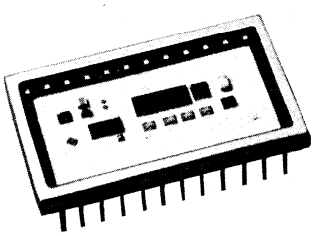
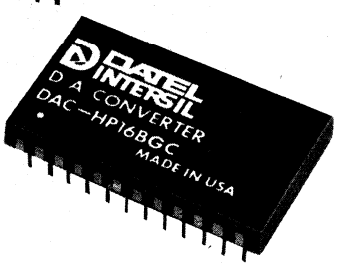
INTERSIL
D A CONVERTER
DAC—HP16BGC
MADE IN USA

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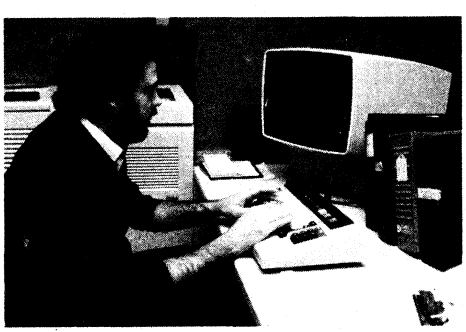
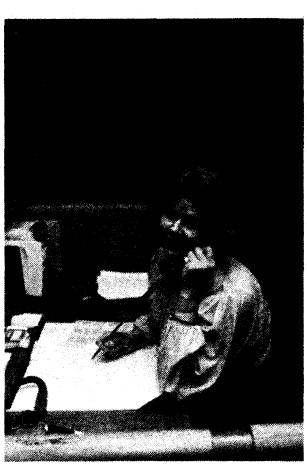
DAC—HP16BGC
MADE IN USA





DIGITAL TO ANALOG CONVERTERS

Digital-To-Analog Converters

Introduction

Digital-to-analog converters are the devices by which computers communicate with the outside world. They are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digitally controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters. D/A converters are also referred to as DAC's and are termed *decoders* by communications engineers.

The transfer function of an ideal 3-bit D/A converter is shown in Figure 1. Each input code word produces a single, discrete analog output value, generally a voltage. Over the output range of the converter 2^n different values are produced including zero; and the output has a one-to-one correspondence with input, which is not true for A/D converters.

There are many different circuit techniques used to implement D/A converters, but a few popular ones are widely used today. Virtually

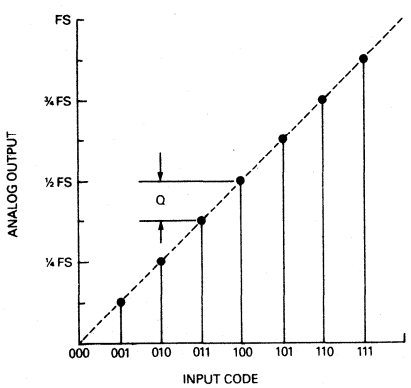


Figure 1. Transfer Function of Ideal 3-Bit D/A Converter

all D/A converters in use are of the *parallel type* where all bits change simultaneously upon application of an input code word; *serial type* D/A converters, on the other hand, produce an analog output only after receiving all digital input data in sequential form.

Weighted Current Source D/A Converter

The most popular D/A converter design in use today is the weighted current source circuit illustrated in Figure 2. An array of switched transistor current sources is used with binary weighted currents. The binary weighting is achieved by using emitter resistors with binary related values of R, 2R, 4R, 8R,.....2^nR. The resulting collector currents are then added together at the current summing line.

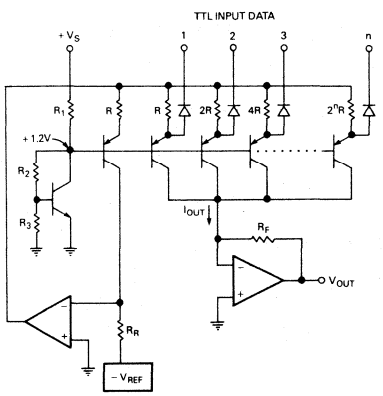


Figure 2. Weighted Current Source D/A Converter

The current sources are switched on or off from standard TTL inputs by means of the control diodes connected to each emitter. When the TTL input is high the current source is on; when the input is low it is off, with the current flowing through the control diode. Fast switching speed is achieved because there is direct control of the transistor current, and the current sources never go into saturation.

To interface with standard TTL levels, the current sources are biased to a base voltage of +1.2V. The emitter currents are regulated to constant values by means of the control amplifier and a precision voltage reference circuit together with a bipolar transistor.

The summed output currents from all current sources that are on go to an operational amplifier summing junction; the amplifier converts this output current into an output voltage. In some D/A converters the output current is used to directly drive a resistor load for maximum speed, but the positive output voltage in this case is limited to about +1 volt.

The weighted current source design has the advantages of simplicity and high speed. Both PNP and NPN transistor current sources can be used with this technique although the TTL interfacing is more difficult with NPN sources. This technique is used in most monolithic, hybrid, and modular D/A converters in use today.

A difficulty in implementing higher resolution D/A converter designs is that a wide range of emitter resistors is required, and very high value resistors cause problems with both temperature stability and switching speed. To overcome these problems, weighted current sources are used in identical groups, with the output of each group divided down by a resistor divider as shown in Figure 3.

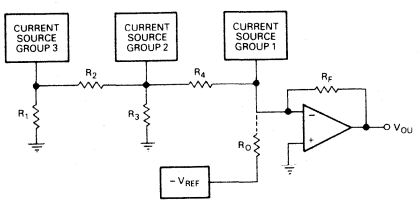


Figure 3. Current Dividing the Outputs of Weighted Current Source Groups

The resistor network R_1 through R_4, divides the output of Group 3 down by a factor of 256 and the output of Group 2 down by a factor of 16 with respect to the output of Group 1. Each group is identical, with four current sources of the type shown in Figure 2, having binary current weights of 1, 2, 4, 8. Figure 3 also illustrates the method of achieving a bipolar output by deriving an offset current from the reference circuit which is then subtracted from the output current line through resistor R_0. This current is set to exactly one half the full scale output current.

R-2R D/A Converter

A second popular technique for D/A conversion is the R-2R ladder method. As shown in Figure 4, the network consists of series resistors of value R and shunt resistors of value 2R. The bottom of each shunt resistor has a single-pole double-throw electronic switch which connects the resistor to either ground or the output current summing line.

The operation of the R-2R ladder network is based on the binary division of current as it flows down the ladder. Examination of the ladder configuration reveals that at point A looking to the right, one measures a resistance of 2R; therefore the reference input to the ladder has a resistance of R. At the reference input the current splits into two equal parts since it sees equal resistances in either direction. Likewise, the current flowing down the ladder to the right continues to divide into two equal parts at each resistor junction.

The result is binary weighted currents flowing down each shunt resistor in the ladder. The digitally controlled switches direct the currents to either the summing line or ground. Assuming all bits are on as shown in the diagram, the output current is

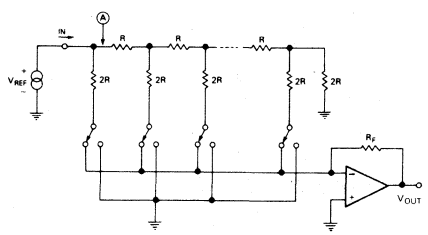


Figure 4. R-2R Ladder D/A converter

$$I_{OUT} = \frac{V_{REF}}{R}\left[\tfrac{1}{2}+\tfrac{1}{4}+\tfrac{1}{8}+.....+\frac{1}{2^n}\right]$$

which is a binary series. The sum of all currents is then

$$I_{OUT} = \frac{V_{REF}}{R}\left(1-2^{-n}\right)$$

where the 2^{-n} term physically represents the portion of the input current flowing through the 2R terminating resistor to ground at the far right.

As in the previous circuit, the output current summing line goes to an operational amplifier which converts current to voltage.

The advantage of the R-2R ladder technique is that only two values of resistors are required, with the resultant ease of matching or trimming and excellent temperature tracking. In addition, for high speed applications relatively low resistor values can be used. Excellent results can be obtained for high resolution D/A convertes by using laser-trimmed thin film resistor networks.

Multiplying and Deglitched D/A Converters

The R-2R ladder method is specifically used for *multiplying type* D/A converters. With these converters, the reference voltage can be varied over the full range of $\pm V_{max}$ with the output the product of the reference voltage and the digit input word. Multiplication can be performed in 1, 2, or 4 algebraic quadrants.

If the reference voltage is unipolar, the circuit is a one-quadrant multiplying DAC; if it is bipolar, the circuit is a two-quadrant multiplying DAC. For four-quadrant operation the two current summing lines shown in Figure 4 must be subtracted from each other by operational amplifiers.

In multiplying D/A converters, the electronic switches are usually implemented with CMOS devices. Multiplying DAC's are commonly used in automatic gain controls, CRT character generation, complex function generators, digital attenuators, and divider circuits. Figure 5 shows two 14-bit multiplying CMOS D/A converters.

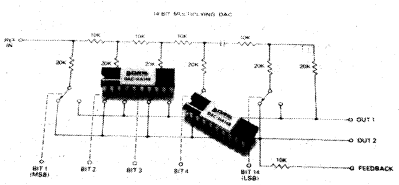


Figure 5. CMOS 14-Bit Multiplying D/A Converters

Another important D/A converter design takes advantage of the best features of both the weighted current source technique and the R-2R ladder technique. This circuit, shown in Figure 6, uses equal value switched current sources to drive the junctions of the R-2R ladder network. The advantage of the equal value current sources is obvious since all emitter resistors are identical and switching speeds are also identical. This technique is used in many ultra-high speed D/A converters.

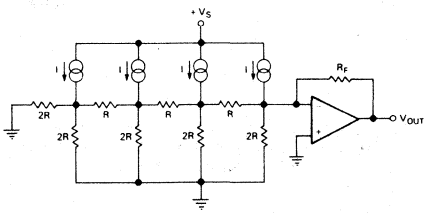


Figure 6. D/A Converter Employing R-2R Ladder with Equal Value Switched Current Sources

One other specialized type D/A converter used primarily in CRT display systems is the *deglitched* D/A converter. All D/A converters produce output spikes, or *glitches*, which are most serious at the major output transitions of ¼ FS, ½ FS, and ¾ FS as illustrated in Figure 7(a).

Glitches are caused by small time differences between some current sources turning off and others turning on. Take, for example, the major code transition at half scale from 0111....1111 to 1000....0000. Here the MSB current source turns on while all other current sources turn off. The small difference in switching times results in a narrow half scale glitch. Such a glitch produces distorted characters on CRT displays.

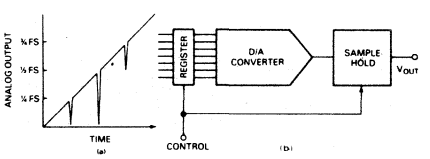


Figure 7. Output Glitches (a) and Deglitched D/A Converter (b)

Glitches can be virtually eliminated by the circuit shown in Figure 7(b). The digital input to a D/A converter is controlled by an input register while the converter output goes to a specially designed sample-hold circuit. When the digital input is updated by the register, the sample-hold is switched into the hold mode. After the D/A has changed to its new output value and all glitches have settled out, the sample-hold is then switched back into the tracking mode. When this happens, the output changes smoothly from its previous value to the new value with no glitches present.

Glossary of Digital To Analog Terms

ABSOLUTE ACCURACY: The worst-case input to output error of a data converter referred to the NBS standard volt.

ACCURACY: The conformance of a measured value with its true value; the maximum error of a device such as a data converter from the true value. See *relative accuracy* and *absolute accuracy.*

BCD: See *Binary Coded Decimal.*

BINARY CODE: See *Natural Binary Code.*

BINARY CODED DECIMAL (BCD): A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

BIPOLAR MODE: For a data converter, when the analog signal range includes both positive and negative values.

BIPOLAR OFFSET: The analog displacement of one half of full scale in a data converter operated in the bipolar mode. The offset is generally derived from the converter reference circuit.

COMPANDING CONVERTER: An A/D or D/A converter which employs a logarithmic transfer function to expand or compress the analog signal range. These converters have large effective dynamic ranges and are commonly used in digitized voice communication systems.

COMPLEMENTARY BINARY CODE: A binary code which is the logical complement of straight binary. All 1's become 0's and vice versa.

CONVERSION RATE: The number of repetitive A/D or D/A conversions per second for a full scale change to specified resolution and linearity.

DAC: Abbreviation for digital-to-analog converter. See *D/A Converter.*

D/A CONVERTER: Digital-to-analog converter. A circuit which converts a digital code word into an output analog (continuous) voltage or current.

DATA CONVERTER: An A/D or D/A Converter.

DATA DISTRIBUTION SYSTEM: A system which uses D/A converters and other circuits to convert the digital outputs of a computer into analog form for control of a process or system.

DECODER: A communications term for D/A converter.

DEGLITCHED DAC: A D/A converter which incorporates a deglitching circuit to virtually eliminate output spikes (or glitches). These DAC's are commonly used in CRT display systems.

DEGLITCHER: A special sample-hold circuit used to eliminate the output spikes (or glitches) from a D/A converter.

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of $FSR/2^n$.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

DYNAMIC ACCURACY: The total error of a data converter or conversion system when operated at its maximum specified conversion rate or throughput rate.

DYNAMIC RANGE: The ratio of full scale range (FSR) of a data converter to the smallest difference it can resolve. In terms of converte resolution:

$$\text{Dynamic Range (DR)} = 2^n$$

It is generally expressed in dB:

$$DR = 20 \log_{10} 2^n = 6.02n$$

where n is the resolution in bits.

FSR: Full Scale Range.

FULL SCALE RANGE (FSR): the difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

LEAST SIGNIFICANT BIT (LSB): The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution:

$$\text{LSB Size} = \frac{FSR}{2^n}$$

where FSR is full scale range and n is the resolution in bits.

LINEARITY ERROR: See *Integral Linearity Error* and *Differential Linearity Error.*

LONG TERM STABILITY: The variation in data converter accuracy due to time change alone. It is commonly specified in percent per 1000 hours or per year.

LSB: Least Significant Bit.

LSB SIZE: See *Quantum.*

MAJOR CARRY: See *Major Transition.*

MAJOR TRANSITION: In a data converter, the change from a code of 1000... 000 to 0111...1111 or vice-versa. This transition is the most difficult one to make from a linearity standpoint since the MSB weight must ideally be precisely one LSB larger than the sum of all other bit weights.

MONOTONICITY: For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. *Non-monotonicity* may occur if the converter differential linearity error exceeds ±1 LSB.

MOST SIGNIFICANT BIT (MSB): The left-most bit in a data converter code. It has the largest weight, equal to one half of full scale range.

MSB: Most Significant Bit.

MULTIPLYING D/A CONVERTER: A type of digital-to-analog converter in which the reference voltage can be varied over a wide range to produce an analog output which is the product of the input code and input reference voltage. Multiplication can be accomplished in one, two, or four algebraic quadrants.

NATURAL BINARY CODE: A positive weighted code in which a number is represented by

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \ldots + a_n 2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n}$$

and N has a fractional value between zero and one.

NONMONOTONIC: A D/A converter transfer characteristic in which the output does not continuously increase with increasing input. At one or more points there may be a dip in the output function.

OFFSET BINARY CODE: Natural binary code in which the code word 0000....0000 is displaced by one-half analog full scale. The code represents analog values between −FS and +FS (full scale). The code word 1000....0000 then corresponds to analog zero.

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

OFFSET ERROR: The error at analog zero for a data converter operating in the bipolar mode.

ONE'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all one's.

PARALLEL TYPE D/A CONVERTER: The most commonly used type of D/A converter in which upon application of an input code, all bits change simultaneously to produce a new output.

POWER SUPPLY SENSITIVITY: The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

PRECISION: The degree of repeatability, or reproducibility of a series of successive measurements. Precision is affected by the noise, hysteresis, time, and temperature stability of a data converter or other device.

QUAD CURRENT SWITCH: A group of four current sources weighted 8-4-2-1 which are switched on and off by TTL inputs. They are used to implement A/D and D/A converter designs up to 16 bits resolution by using multiple quads with current dividers between each quad.

QUANTUM: The analog difference between two adjacent codes for an A/D or D/A converter. Also called *LSB size*.

R-2R LADDER NETWORK: An array of matched resistors with series values of R and shunt values of 2R in a standard ladder circuit configuration.

RELATIVE ACCURACY: The worst case input to output error of a data converter, as a percent of full scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

REFERENCE CIRCUIT: A circuit which produces a stable output voltage over time and temperature for use in A/D and D/A converters. The circuit generally uses an operational amplifier with a precision Zener or bandgap type reference element.

RESOLUTION: The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

SCALE FACTOR ERROR: See *Gain Error.*

SERIAL TYPE D/A CONVERTER: A type of digital-to-analog converter in which the digital input data is received in sequential form before an analog output is produced.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and D/A converters.

SIGN-MAGNITUDE BCD: A binary coded decimal code in which a sign bit is added to distinguish positive from negative in bipolar operation.

SIGN-MAGNITUDE BINARY CODE: The natural binary code to which a sign bit is added to distinguish positive from negative in bipolar operation.

SPAN: For an A/D or D/A converter, the full scale range or difference between maximum and minimum analog values.

STATIC ACCURACY: The total error of a data converter or conversion system under DC input conditions.

STRAIGHT BINARY CODE: See *Natural Binary Code.*

TEMPERATURE COEFFICIENT: The change in analog magnitude with temperature, expressed in ppm/°C.

TRANSFER FUNCTION: The input to output characteristic of a device such as a data converter expressed either mathematically or graphically.

TWO'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all zero's plus a carry.

UNIPOLAR MODE: In a data converter, when the analog range includes values of one polarity only.

WEIGHTED CURRENT SOURCE D/A CONVERTER: A digital-to-analog converter design based on a series of binary weighted transistor current sources which can be turned on or off by digital inputs.

ZERO DRIFT: The change with temperature of analog zero for a data converter operating in the unipolar mode. It is generally expressed in μV/°C.

ZERO ERROR: The error at analog zero for a data converter operating in the unipolar mode.

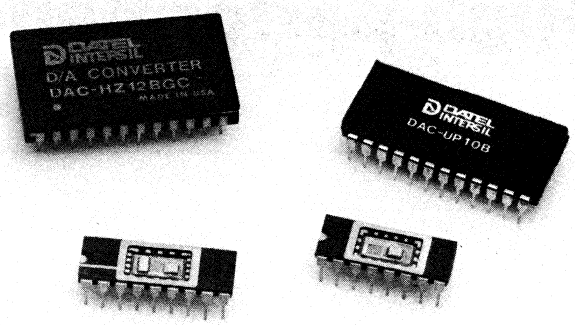
Quick selection: General-purpose D/A converters

	MODEL	DESCRIPTION	RESOLUTION	SETTLING TIME, MAX	LINEARITY ERROR, MAX	OUTPUT	OUTPUT RANGES
	DAC-08BC	Fast 8-bit Monolithic	8 Bits	150 ns	± ½ LSB	Current	0 to −2 mA
	DAC-08BM						
NEW	DAC-562C	Low-cost, 12-bit Monolithic	12 Bits	400 ns	± ½ LSB	Current	0 to −2 mA
NEW	DAC-562M				± ¼ LSB		± 1 mA
	DAC-HA10BC	Precision, CMOS, 4 Quadrant Multiplying D/A Converters	10 Bits	1.3 μs	± ½ LSB	Current	$\pm \bar{V}_{REF}/R_{IN}$
	DAC-HA10BR						
	DAC-HA10BM						
	DAC-HA12BC		12 Bits	5.0 μs	± ½ LSB	Current	$\pm V_{REF}/R_{IN}$
	DAC-HA12BR						
	DAC-HA12BM						
	DAC-HA12DC		3 Digits	5.0 μs	± ½ LSB	Current	$\pm V_{REF}/R_{IN}$
	DAC-HA12DR						
	DAC-HA12DM						
	DAC-HZ12BGC	Low-cost Complete 12-bit D/A	12 Bits	3 μs	± ½ LSB	Voltage	0 to +5V 0 to +10V ±2.5V, ±5V ±10V
	DAC-HZ12BMC						
	DAC-HZ12BMR						
	DAC-HZ12BMM						
	DAC-HZ12DGC		3 Digits		± ¼ LSB		0 to +2.5V 0 to +5V 0 to +10V
	DAC-HZ12DMC						
	DAC-HZ12DMR						
	DAC-HZ12DMM						
	DAC-IC8BC	Low-cost 8-bit D/A	8 Bits	300 ns	± ½ LSB	Current	0 to −2 mA
	DAC-IC8BM						
	DAC-IC10BC	Low-cost Fast 10-bit D/A	10 Bits	250 ns	± 1 LSB	Current	0 to −4 mA
	DAC-IC10B				± ½ LSB		
	DAC-IC10BM						
	DAC-UP8BC	8 Bits with Input Register	8 Bits	2 μs	± ½ LSB	Voltage	0 to +10V ±5V
	DAC-UP8BM						
NEW	DAC-UP10BC	Input Register	10 Bits	5 μs	± 1 LSB	Voltage	0 to +10V, ±5V
NEW	DAC-608C	8, 10, 12-Bit μP Compatible Multiplying D/A's	8 Bits	1 μsec	± ½ LSB	Current	$\left(\frac{Vref}{15k\Omega}\right)\left(\frac{D}{256}\right)$
NEW	DAC-610C		10 Bits	500 nsec			$\left(\frac{Vref}{15k\Omega}\right)\left(\frac{D}{1024}\right)$
NEW	DAC-612R		12 Bits	1 μsec			$\left(\frac{Vref}{15k\Omega}\right)\left(\frac{D}{4096}\right)$

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

DATEL-INTERSIL manufactures a complete line of moderate performance, general purpose digital to analog converters. Devices offered range from a full line of four-quadrant, multiplying D/As to a low cost 12-bit monolithic D/A.

A new addition to this line is the DAC-UP10B, a monolithic 10-bit D/A with input registers. The input registers are controlled by two enable lines to ease data bus interfacing.



INPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
Binary	10 ppm/°C	16-pin DIP	Monolithic	0 to +70	166
				−55 to +125	
Binary	10 ppm/°C	24-pin DIP	Monolithic	0 to +70	184
				−55 to +125	
Binary	20 ppm/°C	16-pin DIP	Hybrid	0 to +70	136
				−25 to +85	
				−55 to +125	
Binary	5 ppm/°C	18-pin DIP	Hybrid	0 to +70	
				−25 to +85	
				−55 to +125	
BCD	5 ppm/°C	18-pin DIP	Hybrid	0 to +70	154
				−25 to +85	
				−55 to +125	
C Binary	20 ppm/°C	24-pin DIP	Hybrid	0 to +70	
				−25 to +85	
				−55 to +125	
C BCD				0 to +70	
				−25 to +85	
				−55 to +125	
Binary	20 ppm/°C	16-pin DIP	Monolithic	0 to +70	158
				−55 to +125	
Binary	20 ppm/°C	16-pin DIP	Monolithic	0 to +70	162
				−55 to +125	
Binary	20 ppm/°C	22-pin DIP	Monolithic	0 to +70	170
				−55 to +125	
Binary	20 ppm/°C	24-pin DIP	Monolithic	0 to +70	174
Binary	6 ppm/°C	20 Pin DIP	Monolithic	0 to +70	188
	10 ppm/°C	20 Pin DIP		0 to +70	
	6 ppm/°C	24 Pin DIP		−25 to +85	

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Quick selection: High-performance D/A converters

MODEL	DESCRIPTION	RESOLUTION	SETTLING TIME, MAX	LINEARITY ERROR, MAX	OUTPUT
DAC-85C-CBI-I	Industry Standard Military and Industrial 12-bit Converters Input logic current only 10 μA	12 Bits	300 ns	± ½ LSB	Current
DAC-85C-CBI-V			3 μs		Voltage
DAC-85-CBI-I			300 ns		Current
DAC-85-CBI-V			3 μs		Voltage
DAC-87-CBI-I			300 ns		Current
DAC-87-CBI-V			3 μs		Voltage
DAC-85C-CCD-I		3 Digits	300 ns	± ¼ LSB	Current
DAC-85C-CCD-V			3 μs		Voltage
DAC-85-CCD-I			300 ns		Current
DAC-85-CCD-V			3 μs		Voltage
DAC-87-CCD-I			300 ns		Current
DAC-87-CCD-V			3 μs		Voltage
DAC-7523	Low cost, high performance 8, 10 and 12 bit multiplying DAC's	8 Bit	200 nsec	± .1%	Voltage
DAC-7533		10 Bit	800 nsec	± .0.1%	
DAC-7541		12 Bit	1 μsec	± .012%	
DAC-HK12BGC	Fast Settling Voltage Output with Input Registers	12 Bits	3 μs	± ½ LSB	Voltage
DAC-HK12BMC					
DAC-HK12BMR					
DAC-HK12BMM					
DAC-HK12DGC		3 Digits	3 μs	± ½ LSB	Voltage
DAC-HK12DMC					
DAC-HK12DMR					
DAC-HK12DMM					
DAC-HK12BGC-2		12 Bits	3 μs	± ½ LSB	Voltage
DAC-HK12BMC-2					
DAC-HK12BMR-2					
DAC-HK12BMM-2					

Quick selection: High-speed D/A converters

MODEL	DESCRIPTION	RESOLUTION	SETTLING TIME, MAX	LINEARITY ERROR, MAX	OUTPUT
DAC-HF8BMC	Ultra-fast, Current output, 8, 10, and 12-bit converters	8 Bits	25 ns	± ½ LSB	Current
DAC-HF8BMR					
DAC-HF8BMM					
DAC-HF10BMC		10 Bits	25 ns	± ½ LSB	Current
DAC-HF10BMR					
DAC-HF10BMM					
DAC-HF12BMC		12 Bits	50 ns	± ½ LSB	Current
DAC-HF12BMR					
DAC-HF12BMM					
DAC-HI8B	Ultra-fast Compact Module	8 Bits	25 ns	± ½ LSB	Current
DAC-HI10B		10 Bits			
DAC-HI12B		12 Bits	50 ns		
DAC-DG12B1	High Speed Deglitched D/A	12 Bits	600 ns	± ½ LSB	Voltage
DAC-DG12B2					
DAC-8308	8-Bit composite Video D/A	8 Bits	7.5 ns (Typ.)	± ½ LSB	Voltage
DAC-8318	Ultra-fast 8 Bit D/A				

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The DAC-85/87s are a family of industry standard military and industrial D/A converters. This comprehensive line of DACs allows a choice of voltage or current output with either 12-bit complimentary binary or 3-digit complimentary BCD input coding.

These high-performance 12-bit, digital to analog converters are an ideal choice for systems applications, features a fast settling voltage output and a level controlled input storage register to ease data bus interfacing.

OUTPUT RANGES	INPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
(Current out) 0 to −2 mA ±1 mA (Voltage out) 0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V	C Binary	±20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	180
(Current out) 0 to −1.25 mA (Voltage out) 0 to ±2.5V 0 to +5V 0 to +10V	C BCD	±20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	
−100 mV to V+	Binary	10 ppm/°C of FSR	16 Pin DIP 18 Pin DIP	Monolithic	0° to 70°	194
0 to +5V 0 to +10V ±2.5V, ±5V ±10V	Binary	±20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	146
0 to ±2.5V 0 to +5V 0 to +10V	BCD	±20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	
0 to +5V 0 to +10V ±2.5V, ±5V ±10V	2C	±20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	

DATEL-INTERSIL's line of ultra-fast digital to analog converters combines high speed capability and high stability operation in one design. These devices are an ideal choice for innumerable applications including graphic display systems, CRT displays, fast computer control systems, and high-speed function generators.

OUTPUT RANGES	INPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
0 to +5 mA ±2.5 mA	Binary	20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	142
0 to +5 mA ±2.5 mA	Binary	20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	
0 to +5 mA ±2.5 mA	Binary	20 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	
0 to +5 mA ±2.5 mA	Binary	15 ppm/°C 20 ppm/°C	2 x 2 x 0.375 in (51 x 51 x 10 mm)	Module	0 to +70	—
0 to −10V, ±5V, ±10V ±5V, ±10V	C Binary C 2C	35 ppm/°C	4 x 2 x 0.4 in (102 x 51 x 10 mm)	Module	0 to +70	132
0 to −1.054V 0 to −1V	Binary		2 x 3 x 0.375 in (50 x 75 x 10 mm)	Module	0 to +70	196

Quick selection: High-resolution D/A converters

	MODEL	DESCRIPTION	RESOLUTION	SETTLING TIME, MAX	LINEARITY ERROR, MAX	OUTPUT
	DAC-HA14BC	Multiplying CMOS D/A	14 Bits	7.0 μs	±1 LSB	Current
	DAC-HA14BR					
	DAC-HA14BM					
	DAC-HR13B	Ultra-low drift, Low-profile Module	13 Bits	1 μs	±½ LSB	Current
	DAC-HR14B		14 Bits			
	DAC-HR15B		15 Bits		±1 LSB	
	DAC-HR16B		16 Bits		±2 LSB	
	DAC-HP16BGC	Complete Self-contained Voltage output D/A	16 Bits	15 μs	±0.003%	Voltage
	DAC-HP16BMC					
	DAC-HP16BMR					
	DAC-HP16BMM					
	DAC-HP16DGC		4 Digits	15 μs	±0.005%	Voltage
	DAC-HP16DMC					
	DAC-HP16DMR					
	DAC-HP16DMM					
NEW	DAC-71-CSB-1	Low cost, high resolution Industry Standard Converters	16 Bits	1 μsec	±.003%	Current
NEW	DAC-71-COB-I					
NEW	DAC-71-CCD-I		4 Digits		±.005%	
NEW	DAC-71-CSB-V		16 Bits	10 μsec	±.003%	Voltage
NEW	DAC-71-COB-V					
NEW	DAC-71-CCD-V		4 Digits		±.005%	
NEW	DAC-72C-CSB-I	Industry Standard High-resolution D/A Converters	16 Bits	1 μs	±0.003%	Current
NEW	DAC-72C-COB-I					
NEW	DAC-72C-CCD-I		4 Digits		±0.005%	
NEW	DAC-72C-CSB-V		16 Bits	10 μs	±0.003%	Voltage
NEW	DAC-72C-COB-V					
NEW	DAC-72C-CCD-V		4 Digits		±0.005%	
NEW	DAC-72-CSB-I		16 Bits	1 μs	±0.003%	Current
NEW	DAC-72-COB-I					
NEW	DAC-72-CCD-I		4 Digits		±0.005%	
NEW	DAC-72-CSB-V		16 Bits	10 μs	±0.003%	Voltage
NEW	DAC-72-COB-V					
NEW	DAC-72-CCD-V		4 Digits		±0.005%	

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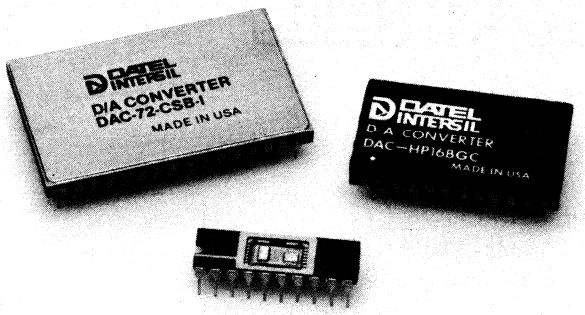
DATEL-INTERSIL offers a complete line of high-performance, low-cost, high-resolution digital to analog converters. The high resolution, performance and stability of these converters make them a good choice for precision applications such as speech and waveform reconstruction, precision ramp generators, and computer controlled testing.

The new DAC-72 is a fast, high-performance, 16-bit D/A converter. Voltage or current output models are available with either complementary 16-bit binary or complementary 4-digit BCD, TTL-compatible, input coding. The DAC-72 is completely pin and function compatible with competing devices of this type.



OUTPUT RANGES	INPUT CODING	GAIN TEMPCO	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
$\pm V_{REF}/V_{IN}$	Binary	5 ppm/°C	20-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	136
0 to −2 mA ±1 mA	C Binary	1.5 ppm/°C	4 x 2 x 0.375 in (102 x 51 x 10 mm)	Module	0 to +70	—
0 to +10V ±5V	C Binary	20 ppm/°C 15 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	150
0 to +10V	C BCD	20 ppm/°C 15 ppm/°C	24-pin DIP	Hybrid	0 to +70 −25 to +85 −55 to +125	150
0 to −2 mA ±1 mA	C Binary	45 ppm/°C	24 Pin Dip	Hybrid	0° to +70°C	178
0 to −2 mA	C BCD	45 ppm/°C	24 Pin Dip	Hybrid	0° to +70°C	178
0 to +10V ±10V	C Binary	15 ppm/°C	24 Pin DIP	Hybrid	0° to +70°	178
0 to +10V	C BCD	15 ppm/°C	24 Pin DIP	Hybrid	0° to +70°	178
0 to −2 mA ±1 mA	C Binary	45 ppm/°C	24-pin DIP	Hybrid	0 to +70	178
0 to −2 mA	C BCD	45 ppm/°C	24-pin DIP	Hybrid	0 to +70	178
0 to +10V ±10V	C Binary	15 ppm/°C	24-pin DIP	Hybrid	0 to +70	178
0 to +10V	C BCD	15 ppm/°C	24-pin DIP	Hybrid	0 to +70	178
0 to −2 mA ±1 mA	C Binary	35 ppm/°C	24-pin DIP	Hybrid	−25 to +85	178
0 to −2 mA	C BCD	35 ppm/°C	24-pin DIP	Hybrid	−25 to +85	178
0 to +10V ±10V	C Binary	15 ppm/°C	24-pin DIP	Hybrid	−25 to +85	178
0 to +10V	C BCD	15 ppm/°C	24-pin DIP	Hybrid	−25 to +85	178

Fast, 12-Bit Deglitched Digital-to-Analog Converter DAC-DG12B

FEATURES

- **±2 LSB Max. Glitch**
- **600 nsec. Settling Time**
- **Up to 2.5 MHz Update Rate**
- **12 Bit Resolution**
- **Self-Contained Module**

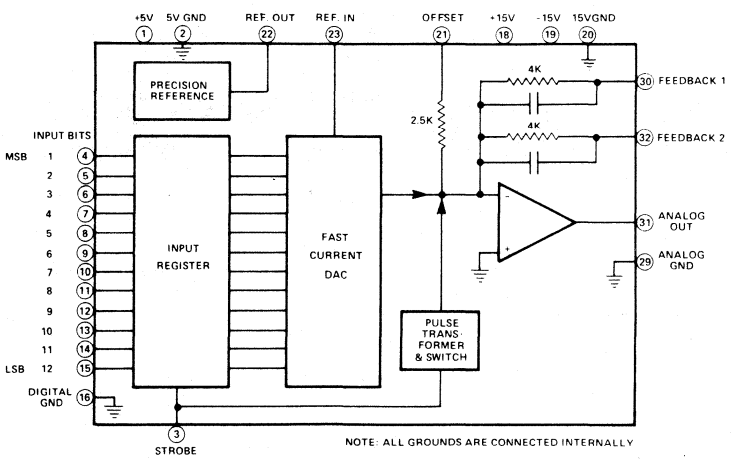
GENERAL DESCRIPTION

Model DAC-DG12B is a deglitched 12-bit D/A converter with a fast voltage output. The maximum output glitch amplitude is ±2 LSB's while settling time for a 10 volt output change is 600 nsec. to 1 LSB. For a 10 volt change to 1% the settling time is 250 nsec., and for small output changes it is only 400 nsec., permitting update rates as fast as 2.5 MHz.

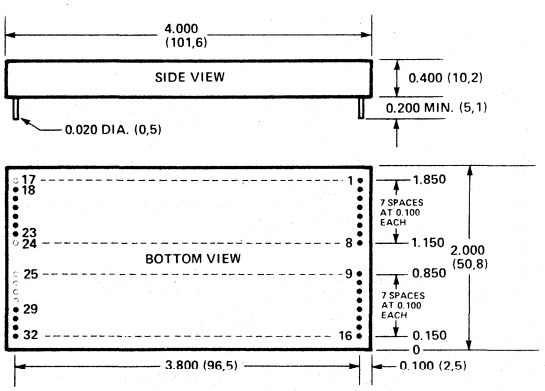
The unique circuit design of the DAC-DG12B realizes both small size and low price at the same time. Unlike other deglitched DAC's which are comprised of several inter-connected modules mounted on a circuit card, the DAC-DG12B is completely self-contained in a compact 4 x 2 x 0.4 inch (102 x 51 x 10 mm) module. It consists of several optimized circuit functions: digital input register, ultra-fast 12-bit current DAC, stable Zener voltage reference, fast deglitching switch, and a fast output operational amplifier.

The DAC-DG12B has three voltage output ranges determined by external pin connection: 0 to −10 V, ±5V and ±10 V. Output current is ±10 mA with output short circuit protection; for higher output current requirements an external current booster amplifier may be connected inside the feedback loop of the output amplifier. There are two input coding options: complementary binary complementary offset binary or complementary two's complement.

The DAC-DG12B is an ideal device for fast CRT display applications and for other test and measurement applications where monotonic output changes are required.



MECHANICAL DIMENSIONS—INCHES (MM)



NOTE: OPEN HOLES DESIGNATE OMITTED PINS

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	-5 V POWER
2	5 V GND
3	STROBE
4	BIT 1 IN MSB
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	BIT 11 IN
15	BIT 12 IN (LSB)
16	DIGITAL GND
18	+15 V POWER
19	-15 V POWER
20	15 V GND
21	OFFSET
22	REF. OUT
23	REF. IN
29	ANALOG GND
30	FEEDBACK 1
31	ANALOG OUT
32	FEEDBACK 2

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SPECIFICATIONS, DAC-DG12B
(Typical at 25° C, ±15 V and +5 V supplies unless otherwise noted)

INPUTS

Resolution	12 bits
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary [1] Complementary Two's Comp.[1]
Input Logic Level, bit ON ("0")	0V to +0.8 V
Input Logic Level, bit OFF ("1")	+2.0 V to +5.5 V
Logic Loading	1 TTL load
Input Strobe Pulse[2]	HI to LO transition causes transfer of data from register to DAC.
Input Strobe Loading	2 TTL loads

OUTPUTS

Output Voltage, unipolar[3]	0 to −10 V
Output Voltage, bipolar[3]	±5 V, ±10 V
Output Current, S.C. protected	±20 mA typ., ±10 mA min.
Output Impedance, DC	0.05 ohm

PERFORMANCE

Linearity Error	±½ LSB max.
Differential Nonlinearity	±½ LSB max.
Zero Error, before trimming	±½ LSB max.
Gain Tempco	±35 ppm/° C max.
Offset Tempco, bipolar	±15 ppm/° C max.
Zero Tempco, unipolar	±5 ppm/° C of FS max.
Diff. Nonlinearity Tempco	±2 ppm/° C of FS
Monotonicity	0° C to 70° C
Settling Time, 10 V change to 1 LSB	600 nsec. typ., 700 nsec. max.
Settling Time, 20 V change to 1 LSB	1.0 μsec. typ., 1.2 μsec. max.
Settling Time, 10 V change to 1%	250 nsec. max.
Settling Time, 20 V change to 1%	550 nsec. max.
Settling Time, ±4 LSB change[5]	400 nsec.
Slew Rate	50 V/μsec.
Glitch Amplitude[4]	±1 LSB typ., ±2 LSB max.
Glitch Area	250 mV-nsec.
Power Supply Rejection	0.01%/% supply

POWER REQUIREMENT	+15 VDC ±0.5 V @ 50 mA −15 VDC ±0.5 V @ 35 mA + 5 VDC ±0.25 V @ 230 mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0° C to 70° C
Storage Temperature Range	−55° C to +125° C
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2 mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	0.020" round, gold plated, 0.200 lg. min.
Weight	4 oz. max. (114 g)

NOTES

1. Because the analog output is inverted, in the bipolar mode the complementary offset binary code is equivalent to offset binary and the complementary two's complement code is equivalent to two's complement. See Technical Note 4.
2. Has same logic levels as data inputs.
3. Determined by external pin connection.
4. Measured with 20 MHz bandwidth oscilloscope at major carry (half scale) and at 7 transitions either side of major carry.
5. See Technical Note 7.

TECHNICAL NOTES

1. The sequence of operations inside the DAC-DG12B after the input strobe changes from HI to LO are:
   a. the pulse transformer and switch are activated and turn ON
   b. within 11 nanoseconds (typically) the data in the input register is transferred to the current DAC
   c. during the next 19 nanoseconds (typically) the DAC output current changes
   d. after 30 nanoseconds (typically) from the strobe change the pulse transformer and switch are deactivated, turning OFF
   e. the output amplifier begins to change to its new output value
2. A 5 nanosecond minimum setup time is required for the input data to be valid before the input strobe goes from HI to LO. The input strobe then should not go HI again for at least 40 nanoseconds.
3. The maximum update rate for the DAC-DG12B is 2.5 MHz, based on the 400 nanosecond settling time for small output changes (±4 LSB's max.). For 10 V changes to 1% of final value the maximum update rate is 4 MHz and for 10 V changes to within 1 LSB of final value the maximum update rate is 1.6 MHz.
4. From the coding tables it should be noted that each model of the DAC-DG12B has its coding defined in two ways when operating in bipolar mode. For the DAC-DG12B1 the complementary offset binary coding with inverted (negative) analog output is the same as offset binary coding with noninverted (positive) analog output except for an analog shift of 1 LSB. The converter therefore can be externally calibrated for either code. For the DAC-DG12B2 the complementary two's complement coding with inverted (negative) analog output is the same as two's complement coding with noninverted (positive) analog output except for an analog shift of 1 LSB.
5. The DAC-DG12B is internally calibrated at zero for unipolar operation, with a zero error of ±½ LSB maximum. In many applications, therefore, no external zero adjustment is required. For exact calibration the external zero adjustment should be used. The DAC-DG12B2 operates in unipolar mode except that its input code is complementary binary with the MSB inverted.
6. For higher output current drive capability a wideband current booster amplifier with unity voltage gain may be enclosed inside the feedback loop of the output amplifier.
7. The DAC-DG12B can be updated at up to 10 MHz with partial settling. This mode can be useful in some applications such as fast CRT displays. The DAC's output is integrated by the CRT deflection amplifier, resulting in a continuous, monotonic deflection signal that is offset by a small amount from its theoretical value. This small offset is the sole effect of the D/A's partial settling.

ORDERING INFORMATION

MODEL	CODING
DAC-DG12B1	Comp. Binary/Comp. Offset Binary
DAC-DG12B2	Comp. Two's Complement

Mating Socket: DILS-2, 2 Req'd Per Unit
Trimming Potentiometers: TP100 (100Ω), TP10K (10KΩ)

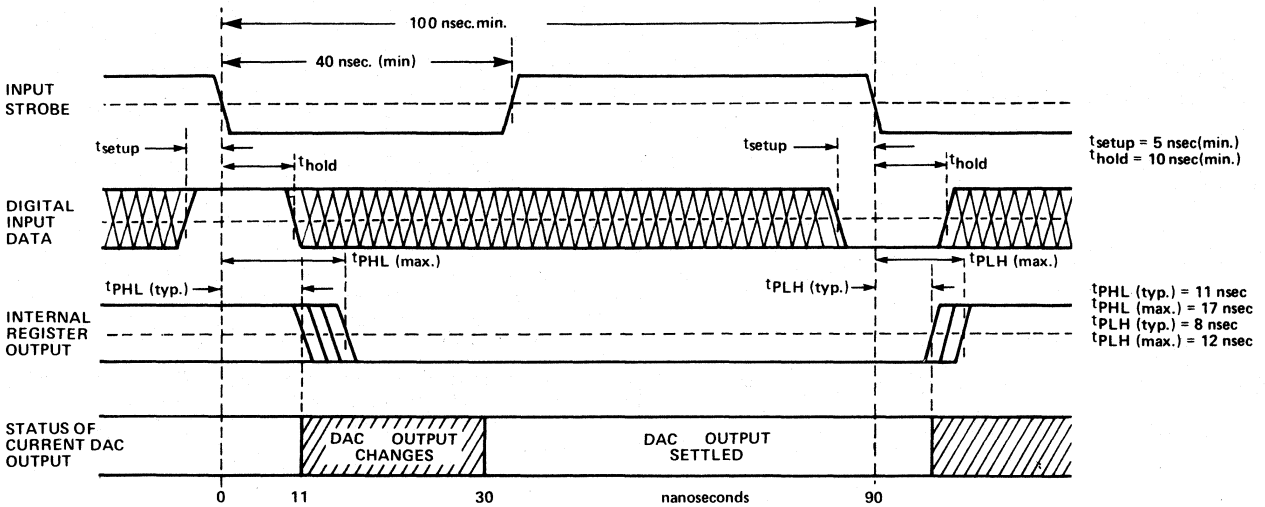
For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	−25°C to +85°C Operation
−EXX-HS	−55°C to +85°C Operation with Hermetically sealed semiconductor components

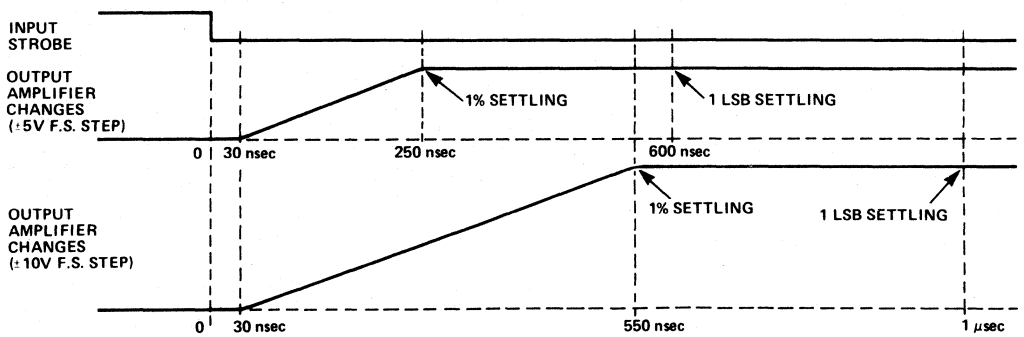
THE DAC-DG12B IS COVERED BY GSA CONTRACT

TIMING DIAGRAMS

INTERNAL TIMING



EXTERNAL TIMING



CODING TABLES

UNIPOLAR OPERATION

SCALE	VOLTAGE RANGE	DAC-DG12B1
	0 TO −10 V	COMP. BINARY
0	0.0000	1111 1111 1111
0-1 LSB	−0.0024	1111 1111 1110
−¼FS	−2.5000	1011 1111 1111
−½FS	−5.0000	0111 1111 1111
−¾FS	−7.5000	0011 1111 1111
−FS + 1 LSB	−9.9976	0000 0000 0000

BIPOLAR OPERATION

SCALE	VOLTAGE RANGE		DAC-DAC-DG12B1		DAC-DG12B2	
	±5 V	±10 V	COMP. OFFS. BIN	OFFSET BINARY	COMP. 2's COMP.	2'S COMPLEMENT
+FS	+5.0000 V	+10.0000 V	1111 1111 1111		0111 1111 1111	
+FS-1 LSB	+4.9976	+9.9951	1111 1111 1110	1111 1111 1111	0111 1111 1110	0111 1111 1111
0 + 1 LSB	+0.0024	+0.0049	1000 0000 0000	1000 0000 0001	0000 0000 0000	0000 0000 0001
0	0.0000	0.0000	0111 1111 1111	1000 0000 0000	1111 1111 1111	0000 0000 0000
−FS + 1 LSB	−4.9976	−9.9951	0000 0000 0000	0000 0000 0001	1000 0000 0000	1000 0000 0001
−FS	−5.0000	−10.000		0000 0000 0000		1000 0000 0000

CONNECTIONS AND CALIBRATION

CALIBRATION PROCEDURE

Select the desired output voltage range (0 to −10 V, ±5 V, or ±10 V) and make the connections shown in the diagrams below. To calibrate refer to the coding tables on the previous page.

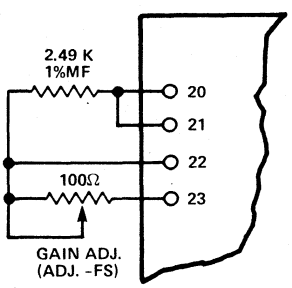
UNIPOLAR OPERATION (0 TO −10 V OUTPUT)

1. **Zero Adjustment:** Set the digital input code to 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.0000 V output.
2. **Gain Adjustment:** Set the digital input code to 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give −9.9976 V output.

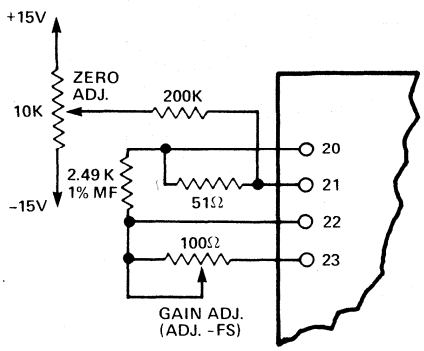
BIPOLAR OPERATION (±5 V OR ±10 V OUTPUT)

1. **Offset Adjustment:** Set the digital input code to 0111 1111 1111 (comp. offset binary), 1000 0000 0000 (offset binary), 1111 1111 1111 (comp. two's complement), or 0000 0000 0000 (two's complement) and adjust the BIPOLAR OFFSET ADJ. potentiometer to give 0.0000 V output.
2. **Gain Adjustment:** Set the digital input code to 0000 0000 0000 (comp. offset binary), 0000 0000 0001 (offset binary), 1000 0000 0000 (comp. two's complement), or 1000 0000 0001 (two's complement) and adjust the GAIN ADJ. potentiometer to give −4.9976 V output (for ±5 V range) or −9.9951 V output (for ±10 V range).
3. Repeat steps 1 and 2 to recheck adjustments.

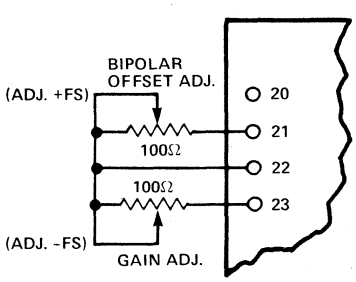
UNIPOLAR OPERATION—NO ZERO ADJ.



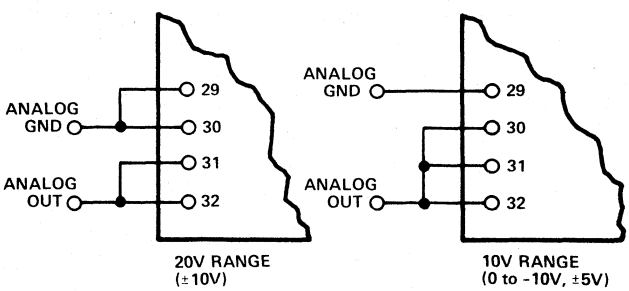
UNIPOLAR OPERATION—WITH ZERO ADJ.



BIPOLAR OPERATION



OUTPUT CONNECTIONS



Precision, Multiplying CMOS D/A Converters DAC-HA Series

FEATURES

- **10, 12 & 14 Bit Binary Models**
- **3 Digit BCD Model**
- **20 MHz Reference Bandwidth**
- **2 ppm/°C Gain Tempco**
- **+5V and +15V Supply Versions**
- **Input Protected**

GENERAL DESCRIPTION

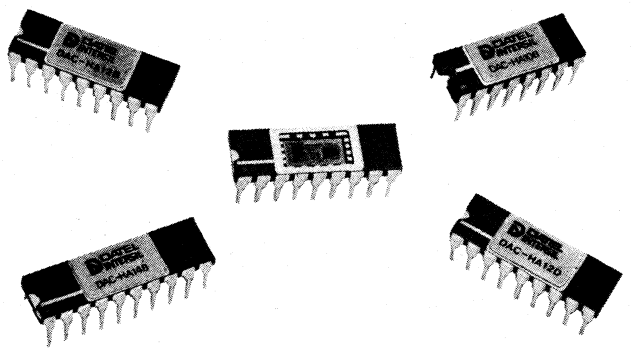
The DAC-HA Series are new, high performance multiplying digital to analog converters specifically designed for critical applications. The series features 10, 12, and 14 bit models and a 3 digit BCD model with a choice of either +5V or +15V power supply options. They are fabricated with advanced thin-film hybrid technology combining low ON-resistance CMOS switches with a precision laser trimmed R-2R ladder network. The ladder network is deposited on glass to realize low distributed capacitance resulting in a 20 MHz minimum reference bandwidth. Digital and power supply inputs are protected against overvoltage and latchup.

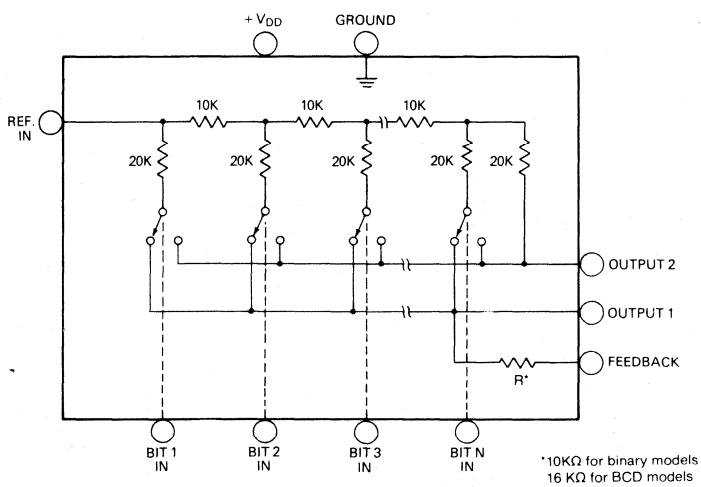
The DAC-HA series offer significant performance advantages over similar monolithic multiplying DAC's while retaining the industry 7500 series pin compatibility. Tightly controlled process parameters hold the ladder resistance to 10K ohms ±30% rather than the −50%, +100% tolerance common to monolithic versions. Close temperature tracking between the R-2R ladder and the feedback resistor results in a typical gain tempco of 2 ppm/°C. Linearity error is ±½ LSB max. for the 10 and 12 bit models and ±1 LSB max. for the 14 bit model.

The +5V supply versions draw only 1 μA of supply current while the +15V supply versions draw 1.4 mA; both have optimized accuracy at the specified supply voltages. Different models are also available for three standard operating temperature ranges along with MIL-STD-883 level B versions. The units are packaged in hermetically sealed 16, 18, or 20 pin ceramic packages for the 10, 12, and 14 bit verisons respectively.

Applications include digitally controlled attenuators, automatic gain control circuits, CRT character generation, one, two or four quadrant multiplier circuits, one or two quadrant divider circuits, complex function circuits and automatic bridge circuits.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.





INPUT/OUTPUT CONNECTIONS

DAC-HA10B

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN (LSB)
14	+VDD
15	REFERENCE IN
16	FEEDBACK

DAC-HA12B, 12D

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	BIT 11 IN
15	BIT 12 IN (LSB)
16	+VDD
17	REFERENCE IN
18	FEEDBACK

DAC-HA14B

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	BIT 11 IN
15	BIT 12 IN
16	BIT 13 IN
17	BIT 14 IN (LSB)
18	+VDD
19	REFERENCE IN
20	FEEDBACK

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SPECIFICATIONS, DAC-HA SERIES Typical at 25°C. V_{REF} = +10V. +5V standard or +15V optional[1] power supply

	DAC-HA14B	DAC-HA12B	DAC-HA12D	DAC-HA10B
MAXIMUM RATINGS				
V_{DD}, +5V Supply Option	+15V, −10V	*	*	*
V_{DD}, +15V Supply Option	+40V, −30V	*	*	*
Logic Input Voltage	+10V, −5V	*	*	*
Reference Input Voltage	±25V	*	*	*
Output 1 or Output 2 Voltage	+5V, −0.5V	*	*	*
Feedback Resistor to Gnd	±25V	*	*	*
INPUTS				
Resolution	14 Bits	12 Bits	12 Bits	10 Bits
Coding, Unipolar Operation	Straight Binary	*	BCD	*
Coding, Bipolar Operation	Offset Binary	*	—	*
Logic Threshold, Bit ON ("1")[2]	≥+4.0V	*	*	*
Logic Threshold, Bit OFF ("0")[2]	≤+1.0V	*	*	*
Logic Input Current[3]	±1 μA	*	*	*
Reference Input Voltage Range	±12V	*	*	*
Reference Input Resistance	10K ±30%	*	*	*
Reference Input Resistance vs Temp.	0 to +50 ppm/°C	*	*	*
OUTPUTS				
Output Current Range, Either Output	$\pm V_{REF}/R_{IN}$	*	*	*
Output Capacitance, Output 1[4]	260 pF	260 pF	260 pF	55 pF
Output Capacitance, Output 2[4]	160 pF	160 pF	160 pF	18 pF
Output Capacitance, Output 1[5]	160 pF	160 pF	160 pF	18 pF
Output Capacitance, Output 2[5]	260 pF	260 pF	260 pF	55 pF
PERFORMANCE				
Integral Linearity Error[6], max.	±1 LSB	±½ LSB	±½ LSB	±½ LSB
Differential Linearity Error[6]	±½ LSB typ. ±1 LSB max.	±¼ LSB typ. ±½ LSB max.	±¼ LSB typ. ±½ LSB max.	±¼ LSB typ. ±½ LSB max.
Differential Linearity Error Over Temp[6]	±2 LSB max.	±1 LSB max.	±1 LSB max.	±1 LSB max.
Gain Linearity Error, max.	±1 LSB	±½ LSB	±½ LSB	±½ LSB
Gain Error, Before Trimming[7]	+0, −0.2%	*	*	*
Output Leakage Current, max.[8]	100 pA	100 pA	100 pA	50 pA
Gain Temp. Coefficient, ppm/°C[9]	2 typ, 5 max.	2 typ, 5 max.	2 typ, 5 max.	7 typ, 20 max.
Monotonicity	At 25°C	Over Temp Range	Over Temp Range	Over Temp Range
Output Current Settling Time, max.[10]	7 μsec.	5 μsec.	5 μsec.	1.3 μsec.
Reference Input Bandwidth, −3 dB	20 MHz	*	*	*
Feedthrough at 20 KHz	0.025%	0.025%	0.025%	0.01%
Power Supply Rejection	5 ppm of FSR/%	5 ppm of FSR/%	5 ppm of FSR/%	0.01% of FSR/%
POWER REQUIREMENT				
Standard Version Supply Voltage	+5 VDC	*	*	*
Standard Version Supply Range	+3V to +7.5V	*	*	*
Standard Version Supply Current, max.	1 μA	*	*	*
Optional Version Supply Voltage[1]	+15 VDC	*	*	*
Optional Version Supply Range	+7.5V to +20V	*	*	*
Optional Version Supply Current, max.	1.4 mA	*	*	*
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range, C Suffix	0°C to 70°C	*	*	*
R Suffix	−25°C to +85°C	*	*	*
M Suffix	−55°C to +125°C	*	*	*
Storage Temp. Range	−65°C to +150°C	*	*	*
Package Type, Ceramic	20 Pin DIP	18 Pin DIP	18 Pin DIP	16 Pin DIP

*Specification same as first column.

NOTES:

1. The optional +15V version is designated by the Suffix −1.
2. Interfaces with TTL logic. See Technical Notes
3. Over Operating Temperature Range
4. All Digital Inputs HI
5. All Digital Inputs LO
6. $V_{OUT}\,1 = V_{OUT}\,2 = \pm 200$ mV
7. Adjustable to Zero
8. At +125°C Leakages are 100 nA and 50 nA max. respectively.
9. Using feedback resistor.
10. To ½ LSB for full scale digital input change.

THEORY OF OPERATION

The circuit of the DAC-HA series uses a precision, thin-film R-2R ladder network with R = 10K ohms ±30%, as shown in Figure 1. An external reference source is applied at the input of the network, and, depending on the digital input code, the resulting current is split between the Output 1 and Output 2 terminals. The switches at the bottom of the 20K network resistors are low on-resistance, single pole double throw CMOS devices of the type shown in Figure 2. The equivalent input impedance seen by the reference source is shown in Figure 3.

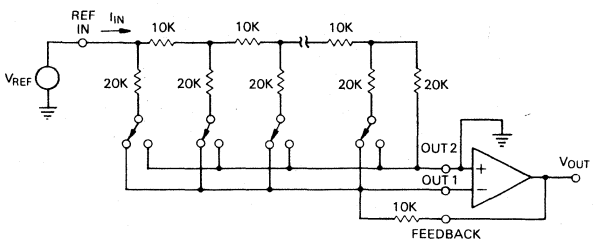


Figure 1. PRECISION DAC-HA CIRCUIT

From the reference end of the network, the input current divides in two at each successive junction as it flows down the ladder. It should be noted that the 20K terminating resistor at the right end of the network goes to Output 2 in the DAC-HA series rather than to ground as in monolithic devices of the 7500 type. The output currents at Output 1 and Output 2 represent the digital complements of one another except for a 1 LSB analog difference. The result is that when Output 1 and Output 2 are added together they always sum to the reference input current.

Furthermore, with a digital input code of 1000....0000, the two output currents are precisely equal. Therefore, in 4 quadrant multiplying applications where the two outputs are subtracted, the result is zero. With 7500 series monolithic units these currents do not cancel each other and an additional 1 LSB offset current must be externally provided to give exact cancellation.

The DAC-HA series are designed to be used with an external operational amplifier which converts the current output into a voltage. Since the feedback resistor tracks the ladder network with temperature, the resulting gain tempco is ±2 ppm/°C typical except for the 10 bit model. If the output current is used without the internal feedback resistor, the output current tempco is then 0 to −50 ppm/°C.

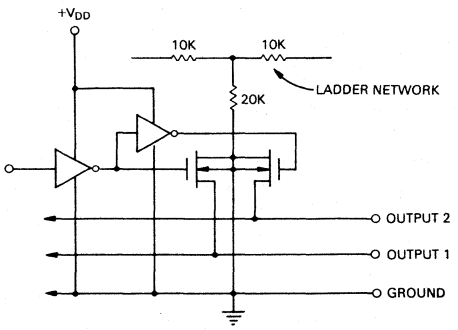


Figure 2. SINGLE POLE DOUBLE THROW CMOS SWITCH

With an external amplifier at Output 1 the output voltage ranges from zero to $-V_{REF}$ $(1\text{-}2^{-n})$, depending on the input code. If an external amplifier is used at Output 2 with the same value of feedback resistor, the output voltage ranges from zero to $-V_{REF}$ depending on input code.

The DAC-HA series have optimized linearity for the two power supply options +5V and +15V. It should be noted that while 7500 series devices operate over a +5V to +15V supply range, nonlinearity increases as the supply voltage is decreased from +15V.

To realize the specified linearity, it is necessary to carefully zero the input offset voltage of the amplifier or amplifiers used at the outputs. The input offset voltage should be zeroed to less than ±0.1 mV in order to have negligible effect on accuracy. Actually the two offset voltages can be as large as ±200 mV if they are within ±0.1 mV of each other.

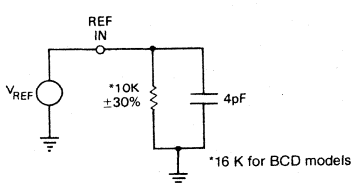


Figure 3. EQUIVALENT INPUT IMPEDANCE OF DAC-HA REFERENCE INPUT

CODING TABLE

CODE	SCALE	OUTPUT 1	OUTPUT 2
1111...11	FS-1 LSB	$I_{IN}(1\text{-}2^{-n})$	$I_{IN}(2^{-n})$
1100...00	+3/4 FS	$I_{IN}(2^{-1}+2^{-2})$	$I_{IN}(2^{-2})$
1000...01	+1/2 FS + 1 LSB	$I_{IN}(2^{-1}+2^{-n})$	$I_{IN}(2^{-1}-2^{-n})$
1000...00	+1/2 FS	$I_{IN}(2^{-1})$	$I_{IN}(2^{-1})$
0100...00	+1/4 FS	$I_{IN}(2^{-2})$	$I_{IN}(2^{-1}+2^{-2})$
0000...01	+1 LSB	$I_{IN}(2^{-n})$	$I_{IN}(1\text{-}2^{-n})$
0000...00	0	$I_{IN}(0)$	$I_{IN}(1)$

NOTE: $I_{IN} = \frac{V_{REF}}{R_{IN}}$

where R_{IN} is ladder network impedance, or 10k ±30%

OUTPUT EQUATIONS

$$\text{OUTPUT 1} = I_{IN}(a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + ... + a_n 2^{-n})$$

$$\text{OUTPUT 2} = I_{IN}(\bar{a}_1 2^{-1} + \bar{a}_2 2^{-2} + \bar{a}_3 2^{-3} + ... + \bar{a}_n 2^{-n} + 2^{-n})$$

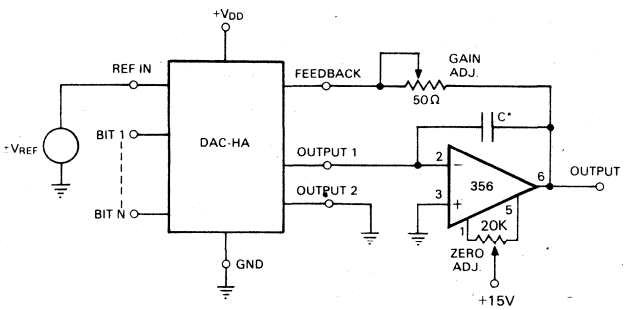
"a's" are digital coefficients, 0 or 1.
n = converter resolution in bits

TECHNICAL NOTES

1. CAUTION. The DAC-HA series contains MOS devices and should be handled carefully to prevent static charge pickup that might damage the units. The converters should be kept in conductive foam until ready for installation. During installation the user should be grounded by means of a conductive wrist strap. Do not insert or remove these devices from their sockets unless power is turned off.
2. Unused digital inputs should be connected to ground or to +5V, never left open.
3. In general, pull-up resistors are not required for TTL logic interfacing. The DAC-HA series will interface directly with all standard TTL circuits and operate within specifications.
4. The logic input voltages are stated as $\leq +1.0V$ for a logic "0" and $\geq +4.0V$ for a logic "1" at the recommended power supply voltages of +5V or +15V. For other supply voltages in the specified range, the logic "1" level becomes $V_{DD}-1$ for the 5V version and $\frac{V_{DD}}{3}-1$ for the +15V version.
5. For interfacing with HNIL or CMOS logic where logic HI is greater than +5V, CD4050 interface circuits should be used and connected as shown in the applications diagram.
6. The DAC-HA series devices are protected against both power supply and logic input overvoltages by means of series thin-film resistors. The result is that these devices are free from latch-up problems which have been associated with some CMOS multiplying DAC circuits in the past.
7. While the DAC-HA series gives optimum accuracy at recommended supply voltage and at room temperature, the maximum linearity error is ±1 LSB over both specified supply range and temperature range for the 10 and 12 bit models and is ±2 LSB for the 14 bit model.
8. The supply current is given as the quiescent value. The current increases to 200 μA max. for the +5V version and 1.6 mA max. for the +15V version with all bits switched at a 10 KHz rate at 50% duty cycle. Supply current increases at the rate of 1 μA per KHz of switching frequency.
9. The noise output of the DAC-HA devices can be computed from the Johnson noise of the resistance between either output terminal and ground. This resistance varies with input code from 6.67K (based on nominal ladder resistance of 10K) to 30K for Output 2 and from 6.67K to infinity for Output 1. When using an output amplifier at either output the feedback resistor is then in parallel with the ladder resistance, and the noise gain of the amplifier must also be used in the computation.
10. Feedthrough, which is specified at 20 KHz, is due to capacitive coupling from the reference input to the output, and increases directly with frequency. The frequency of the reference input is only limited by the amount of feedthrough error.
11. With most output amplifiers a small feedback capacitor across the feedback resistor is necessary to compensate for the output capacitance of the DAC-HA. By using a small trim capacitor, the compensation can be adjusted for optimum response.
12. It is recommended that output amplifiers with less than 25 nA input bias current be used with the DAC-HA series. This permits precise adjustment of the output voltage to zero with all digital inputs OFF and at the same time assures that the input offset voltage is minimized. For most applications the 356 type op amp is an excellent choice. For faster response, however, Datel's AM-462 is recommended.

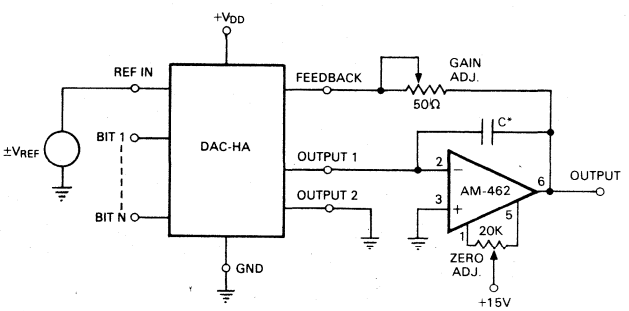
CONNECTIONS

DAC-HA CONNECTION WITH 356 OUTPUT AMPLIFIER



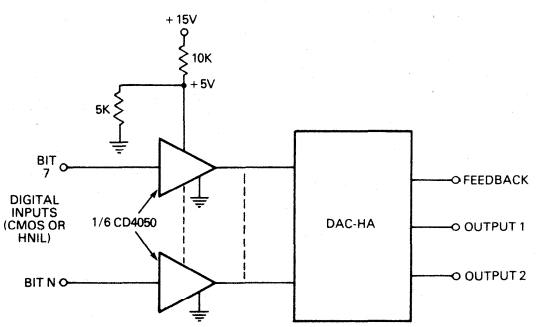
*Use 3 to 30pF trim capacitor and adjust for optimum step response.

DAC-HA CONNECTION FOR FAST VOLTAGE OUTPUT USING DATEL AM-462 MONOLITHIC OPERATIONAL AMPLIFIER



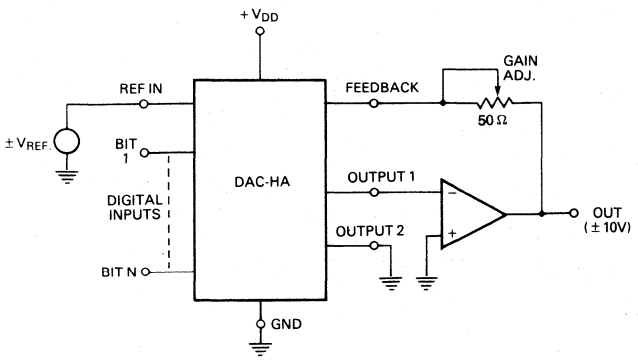
*Use 3 to 30pF trim capacitor and adjust for optimum step response.

CMOS OR HNIL LOGIC INTERFACE

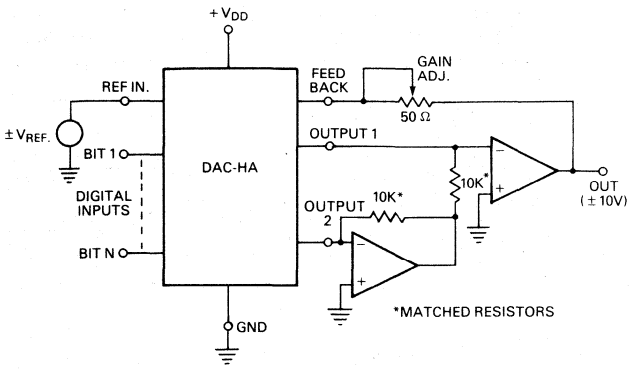


APPLICATIONS

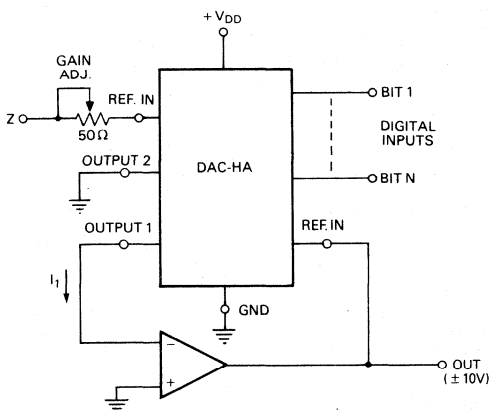
2 QUADRANT MULTIPLICATION (DIGITAL ATTENUATOR)



4 QUADRANT MULTIPLICATION



DIVISION CIRCUIT USING DAC-HA



$(D) = \text{Digital Input} = (a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n})$

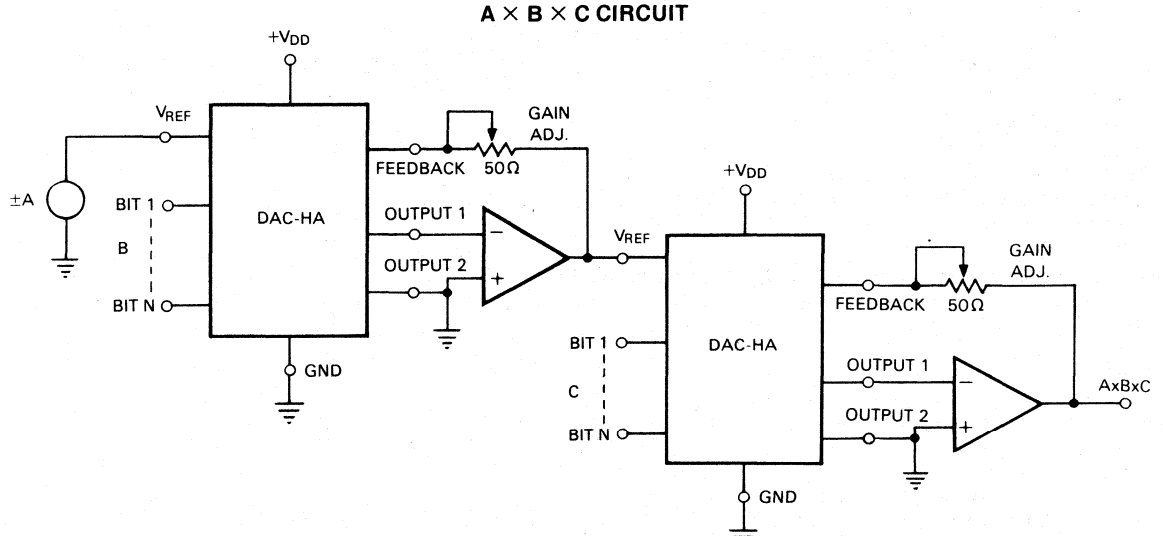
$I_1 = \dfrac{\text{OUT (D)}}{R}$ where R is internal ladder resistance = 10K

$I_1 = \dfrac{-Z}{R}$ R is feedback resistor which is matched to internal ladder resistance.

$\dfrac{\text{OUT (D)}}{R} = \dfrac{-Z}{R}$ $\quad \boxed{\text{OUT} = \dfrac{-Z}{(D)}}$

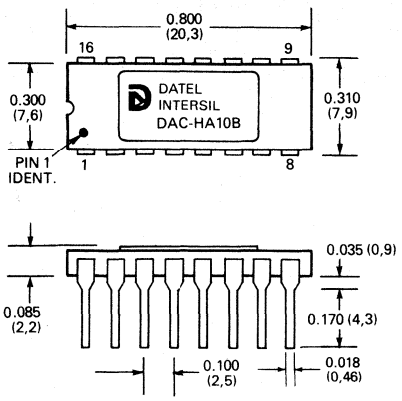
The circuit is stable for ±Z.

A × B × C CIRCUIT

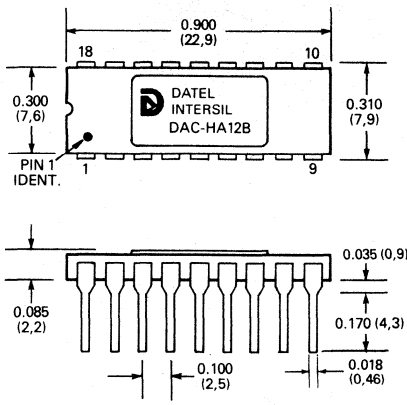


MECHANICAL DIMENSIONS—INCHES (MM)

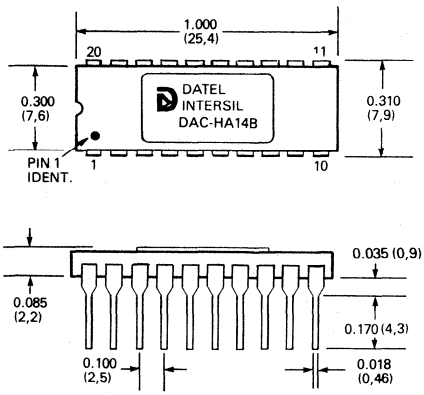
16-PIN DIP CERAMIC PACKAGE



18-PIN DIP CERAMIC PACKAGE



20-PIN DIP CERAMIC PACKAGE



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	POWER SUPPLY	PRICE (1-24)	MODEL	OPERATING TEMP. RANGE	POWER SUPPLY	PRICE (1-24)
DAC-HA10BC	0 to 70°C	+5 VDC		**DAC-HA10BC-1**	0 to 70°C	+15 VDC	
DAC-HA10BR	−25 to +85°C	+5 VDC		**DAC-HA10BR-1**	−25 to +85°C	+15 VDC	
DAC-HA10BM	−55 to +125°C	+5 VDC		**DAC-HA10BM-1**	−55 to +125°C	+15 VDC	
DAC-HA12BC	0 to 70°C	+5 VDC		**DAC-HA12BC-1**	0 to 70°C	+15 VDC	
DAC-HA12BR	−25 to +85°C	+5 VDC		**DAC-HA12BR-1**	−25 to +85°C	+15 VDC	
DAC-HA12BM	−55 to +125°C	+5 VDC		**DAC-HA12BM-1**	−55 to +125°C	+15 VDC	
DAC-HA12DC	0 to 70°C	+5 VDC		**DAC-HA12DC-1**	0 to 70°C	+15 VDC	
DAC-HA12DR	−25 to +85°C	+5 VDC		**DAC-HA12DR-1**	−25 to +85°C	+15 VDC	
DAC-HA12DM	−55 to +125°C	+5 VDC		**DAC-HA12DM-1**	−55 to +125°C	+15 VDC	
DAC-HA14BC	0 to 70°C	+5 VDC		**DAC-HA14BC-1**	0 to 70°C	+15 VDC	
DAC-HA14BR	−25 to +85°C	+5 VDC		**DAC-HA14BR-1**	−25 to +85°C	+15 VDC	
DAC-HA14BM	−55 to +125°C	+5 VDC		**DAC-HA14BM-1**	−55 to +125°C	+15 VDC	

Trimming Potentiometer: TP50 (50 ohms)
For high reliability versions of the DAC-HA series including units screened to MIL-STD-883 level B, contact factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

DATEL INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

Ultra-Fast Microelectronic D/A Converters DAC-HF Series

FEATURES

- **8, 10, 12 Bit Resolution**
- **Settling Times to 25 nsec.**
- **20 ppm/°C Tempco**
- **Unipolar or Bipolar Operation**
- **Current Output**
- **Internal Feedback Resistor**

GENERAL DESCRIPTION

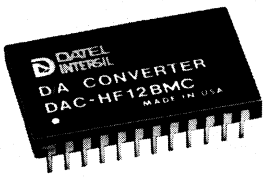
The DAC-HF series of hybrid DAC's are ultra high speed, current output devices. They incorporate state-of-the art performance in a miniature package, achieving maximum output settling times of 25 nanoseconds for the 8 and 10 bit models and 50 nanoseconds for the 12 bit model. They can be used to drive a resistor load directly for up to ±1V output or a fast operational amplifier (such as Datel-Intersil's AM-500) for higher voltage outputs with sub-microsecond settling times. A tapped feedback resistor and a bipolar offset resistor are included internally to give five programmable output voltage ranges with an external op amp.

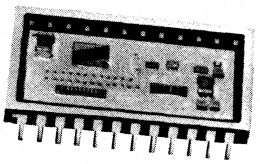
The DAC-HF design combines proven hybrid production techniques with advanced circuit design to realize high speed current switching. The design incorporates fast PNP current switches driving a low impedance R-2R thin film ladder network. The nichrome thin film resistor network is deposited by electron beam evaporation on a low capacitance substrate to assure high speed performance. The resistors are then functionally trimmed by laser for optimum linearity.

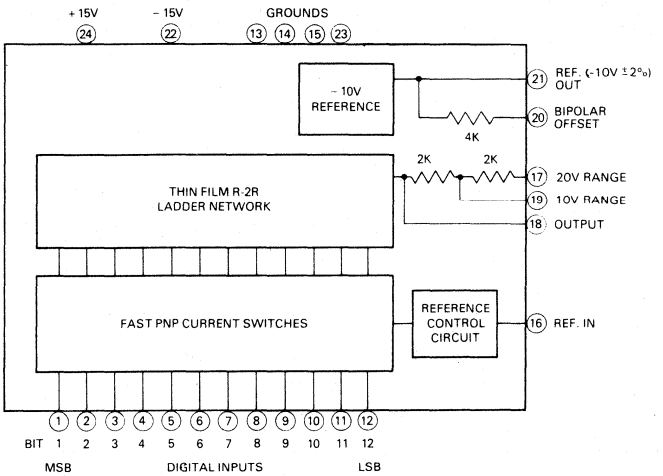
The digital inputs are TTL compatible and use straight binary coding for unipolar operation and offset binary coding for bipolar operation. Output current is 0 to +5 mA for unipolar operation and ±2.5 mA for bipolar operation into an output amplifier summing junction. Linearity is ±½ LSB, and the converters are monotonic over the operating temperature range specified for each. Gain temperature coefficient is ±20 ppm/°C maximum.

Applications for the DAC-HF series include high speed function generators, fast computer control systems, graphic display systems, and CRT displays.

Power supply requirement is ±15 VDC with less than 780 milliwatts consumption. The DAC-HF is available in models covering three operating temperature ranges.

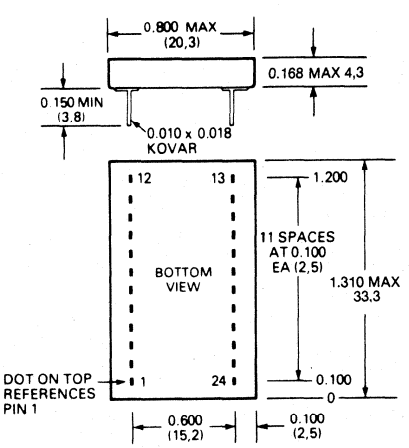






NOTE: FOR DAC-HF10B PINS 11 & 12 ARE NO CONNECTION
FOR DAC-HF8B PINS 9, 10, 11 & 12 ARE NO CONNECTION

MECHANICAL DIMENSIONS INCHES (MM)



NOTE PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	GROUND
2	BIT 2 IN	14	GROUND
3	BIT 3 IN	15	GROUND
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	20 V RANGE
6	BIT 6 IN	18	OUTPUT
7	BIT 7 IN	19	10 V RANGE
8	BIT 8 IN	20	BIPOLAR OFFSET
9	BIT 9 IN	21	REF. OUT
10	BIT 10 IN	22	-15 VDC
11	BIT 11 IN	23	GROUND
12	BIT 12 IN (LSB)	24	+15 VDC

DATEL INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-HF SERIES
(Typical at 25°C, ±15V supplies unless otherwise specified)

	8B	10B	12B
MAXIMUM RATINGS			
Positive Supply, Pin 24	+18V		
Negative Supply, Pin 22	−18V		
Digital Input Voltage, Pins 1 to 12	+15V		
INPUTS			
Resolution, Bits	8	10	12
Coding, Unipolar Output	Straight Binary		
Coding, Bipolar Output	Offset Binary		
Input Logic Level, Bit ON ("1")	+2.2 to +5.5V @ +40μA		
Input Logic Level, Bit OFF ("0")	0V to +0.8V @ 2.6mA		
OUTPUT			
Output Current Range, Unipolar	0 to +5 mA		
Output Current Range, Bipolar	±2.5mA		
Output Voltage Compliance	±1.2V		
Output Voltage Ranges[2]	0 to −5V 0 to −10V ±2.5V ±5V ±10V		
Output Resistance	400 ohms		
Output Capacitance	15 pF		
Output Leakage Current, All Bits OFF	15 nA		
PERFORMANCE			
Linearity Error, max	±1/2 LSB		
Differential Linearity Error, max	±1/2 LSB		
Diff. Linearity Tempco	±2 ppm/°C		
Monotonicity	Guaranteed over oper. temp. range		
Gain Tempco, max	±20 ppm/°C		
Offset Tempco, Bipolar, max	±10 ppm/°C of F.S.R.[3]		
Zero Tempco, max	±1.5 ppm/°C of F.S.R.[3]		
Settling Time, nsec. max.[1]	25	25	50
Power Supply Sensitivity	0.01%/% Supply		
POWER REQUIREMENT			
Supply Voltage	±15VDC ±0.5V		
Positive Quiescent Current, max.	30mA	35mA	40mA
Negative Quiescent Current, max.	12mA	12mA	12mA
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range	0°C to +70°C (BMC) −25°C to +85°C (BMR) −55°C to +125°C (BMM)		
Storage Temperature Range	−65°C to +150°C		
Package Type	24 Pin Ceramic DIP		
Pins	.010 x .018 inch Kovar		
Weight	0.2 oz. (6g.)		

NOTES:
1. Full scale current change to 1 LSB with 400Ω load.
2. With External Operational Amplifier.
3. F.S.R. is Full Scale Range, or the difference between minimum and maximum output values.

TECHNICAL NOTES

1. Proper operation of the DAC-HF series converters is dependent on good board layout and connection practices. Supplies should be bypassed as shown in the connection diagrams. Bypass capacitors should be mounted close to the converter, directly to the supply pins where possible.
2. Use of a ground plane is particularly important in high speed D to A converters as it reduces high frequency noise and aids in decoupling the digital inputs from the analog output. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The configuration of the ground plane directly below the DAC-HF is shown in the ground plane layout diagram. The remainder of the ground plane should include as much of the circuit board as possible.
3. When the converter is configured for voltage output with an external op-amp, the leads from the converter to the output amplifier should be kept as short as possible.
4. The high speed current switching technique used in the DAC-HF series inherently reduces the amplitude and duration of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011...1 to 100...0 or vice versa. At this time a skewing of the input codes can create a transition state code of 111...1. The duration of the "transition state code" is dependent on the degree of skewing but its effect is dependent on the speed of the DAC (an ultra-fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC). The effects of input skewing can be easily minimized through the use of a high-speed input register to match input switching times. The input register recommended for use with the DAC-HF is easily implemented with two Texas Instruments SN74S174 hex D-type flip-flops. This register will reduce glitches to a very low level and ensure fast output settling times.
5. Testing of the DAC-HF should be performed with a low capacitance test probe (such as a 10X probe). Care should be taken to assure the shortest possible connection between probe ground and circuit ground. Long probe ground leads may pick up environmental E.M.I. causing artifacts on the scope display, i.e. signals that do not originate at the unit under test.
6. Passive components used with the DAC-HF may be as indicated here: 0.1 μF and 1 μF bypass capacitors should be ceramic type and tantalum type respectively; the 400Ω output load is a 0.1% 10 ppm/°C metal film type; adjustment potentiometers are cermet types; other resistors may be ±10% carbon composition types.
7. Output voltage compliance is ±1.2V to preserve the linearity of the converter. In the bipolar mode the DAC-HF can be operated with no load to give an output voltage of ±1.0V. In the unipolar mode the load resistance must be less than 600Ω to give less than +1.2V output. The specified output currents of 0 to +5 mA and ±2.5 mA are measured into a short circuit or an operational amplifier summing junction.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL	PRICE (1-24)
DAC-HF8BMC	0° to +70°C	Hermetic	
DAC-HF8BMR	−25° to +85°C	Hermetic	
DAC-HF8BMM	−55° to +125°C	Hermetic	
DAC-HF10BMC	0° to +70°C	Hermetic	
DAC-HF10BMR	−25° to +85°C	Hermetic	
DAC-HF10BMM	−55° to +125°C	Hermetic	
DAC-HF12BMC	0° to +70°C	Hermetic	
DAC-HF12BMR	−25° to +85°C	Hermetic	
DAC-HF12BMM	−55° to +125°C	Hermetic	

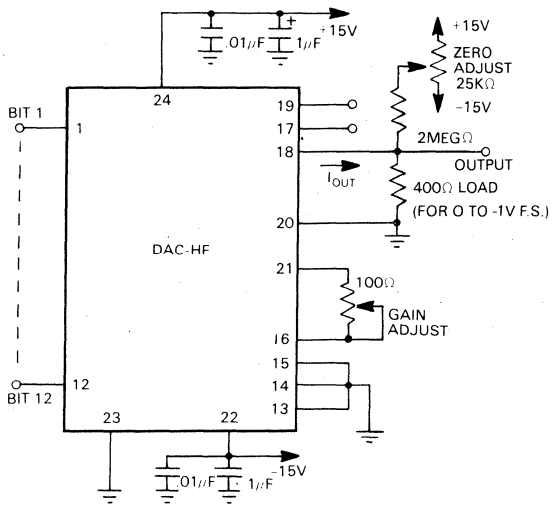
Mating Socket: DILS-3 (24-pin socket)
Trimming Potentiometers: TP-100 or TP25K

For high reliability versions of the DAC-HF series including units screened to MIL-STD-883 Level B, contact factory.

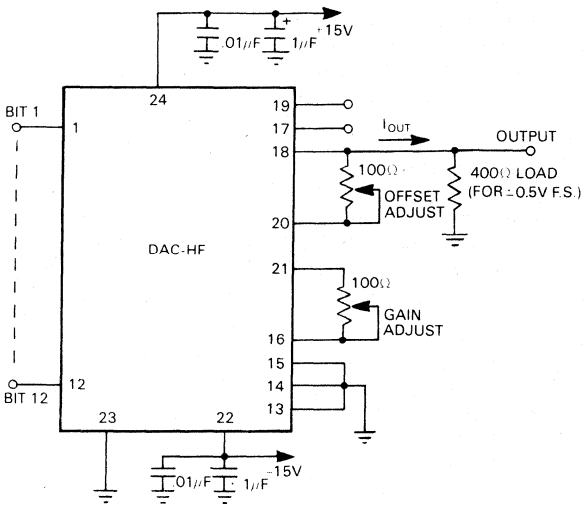
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CONNECTION AND CALIBRATION

UNIPOLAR CURRENT OUTPUT CONNECTIONS



BIPOLAR CURRENT OUTPUT CONNECTIONS



UNIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs LO and adjust the ZERO ADJUST potentiometer for a reading of 0V at the output.
3. Set all inputs HI and adjust the GAIN ADJUST potentiometer for a reading of −F.S. +ILSB (given in the coding table for 12 bit units).

BIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs LO and adjust the OFFSET ADJUST potentiometer for an output reading of +F.S., (given in the coding table for 12 bit units).
3. Set all inputs HI and adjust the GAIN ADJUST potentiometer for an output reading of −F.S. +1 LSB, (given in the coding table for 12 bit units).

CODING TABLES UNIPOLAR OUTPUT

UNIPOLAR SCALE	INPUT CODING STRAIGHT BINARY	ANALOG OUTPUT 0 to +1V F.S.	0 to −5V F.S.	0 to −10V F.S.
−F.S. +1 LSB	1111 1111 1111	+0.9998V	−4.9988V	−9.9976V
−¾ F.S.	1100 0000 0000	+0.7500V	−3.7500V	−7.5000V
−½ F.S.	1000 0000 0000	+0.5000V	−2.5000V	−5.0000V
−¼ F.S.	0100 0000 0000	+0.2500V	−1.2500V	−2.5000V
−1 LSB	0000 0000 0001	+0.0002V	−0.0012V	−0.0024V
0	0000 0000 0000	0.0000V	0.0000V	0.0000V

BIPOLAR OUTPUT

BIPOLAR SCALE	INPUT CODING OFFSET BINARY	ANALOG OUTPUT ±0.5V F.S.	±2.5V F.S.	±5V F.S.	±10V F.S.
−F.S.+1LSB	1111 1111 1111	+0.4998V	−2.4988V	−4.9976V	−9.9951V
−½ F.S.	1100 0000 0000	+0.1250V	−1.2500V	−2.5000V	−5.0000V
−1 LSB	1000 0000 0001	+0.0002V	−0.0012V	−0.0024V	−0.0049V
0	1000 0000 0000	0.0000V	0.0000V	0.0000V	0.0000V
+½ F.S.	0100 0000 0000	−0.1250V	+1.2500V	+2.500V	+5.0000V
+F.S.−1LSB	0000 0000 0001	−0.4998V	+2.4988V	+4.9976V	+9.9951V
+F.S.	0000 0000 0000	−0.5000V	+2.5000V	+5.0000V	+10.0000V

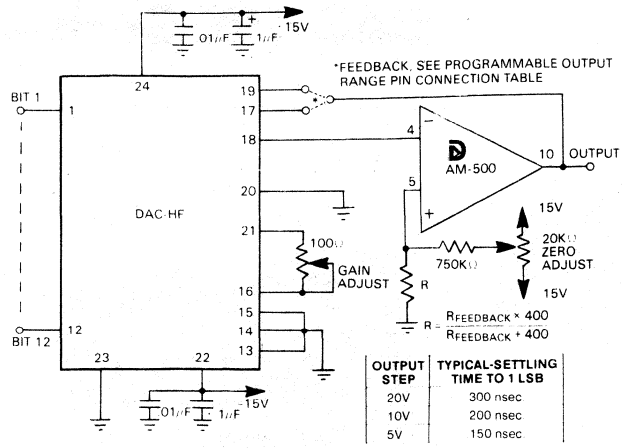
PROGRAMMABLE OUTPUT RANGE PIN CONNECTIONS

OUTPUT VOLTAGE RANGE	FEEDBACK CONNECTION	CONNECT THESE PINS TOGETHER
0 to −5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
0 to −10V	PIN 19	PIN 20 to PIN 23
±2.5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
±5V	PIN 19	PIN 20 to PIN 23
±10V	PIN 17	PIN 20 to PIN 23

In all Programmable Output Ranges PIN 18 connects to external OP-AMP inverting input

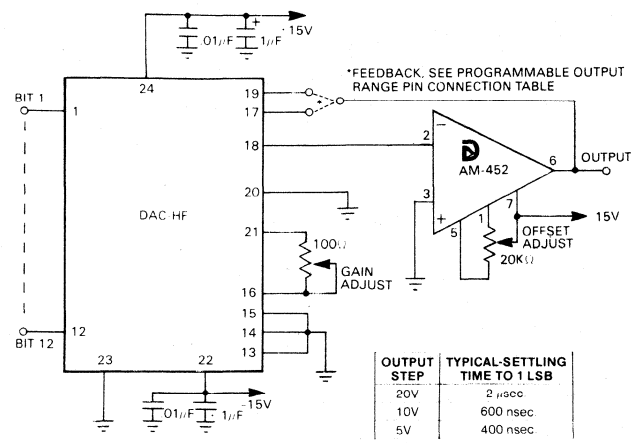
APPLICATIONS

ULTRA-FAST VOLTAGE OUTPUT



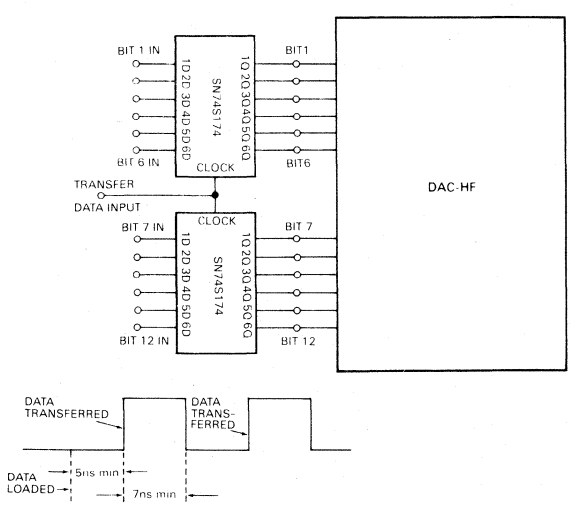
OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	300 nsec
10V	200 nsec
5V	150 nsec

FAST VOLTAGE OUTPUT CIRCUIT

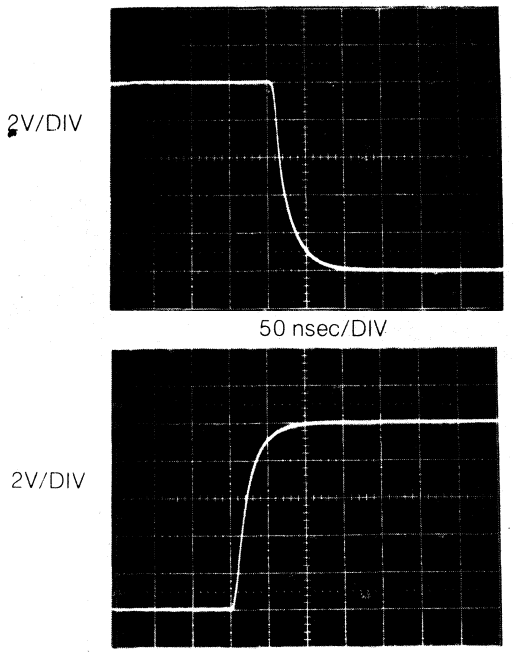


OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	2 μsec
10V	600 nsec
5V	400 nsec

HIGH SPEED INPUT REGISTER

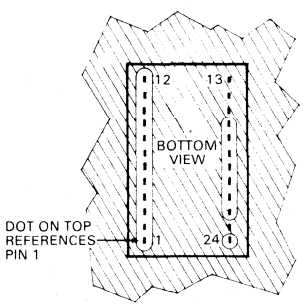


VOLTAGE OUTPUT WAVEFORMS

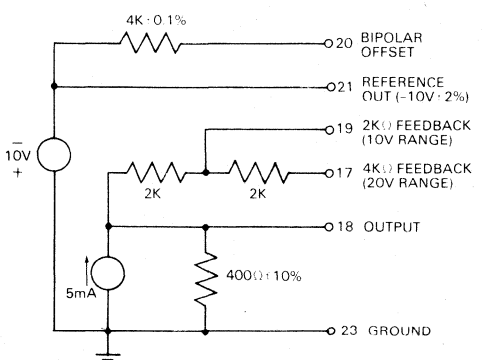


DAC-HF with AM-500, ±5V output full scale (10V) step

GROUND PLANE LAYOUT



EQUIVALENT OUTPUT CIRCUIT



12-Bit Hybrid DAC's with Input Register DAC-HK Series

FEATURES

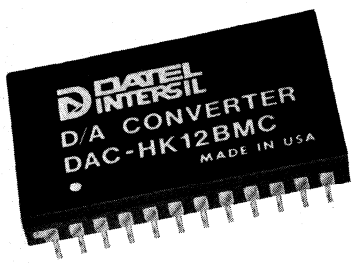
- **12-Bit Resolution**
- **20 ppm/°C Tempco**
- **Input Register**
- **3 Coding Options**
- **Fast Settling Time**

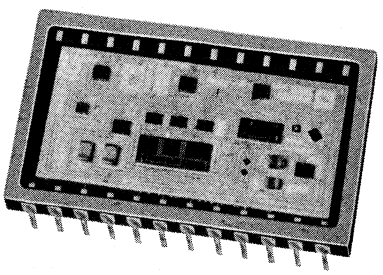
GENERAL DESCRIPTION

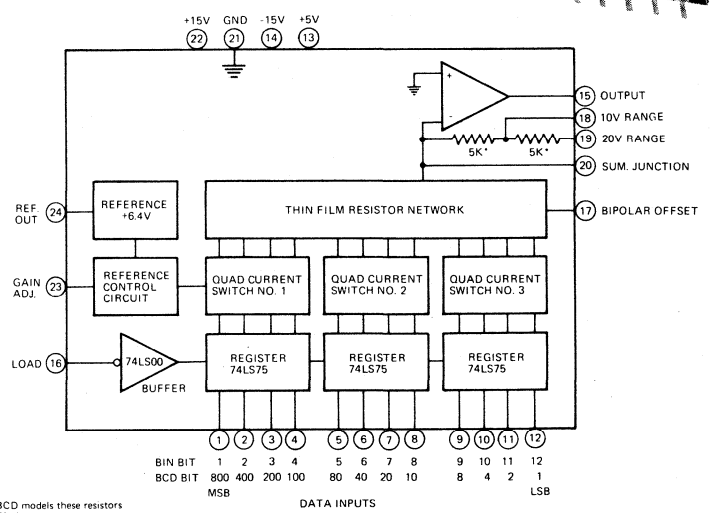
The DAC-HK series hybrid D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high data in the storage register is held, and when the load input is low data is transferred through to the DAC. There are three basic models available by coding option: binary, BCD, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5 V, 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V.

The DAC-HK design is based on proven, reliable thin film hybrid technology. Quad current switches are combined with a low T.C. thin film resistor network and a low T.C. Zener reference to achieve better than 20 ppm/°C gain tempco. Optimum linearity is attained by functional laser trimming of the thin film nichrome resistors. The tight temperature tracking of these resistors and the quad current switch transistors result in a differential linearity error tempco of only 2 ppm/°C. Each model of the DAC-HK series is monotonic over its operating temperature range.

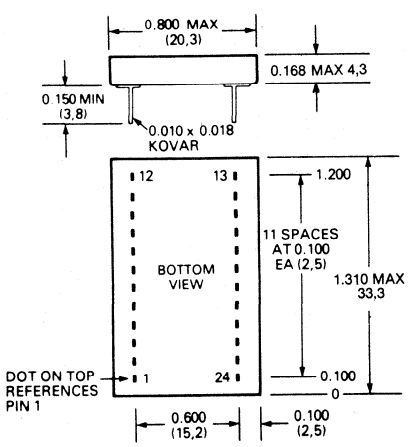
The converters are cased in 24-pin ceramic packages. Models are available for three different operating temperature ranges: 0 to 70, −25 to +85, and −55 to +125 degrees Centigrade. High reliability versions of each model are also available screened to MIL-STD-883 level B. Power requirement is ±15 VDC and +5 VDC. Total power dissipation is 900 milliwatts.







MECHANICAL DIMENSIONS - INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	+5 VDC
2	BIT 2 IN	14	−15 VDC
3	BIT 3 IN	15	OUTPUT
4	BIT 4 IN	16	LOAD
5	BIT 5 IN	17	BIPOLAR OFF.
6	BIT 6 IN	18	10 V RANGE
7	BIT 7 IN	19	20 V RANGE
8	BIT 8 IN	20	SUM. JUNCTION
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15 VDC
11	BIT 11 IN	23	GAIN ADJ.
12	BIT 12 IN (LSB)	24	REF. OUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-HK SERIES
(Typical at 25°C, ±15 V and +5 V supplies unless otherwise noted)

	DAC-HK12B	DAC-HK12D
MAXIMUM RATINGS		
Positive Supply, pin 22	+18 V	*
Negative Supply, pin 14	−18 V	*
Logic Supply, pin 13	+5.25 V	*
Digital Input Voltage, pins 1-12 & 16	+5.5 V	*
Output Current, pin 15	±20 mA	*
INPUTS		
Resolution	12 bits	3 digits
Coding, unipolar output	Straight Binary	BCD
Coding, bipolar output	Offset Binary	-
	Two's Complement [1]	-
Input Logic Level, bit ON ("1")	+2.0 V to +5.5 V	
Input Logic Level, bit OFF ("0")	0 V to +0.8 V	
Logic Loading	1 LSTTL load	
Load Input[2]	HI ("1") = hold data	
	LO ("0") = transfer data	
Load Input Loading	3 LSTTL loads	
OUTPUT		
Output Voltage Ranges[3], unipolar	0 to +5 V	0 to +2.5 V
	0 to +10 V	0 to +5 V
	-	0 to +10 V
Output Voltage Ranges[3], bipolar	±2.5 V	-
	±5 V	-
	±10 V	-
Output Current	±5 mA min.	*
Output Impedance	0.05 ohm	*
PERFORMANCE		
Linearity Error, max.	±½ LSB	±¼ LSB
Differential Linearity Error, max.	±½ LSB	±¼ LSB
Gain Error, before trimming	±0.1%	*
Zero Error, before trimming	±0.1%	*
Gain Tempco, max.	±20 ppm/°C	*
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR	*
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR	*
Diff. Linearity Error Tempco	±2 ppm/°C of FSR	*
Monotonicity	Guaranteed over oper. temp. range	
Settling Time, 5 V change	3 μsec.	3 μsec.
Settling Time, 10 V change	3 μsec.	4 μsec.
Settling Time, 20 V change	4 μsec.	-
Settling Time, 1 LSB change	800 nsec.	*
Slew Rate	20 V/μsec.	*
Power Supply Rejection	±0.002% FSR/%	*
POWER REQUIREMENT	+15 VDC ±0.5 V at 15 mA	
	−15 VDC ±0.5 V at 30 mA	
	+5 VDC ±0.25V at 65mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C (BGC, BMC)	
	−25°C to +85°C (BMR)	
	−55°C to +125°C (BMM)	
Storage Temperature Range	−55°C to +125°C	
Package Type	24-pin Ceramic DIP	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.2 oz. (6g.)	

*Same specification as first column.

NOTES:

1. For two's complement coding order the model described under ordering information.
2. Logic levels are the same as for data inputs.
3. By external pin connection.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1 μF (tantalum type) at the +15, −15, and +5 V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments these capacitors should be shunted with .01 μF ceramic capacitors.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level triggered input which causes the register to hold data with a HI input and transfer data to the DAC with a LO input.
4. A setup time of 50 nsec. minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. The external gain adjustment shown in the Connection Diagrams has a range of ±0.2% of full scale. If a wider range is desired the 18-Megohm resistor can be decreased slightly in value. The full scale output is typically accurate within ±0.1% with no adjustment. The zero, or offset, adjustment has a range of ±0.35% of FS.
6. If the reference output terminal (pin 24) is used an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10μA in order not to affect the T.C. of the reference.

ORDERING INFORMATION

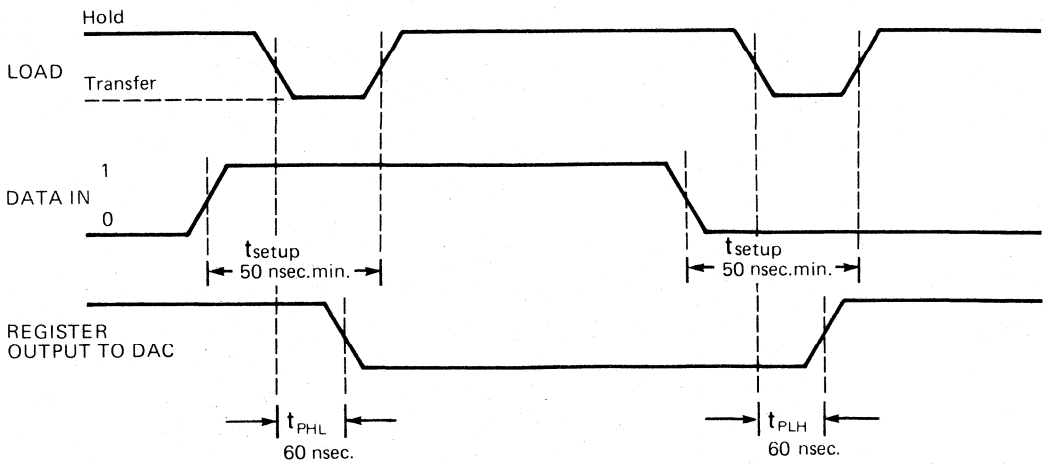
MODEL	TEMP. RANGE	SEAL	PRICE (1-24)
Binary Coding			
DAC-HK12BGC	0 to 70°C	Epoxy	
DAC-HK12BMC	0 to 70°C	Herm.	
DAC-HK12BMR	-25 to +85°C	Herm.	
DAC-HK12BMM	-55 to +125°C	Herm.	
BCD Coding			
DAC-HK12DGC	0 to 70°C	Epoxy	
DAC-HK12DMC	0 to 70°C	Herm.	
DAC-HK12DMR	-25 to +125°C	Herm.	
DAC-HK12DMM	-55 to +125°C	Herm.	
2's Complement Coding			
DAC-HK12BGC-2	0 to 70°C	Epoxy	
DAC-HK12BMC-2	0 to 70°C	Herm.	
DAC-HK12BMR-2	-25 to +85°C	Herm.	
DAC-HK12BMM-2	-55 to +125°C	Herm.	

Mating Socket: DILS-3(24-pin socket)
Trimming Potentiometers: TP100K (100K ohms)

For high reliability versions of the DAC-HK series, including units screened to MIL-STD-883 level B, contact factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

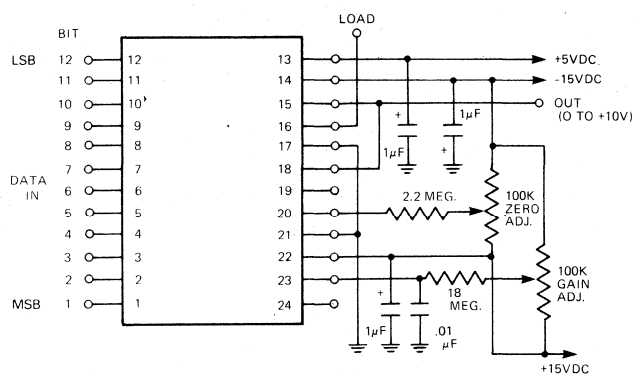
TIMING DIAGRAM



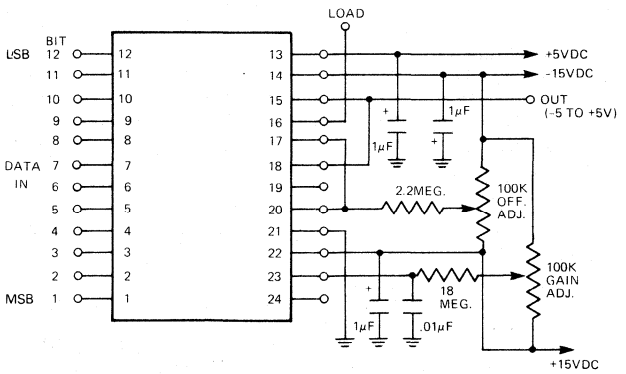
All rise and fall times ⩽10 nsec.

CONNECTION DIAGRAMS

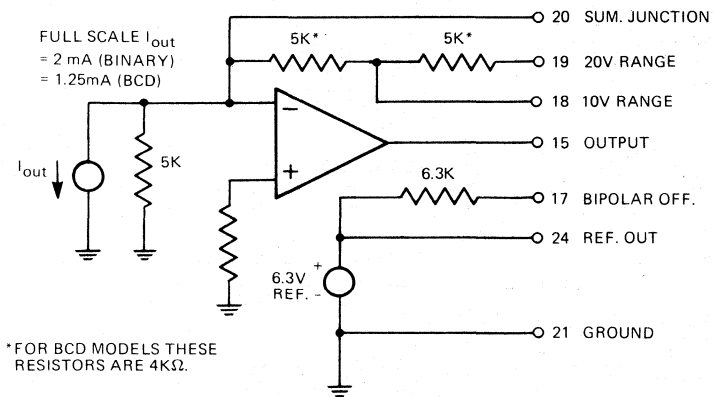
UNIPOLAR OPERATION
(0 to +10V)



BIPOLAR OPERATION
(±5 V)



OUTPUT CIRCUIT



OUTPUT RANGE SELECTION

BINARY, 2's COMP.	CONNECT THESE PINS TOGETHER		
±10 V	15 & 19	17 & 20	
±5 V	15 & 18	17 & 20	
±2.5 V	15 & 18	17 & 20	19 & 20
+10 V	15 & 18	17 & 21	
+5 V	15 & 18	17 & 21	19 & 20
BCD	**CONNECT THESE PINS TOGETHER**		
+10 V	15 & 19		17 & 21
+ 5 V	15 & 18		17 & 21
+2.5 V	15 & 18	19 & 20	17 & 21

CODING TABLES

UNIPOLAR OPERATION

STRAIGHT BINARY	OUTPUT RANGES	
MSB LSB	0 to +10 V	0 to +5 V
1111 1111 1111	+9.9976	+4.9988
1100 0000 0000	+7.5000	+3.7500
1000 0000 0000	+5.0000	+2.5000
0100 0000 0000	+2.5000	+1.2500
0000 0000 0001	+0.0024	+0.0012
0000 0000 0000	0.0000	0.0000

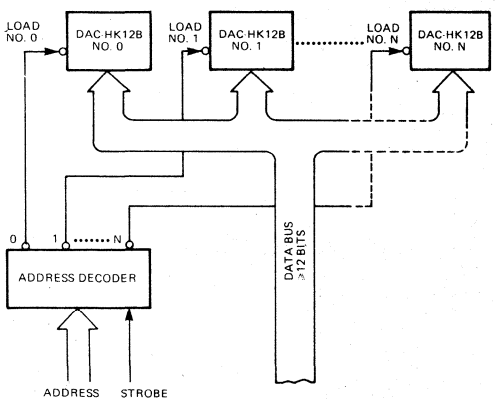
BCD	OUTPUT RANGES		
MSB LSB	0 to +10 V	0 to +5 V	0 to +2.5 V
1001 1001 1001	+9.990	+4.995	+2.498
1000 0101 0000	+7.500	+3.750	+1.875
0101 0000 0000	+5.000	+2.500	+1.250
0010 0101 0000	+2.500	+1.250	+0.625
0000 0000 0001	+0.010	+0.005	+0.003
0000 0000 0000	0.000	0.000	0.000

BIPOLAR OPERATION

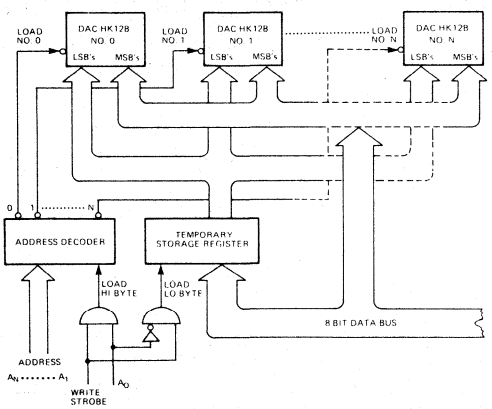
OFFSET BINARY	TWO's COMPLEMENT	OUTPUT RANGES		
MSB LSB	MSB LSB	±10 V	±5 V	±2.5 V
1111 1111 1111	0111 1111 1111	+9.9951	+4.9976	+2.4988
1100 0000 0000	0100 0000 0000	+5.0000	+2.5000	+1.2500
1000 0000 0000	0000 0000 0000	0.0000	0.0000	0.0000
0100 0000 0000	1100 0000 0000	−5.000	−2.5000	−1.2500
0000 0000 0001	1000 0000 0001	−9.9951	−4.9976	−2.4988
0000 0000 0000	1000 0000 0000	−10.0000	−5.0000	−2.5000

APPLICATIONS

INTERFACING TO ≥ 12 BIT DATA BUS



INTERFACING TO 8 BIT DATA BUS



CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter up as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000 V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) or 1001 1001 1001 (BCD) and adjust the GAIN ADJ. potentiometer to give the full scale output voltage shown in the Coding Table.

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full scale output voltage shown in the Coding Table.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or a 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full scale output voltage shown in the Coding Table.

16-Bit, Microelectronic Digital-to-Analog Converters DAC-HP16B And DAC-HP16D

FEATURES

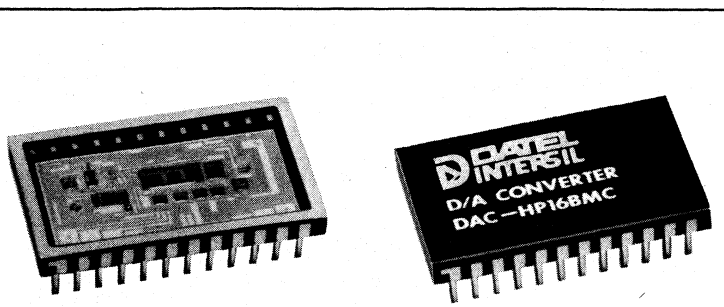
- **16 Bit Binary Model**
- **4 Digit BCD Model**
- **Voltage Output**
- **15ppm/°C max. Gain Tempco**
- **Linearity to ±0.003%**

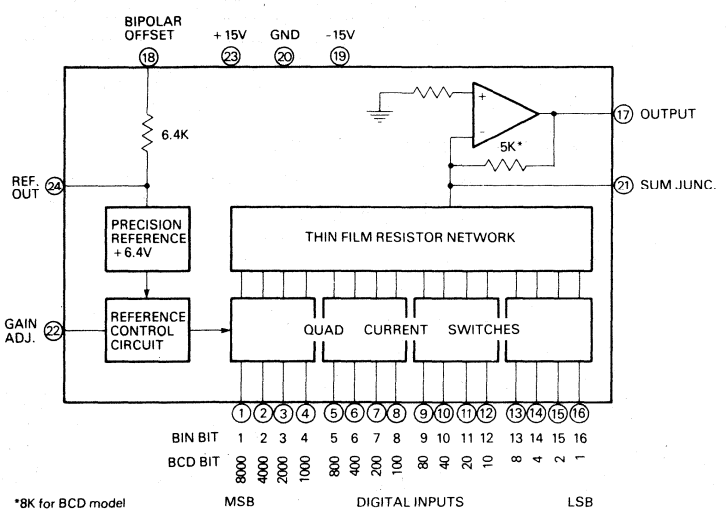
GENERAL DESCRIPTION

The DAC-HP series are high resolution hybrid D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24 pin double spaced ceramic DIP package. There are two basic models in the series. The DAC-HP16B has 16 bit binary resolution with ±0.003% linearity while the DAC-HP16D has 4 digit BCD resolution with ±0.005% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B and complementary BCD for the DAC-HP16D. The binary version operates in both unipolar and bipolar modes with output voltages of 0 to +10V and ±5V respectively. Binary versions with a bipolar output voltage range of ±10V are available, denoted by the suffix "−1" after the model designation. The BCD version operates in the unipolar mode only with 0 to +10V output.

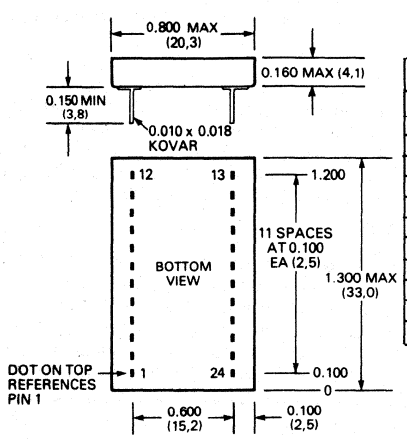
The DAC-HP design incorporates thin film hybrid technology which has been in volume production. Selected low tempco nichrome-on-silicon thin film resistor networks are combined with tightly matched quad current switches to achieve 16 bit resolution. The thin film resistors together with the low tempco zener reference circuit result in a maximum gain tempco of ±15ppm/°C for the DAC. The thin film resistors are functionally laser trimmed for optimum converter linearity.

The resolution, stability, and voltage output of these converters make them ideal for precision applications such as speech and waveform reconstruction, precision ramp generators, and computer controlled testing. They are available in three operating temperature ranges: 0 to 70°C, −25 to +85°C, and −55 to +125°C. High reliability versions are also available screened to MIL-STD-883 level B, Power requirement is ±15VDC.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	BIT 13 IN
2	BIT 2 IN	14	BIT 14 IN
3	BIT 3 IN	15	BIT 15 IN
4	BIT 4 IN	16	BIT 16 IN (LSB)
5	BIT 5 IN	17	OUTPUT
6	BIT 6 IN	18	BIPOLAR OFF.
7	BIT 7 IN	19	−15VDC
8	BIT 8 IN	20	GROUND
9	BIT 9 IN	21	SUM. JUNCTION
10	BIT 10 IN	22	GAIN ADJ.
11	BIT 11 IN	23	+15VDC
12	BIT 12 IN	24	REF. OUT

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SPECIFICATIONS, DAC-HP SERIES
(Typical at 25°C, and ±15 V supplies unless otherwise noted)

	DAC-HP16B (Binary)	DAC-HP16D (BCD)
MAXIMUM RATINGS		
Positive Supply, pin 23	+18V	*
Negative Supply, pin 19	−18V	*
Digital Input Voltage, pins 1-16	+5.5V	*
Output Current, pin 17	±20mA	*
INPUTS		
Resolution	16 bits	4 digits
Coding, unipolar output	Comp. Binary	Comp. BCD
Coding, bipolar output	Comp. Off. Binary	—
Input Logic Level, bit ON ("0")[1]	0V to +0.8V @ −1mA	
Input Logic Level, bit OFF ("1")[1]	+2.4V to +5.5V @ +40μA	
Logic Loading	1 TTL load	*
OUTPUT		
Output Voltage Range, Unipolar[2]	0 to +10V	*
Output Voltage Range, Bipolar	±5V	-
Output Voltage Range, "−1" Suffix	±10V	-
Output Current, min.[6]	±5 mA	0 to −5mA
Output Impedance	0.05 ohm	*
PERFORMANCE		
Linearity Error, max.	±0.003%	±0.005%
Monotonicity, 10° C to 40° C	14 bits	16 bits
Gain Error, before trimming	±0.1%	*
Zero Error, before trimming	±0.1%	*
Gain Tempco, max.[3]	±15ppm/°C	*
Gain Tempco, max. BGC, DGC	±20ppm/° C	*
Zero Tempco, unipolar, max.	±5ppm/° C of FSR[4]	*
Offset Tempco, bipolar, max.	±8ppm/° C of FSR[4]	—
Differential Linearity Tempco	±2ppm/° C of FSR[4]	*
Settling Time, 10V change[5]	15μsec.	15μsec.
Slew Rate	20V/μsec.	*
Power Supply Rejection	±0.002% FSR/%	*
POWER REQUIREMENT (Quiescent, all bits HI)	+15VDC at 38mA −15VDC at 38mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0° C to 70° C (BMC, DMC, BGC, DGC) -25° C to +85° C (BMR, DMR) -55° C to +125° C (BMM, DMM)	
Storage Temperature Range	-65° C to +150° C	
Package Type	24 pin ceramic	
Pins	0.010 x 0.018 inch diameter Kovar	
Weight	0.2 oz. (6g.)	

*Specifications same as first column.

NOTES:
1. Drive from TTL output with only the DAC-HP as load.
2. Unipolar output range for suffix "—1" models, 0 to +10V, is reached at ½ scale input.
3. For all models except DAC-HP16BGC & DAC-16DGC.
4. FSR is 0 to +FS or -FS to +FS voltage.
5. To 0.005% FSR. 6 Pin 17

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1μF (tantalum type) at the +15V and −15V supply pins. The capacitors should be connected as close to the pins as possible. In high frequency noise environments an additional .01μF ceramic capacitor should be used in parallel with each tantalum bypass.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 20 where they all must connect together.
3. The external gain adjustment shown in the diagrams gives an adjustment of ±0.2% of full scale range. The converters are internally trimmed to ±0.1% at full scale. A wider range of adjustment may be achieved by decreasing the value of the 510K ohm resistor.
4. The zero adjustment, or offset adjustment, has an adjustment range of ±0.35% of full scale range. The unipolar zero is internally set to zero within ±0.1% of full scale range.
5. If the reference output (pin 24) is used, it must be buffered by an operational amplifier in the noninverting mode. Current drawn from pin 24 should be limited to ±10μA in order that the temperature coefficient of the reference circuit not be affected. This is sufficient current for the bias current of most of the popular operational amplifier types.

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	SEAL	PRICE (1-24)
DAC-HP16BGC	0 to 70C	EPOXY	
DAC-HP16BMC	0 to 70C	HERM.	
DAC-HP-16BMR	-25 to +85C	HERM.	
DAC-HP16BMM	-55 to +125C	HERM.	
DAC-HP16BMC-1	0 to 70C	HERM.	
DAC-HP16BMR-1	-25 to +85C	HERM.	
DAC-HP16BMM-1	-55 to +125C	HERM.	
DAC-HP16DGC	0 to 70C	EPOXY	
DAC-HP16DMC	0 to 70C	HERM.	
DAC-HP16DMR	-25 to +85C	HERM.	
DAC-HP16DMM	-55 to +125C	HERM.	

Mating Socket: DILS-3 (24 pin socket)

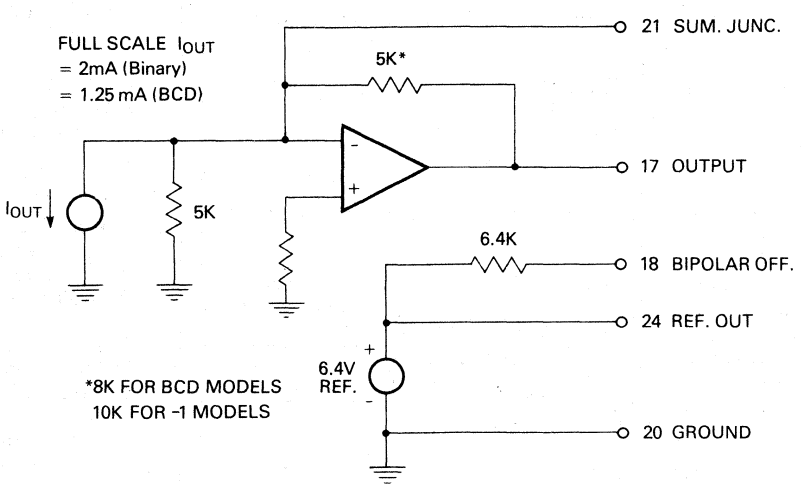
Trimming Potentiometer: TP50K

For high reliability versions of the DAC-HP series, including units screened to MIL-STD-883, Level B, contact factory.

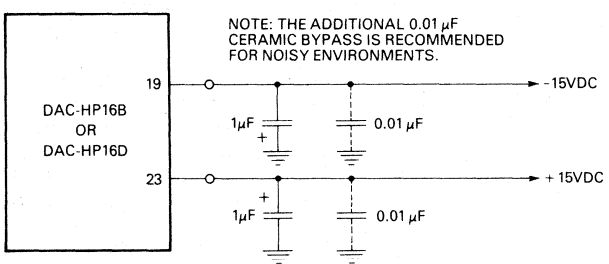
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

APPLICATION

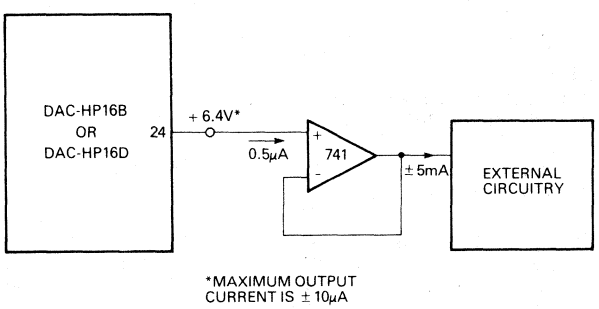
OUTPUT CIRCUIT



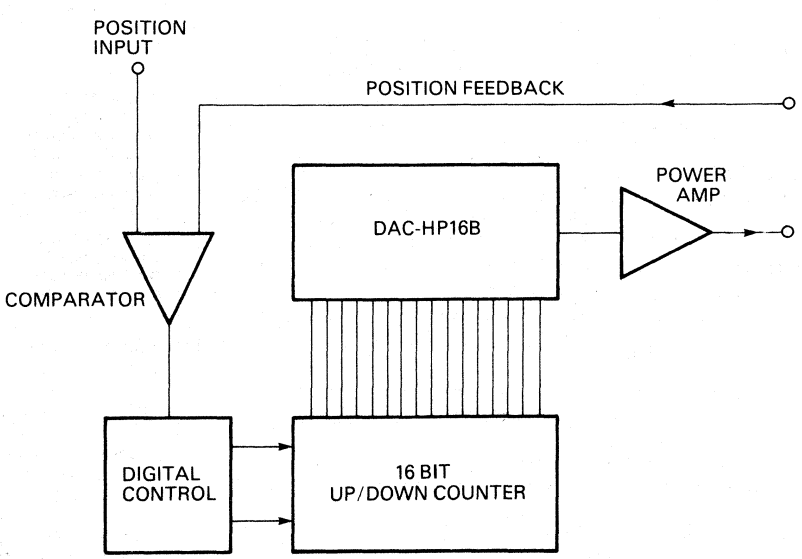
POWER SUPPLY BYPASSING



USE OF REFERENCE OUTPUT



PRECISION INDUSTRIAL POSITION CONTROLLER



CONNECTION AND CALIBRATION

CODING TABLES

BIPOLAR OUTPUT— Complementary Offset Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE	OUTPUT VOLTAGE SUFFIX "−1" MODELS
0000 0000 0000 0000	+FS−1LSB	+4.99985V	+9.99969V
0011 1111 1111 1111	+½FS	+2.50000	+5.00000
0111 1111 1111 1111	0	0.00000	0.00000
1011 1111 1111 1111	−½FS	−2.50000	−5.00000
1111 1111 1111 1110	−FS+1LSB	−4.99985	−9.99969
1111 1111 1111 1111	−FS	−5.00000V	−10.00000V

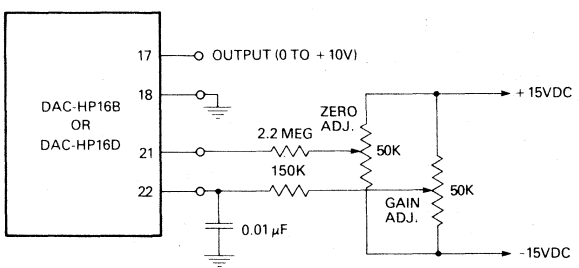
UNIPOLAR OUTPUT—Complementary BCD

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0110 0110 0110 0110	+FS−1LSB	+9.999V
1000 1010 1111 1111	+¾FS	+7.500
1010 1111 1111 1111	+½FS	+5.000
1101 1010 1111 1111	+¼FS	+2.500
1111 1111 1111 1110	+1LSB	+1.00mV
1111 1111 1111 1111	0	0

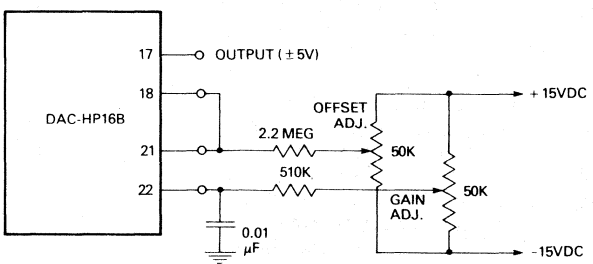
UNIPOLAR OUTPUT—Complementary Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0000 0000 0000 0000	+FS−1LSB	+9.99985V
0011 1111 1111 1111	+¾FS	+7.50000
0111 1111 1111 1111	+½FS	+5.00000
1011 1111 1111 1111	+¼FS	+2.50000
1111 1111 1111 1110	+1LSB	+153μV
1111 1111 1111 1111	0	0

UNIPOLAR OPERATION



BIPOLAR OPERATION



CALIBRATION PROCEDURE

Connect the converter as shown in the application diagrams. For bipolar operation connect Bipolar Offset (pin 18) to Summing Junction (pin 21). For unipolar operation connect Bipolar Offset (pin 18) to Ground (pin 20). In making the following adjustments, refer to the coding tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 1111 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.00000V output.
2. **Gain Adjustment.** Set the input digital code to 0000 0000 0000 0000 (complementary binary) or 0110 0110 0110 0110 (complementary BCD) and adjust the GAIN ADJ. potentiometer to give +9.99985V output (complementary binary) or +9.999V output (complementary BCD).

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the Digital Input Code to 1111 1111 1111 1111 and adjust the OFFSET ADJ. potentiometer to give the −F.S. output shown in the coding table above for the model being calibrated.
2. **Gain Adjustment.** Set the Digital Input Code to 0000 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give the +FS-1 LSB output shown in the coding table above for the model being calibrated.

12 Bit Hybrid Digital-to-Analog Converters DAC-HZ Series

FEATURES

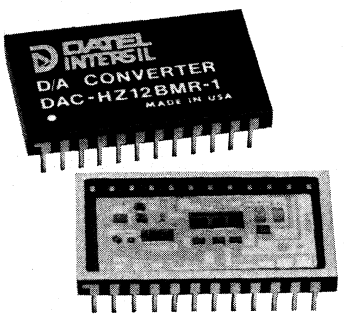
- 12 Bit Binary or 3 Digit BCD
- 5 Output Ranges
- 3 μSec. Settling Time
- Internal Ref. & Output Amp.
- High Performance

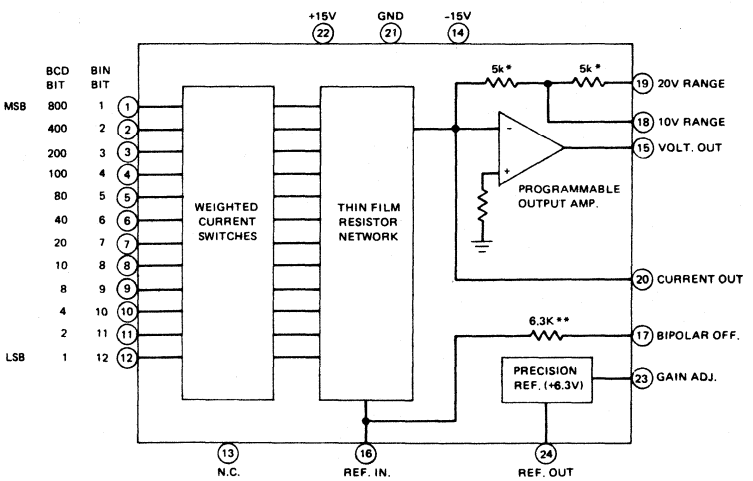
GENERAL DESCRIPTION

The DAC-HZ series are high performance, hybrid 12 bit binary and 3 digit BCD digital-to-analog converters. These converters are manufactured in volume in Dåtel Intersil's modern in-house thin film hybrid facility. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V with only unipolar ranges available on the BCD models. Current output is also provided.

The internal design utilizes three quad current switches, two thin film resistor networks, a precision zener reference circuit, reference control circuit and output amplifier. The thin film resistor networks are functionally trimmed with a laser to precisely set the binary weights of the current switches. The excellent tracking of the thin film resistors in conjunction with the tightly matched current switches results in a differential nonlinearity tempco of only 2ppm/°C. Temperature coefficient of gain is ±20ppm/°C max. and tempco of zero is ±5ppm/°C of FS max.

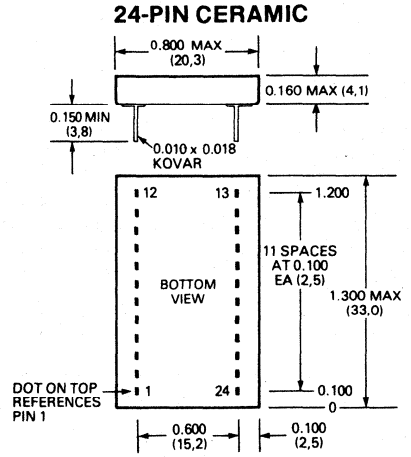
The DAC-Hz series consists of 8 different models covering the operating temperature ranges of 0°C to 70°C, −25°C to +85°C, and −55°C to +125°C. The models come in a 24-pin ceramic package. Power requirement is ±15 VDC at 35mA with no 5V logic supply required. Input coding is complementary binary or complementary BCD. Voltage output settling time is 3 μsec. to ½ LSB.





* For BCD model these resistors are 4KΩ.
** For BCD model this resistor is open circuit.

MECHANICAL DIMENSIONS INCHES (MM) 24-PIN CERAMIC



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN	13	NO CONN.
2	BIT 2 IN	14	-15VDC
3	BIT 3 IN	15	VOLT. OUT
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	BIPOLAR OFF.
6	BIT 6 IN	18	10V RANGE
7	BIT 7 IN	19	20V RANGE
8	BIT 8 IN	20	CURRENT OUT
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15VDC
11	BIT 11 IN	23	GAIN ADJ.
12	BIT 12 IN	24	REF. OUT

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SPECIFICATIONS, DAC-HZ SERIES
(Typical at 25°C and ±15V supplies unless otherwise noted)

	DAC-HZ12B (Binary)	DAC-HZ12D (BCD)
INPUTS		
Resolution	12 Binary bits	3 BCD digits
Coding, unipolar output	Complementary Binary	Complementary BCD
Coding, bipolar output	Comp. Offset Bin.	—
Input Logic Level, bit ON ("0")	0V to +0.8V @ -1mA	
Input Logic Level, bit OFF ("1")	+2.4V to +5.5V @ +40μA	
Logic Loading	1 TTL load	
OUTPUTS		
Output Current, unipolar	0 to −2mA, ±10%	0 to −1.25mA, ±10%
Output Current, bipolar	±1mA, ±10%	—
Voltage Compliance, Iout	±2.5V	*
Output Impedance, Iout, unipolar	5K ohms	*
Output Impedance, Iout, bipolar	2.8K ohms	—
Output Voltage Ranges, unipolar	0V to +5V	0 to +2.5V
	0V to +10V	0 to +5V
		0 to +10V
Output Voltage Ranges, bipolar	±2.5V	—
	±5V	—
	±10V	—
Output Current, Vout	±5mA min.	*
Output Impedance, Vout	.05 ohm	*
PERFORMANCE, Voltage Output		
Nonlinearity	±1/2 LSB max.	±1/4 LSB max.
Differential Nonlinearity	±1/2 LSB max.	±1/4 LSB max.
Gain Error, before trimming	±0.1% of FSR[1]	*
Zero Error, before trimming	±0.1% of FSR[1]	*
Gain Tempco, max.	±20ppm/°C	*
Zero Tempco, unipolar, max.	±5ppm/°C of FSR[1]	*
Offset Tempco, biopolar, max.	±10ppm/°C of FSR[1]	*
Diff. Nonlinearity Tempco	±2ppm/°C of FSR[1]	*
Monotonicity	Over oper. temp. range	*
Settling Time, Iout to 1/2 LSB[2]	300nsec.	*
Settling Time, Vout to 1/2 LSB	3 μsec.[3]	*
Slew Rate	20V/μsec.	*
Power Supply Rejection	±.002% FSR/% Supply[1]	*
POWER REQUIREMENT		
Power Supply Voltage	±15VDC ±0.5V	
Quiescent Current	35mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Ranges	0°C to 70°C, −25°C to +85°C, and −55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Package Size	1.300 x 0.800 x 0.160 inches	
Package Type	24 Pin Ceramic DIP	
Pins	Kovar 0.010 x 0.018 inches	
Weight	0.22 oz. (63 g.)	

*Specifications same as first column

1. FSR is full scale range and is 10V for 0 to +10V or −5V to +5V output; 20V for ±10V output, etc.
2. Current output mode.
3. For 2.5K or 5K feedback (2K or 4K, BCD). For 10K feedback (8K, BCD) the settling time is 4 μsec.

TECHNICAL NOTES

1. The DAC-HZ12 series converters are designed and factory calibrated to give ±½LSB linearity (binary version) and ±¼LSB linearity (BCD version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be ±1/2 LSB (±1/4 LSB, BCD) everywhere over the full output range without any additional adjustments to achieve a best straight line fit. The linearity specification is therefore a conservative one since the user does not have to make more complicated adjustments for a best straight line fit.
2. The external zero or offset adjustment for the converters has a range of ±0.2% of full scale and the external gain adjustment has a range of ±0.3% of full scale.
3. These converters must be operated with local supply by-pass capacitors from +15V to ground and −15V to ground. Tantalum type capacitors of 1μF are recommended and should be mounted as close as possible to the converter. If the converters are used in a high frequency noise environment a .01μF ceramic capacitor should be used across each tantalum capacitor.
4. When operating in the current output mode the equivalent internal current source of 2mA (1.25mA, BCD) must drive both the internal source resistances and the external load resistor. A 300 nsec. output settling time is achieved for the voltage across a 100 ohm load resistor; for higher value resistors the settling time becomes longer due to the output capacitance of the converter. For fastest possible voltage output for a large transition, an external fast settling amplifier such as Datel-Intersil's AM-500 should be used in the inverting mode. Settling time of less than 1 μsec. can be achieved. See application diagram.

ORDERING INFORMATION

Model	Operating Temp. Range	Seal
DAC-HZ12BGC	0° C to +70° C	Epoxy
DAC-HZ12BMC	0° C to +70° C	Hermetic
DAC-HZ12BMR	-25° C to +85° C	Hermetic
DAC-HZ12BMM	-55° C to +125° C	Hermetic
DAC-HZ12DGC	0° C to +70° C	Epoxy
DAC-HZ12DMC	0° C to +70° C	Hermetic
DAC-HZ12DMR	-25° C to +85° C	Hermetic
DAC-HZ12DMM	-55° C to +125° C	Hermetic

Mating Socket: DILS-3 (24 pin socket)

Trimming Potentiometers: TP10K OR TP100K

For high reliability versions of the DAC-HZ series, including units screened to MIL-STD-883 level B, contact factory.

The DAC-HZ12 SERIES CONVERTERS ARE COVERED BY GSA CONTRACT.

INTERCONNECTIONS AND CALIBRATION

CALIBRATION PROCEDURE

1. Select the desired output range and connect the converter up as shown in the Output Range Selection table and the Standard Connection diagrams below.
2. To calibrate refer to the Coding Tables below. Note that complementary coding is used.
3. **Zero and Offset Adjustments**
   For unipolar operation set all digital inputs to "1" (+2.0 to +5.5V) and adjust the ZERO ADJ. potentiometer for zero output voltage or current. For bipolar operation (binary model only) set all digital inputs to "1" and adjust the OFFSET ADJ. potentiometer for the negative full scale (for voltage out) or positive full scale (for current out) output value shown in the Coding Table.
4. **Gain Adjustment**
   For the binary model set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.
   For the BCD model (unipolar only) set each BCD digit to 0110 and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.

OUTPUT RANGE SELECTION

BIN. RANGE	CONNECT THESE PINS TOGETHER			
±10V	15 & 19	17 & 20		16 & 24
±5V	15 & 18	17 & 20		16 & 24
±2.5V	15 & 18	17 & 20	19 & 20	16 & 24
+10V	15 & 18	17 & 21		16 & 24
+5V	15 & 18	17 & 21	19 & 20	16 & 24
±1mA		17 & 20		16 & 24
−2mA		17 & 21		16 & 24
BCD RANGE	**CONNECT THESE PINS TOGETHER**			
+10V	15 & 19	17 & 21		16 & 24
+5V	15 & 18	17 & 21		16 & 24
+2.5V	15 & 18	17 & 21	19 & 20	16 & 24
−1.25MA		17 & 21		16 & 24

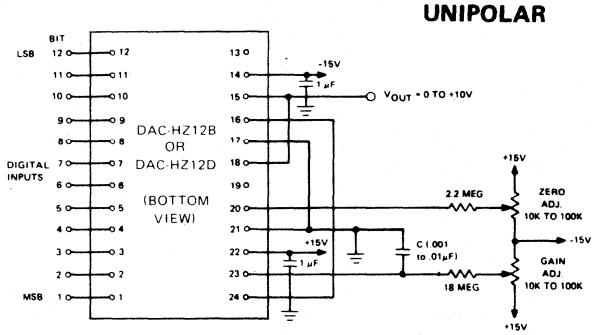
VOLTAGE OUTPUT IS AT PIN 15.
CURRENT OUTPUT IS AT PIN 20.

STANDARD CONNECTIONS

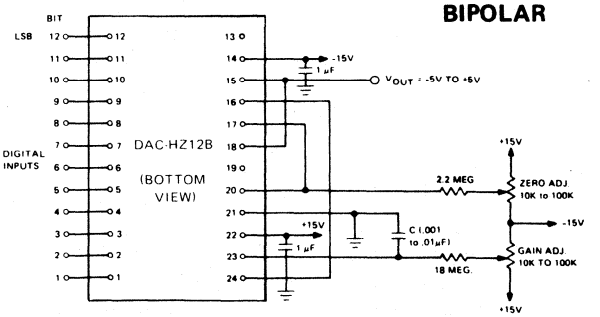
VOLTAGE OUTPUT CONNECTIONS

(FOR DIFFERENT OUTPUT SCALING REFER TO OUTPUT RANGE SELECTION TABLE)

UNIPOLAR

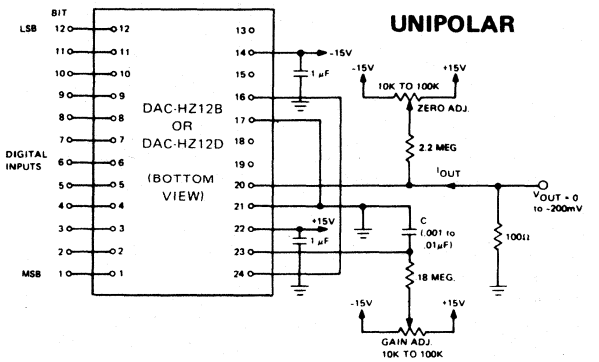


BIPOLAR

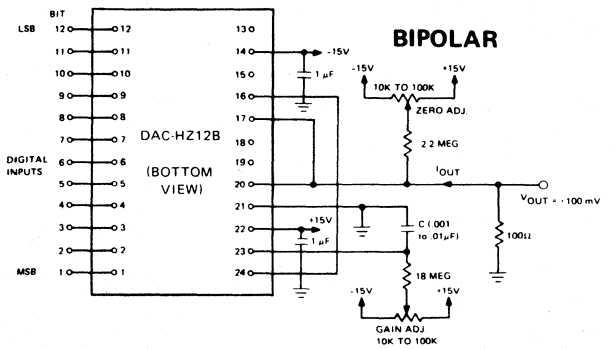


CURRENT OUTPUT CONNECTIONS

UNIPOLAR



BIPOLAR



CODING TABLES

UNIPOLAR OUTPUT – COMPLEMENTARY BINARY

BINARY INPUT CODE		UNIPOLAR OUTPUT RANGES		
MSB	LSB	0 TO +10V	0 TO +5V	0 TO -2MA
0000	0000 0000	+9.9976V	+4.9988V	-1.9995MA
0011	1111 1111	+7.5000	+3.7500	-1.5000
0111	1111 1111	+5.0000	+2.5000	-1.0000
1011	1111 1111	+2.5000	+1.2500	-0.5000
1111	1111 1110	+0.0024	+0.0012	-0.0005
1111	1111 1111	0.0000	0.0000	0.0000

UNIPOLAR OUTPUT – COMPLEMENTARY BCD

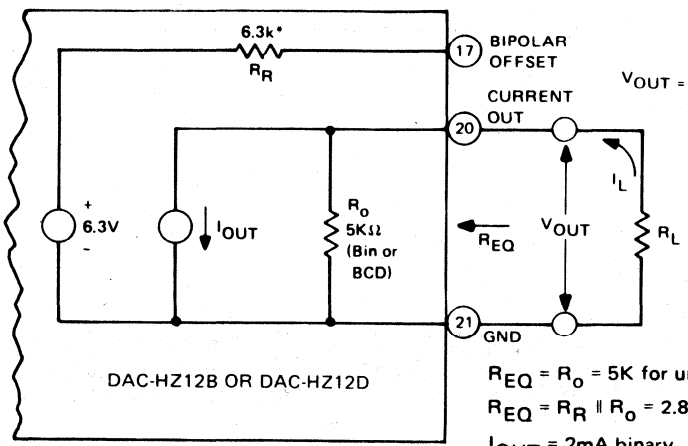
BCD INPUT CODE		UNIPOLAR OUTPUT RANGES			
MSD	LSD	0 TO +10V	0 TO +5V	0 TO +2.5V	0 TO -1.25MA
0110	0110 0110	+9.990V	+4.995V	+2.498V	−1.2488MA
1000	1010 1111	+7.500	+3.750	+1.875	−0.9375
1010	1111 1111	+5.000	+2.500	+1.250	−0.6250
1101	1010 1111	+2.5000	+1.250	+0.625	−0.3125
1111	1111 1110	+0.0100	+0.005	+0.003	−0.0013
1111	1111 1111	0.0000	0.000	0.000	0.0000

BIPOLAR OUTPUT – COMPLEMENTARY OFFSET BINARY

INPUT CODE		BIPOLAR OUTPUT RANGES			
MSB	LSB	±10V	±5V	±2.5V	±1MA
0000	0000 0000	+9.9951V	+4.9976V	+2.4988V	-0.9995MA
0011	1111 1111	+5.0000	+2.5000	+1.2500	-0.5000
0111	1111 1111	0.0000	0.0000	0.0000	0.0000
1011	1111 1111	-5.0000	-2.5000	-1.2500	+0.5000
1111	1111 1110	-9.9951	-4.9976	-2.4988	+0.9995
1111	1111 1111	-10.0000	-5.0000	-2.5000	+1.0000

EQUIVALENT CIRCUITS & APPLICATIONS

EQUIVALENT CURRENT MODE OUTPUT CIRCUIT



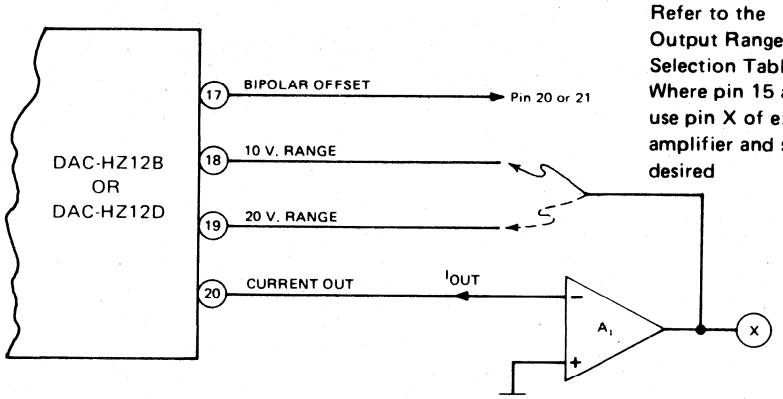
*Open circuit in DAC-HZ12D

$R_{EQ} = R_O = 5K$ for unipolar operation

$R_{EQ} = R_R \parallel R_O = 2.8K$ for bipolar operation

I_{OUT} = 2mA binary
= 1.25mA BCD.

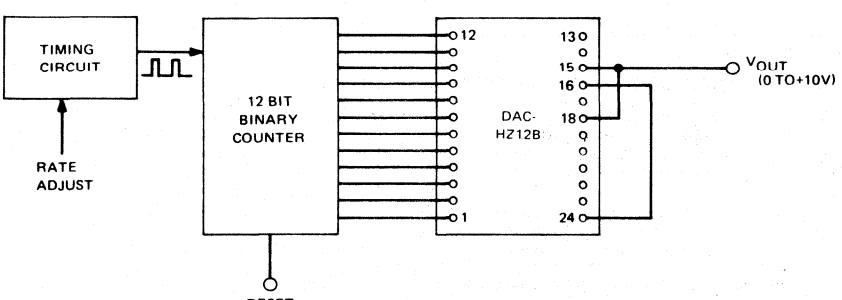
USE OF HIGH SPEED EXTERNAL OP AMP FOR FASTER SETTLING

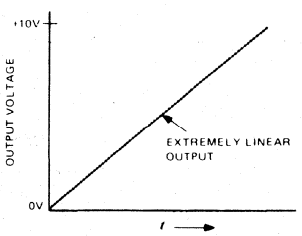


Refer to the Output Range Selection Table. Where pin 15 appears use pin X of external amplifier and scale as desired

A_1 = EXTERNAL HIGH SPEED INVERTING OP AMP., USE DATEL-INTERSIL AM-500 FOR LESS THAN 1.0μSEC. OUTPUT SETTLING.

PRECISION, LOW COST BASE LINE RAMP GENERATOR





THIS CIRCUIT DEVELOPS A HIGHLY LINEAR (.01%) OUTPUT VOLTAGE RAMP FROM 0 TO +10V. THE RAMP CAN BE MADE AS SLOW AS DESIRED WITHOUT AFFECTING LINEARITY BY SETTING THE PULSE RATE OF THE TIMING CIRCUIT TO THE PROPER VALUE. THE OUTPUT RAMP IS GENERATED IN DISCRETE STEPS OF .024% FS (4096 STEPS FOR FS CHANGE).

Low Cost, 8 Bit Monolithic Digital-to-Analog Converters Model DAC-IC8B

FEATURES

- **Low Cost**
- **8 Bit Resolution**
- **Fast Settling—300 nsec.**
- **1 or 2 Quadrant Multiplication**
- **±½LSB Linearity**
- **DTL/TTL Compatible Inputs**

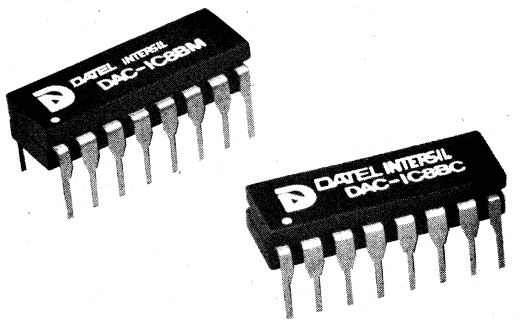
GENERAL DESCRIPTION

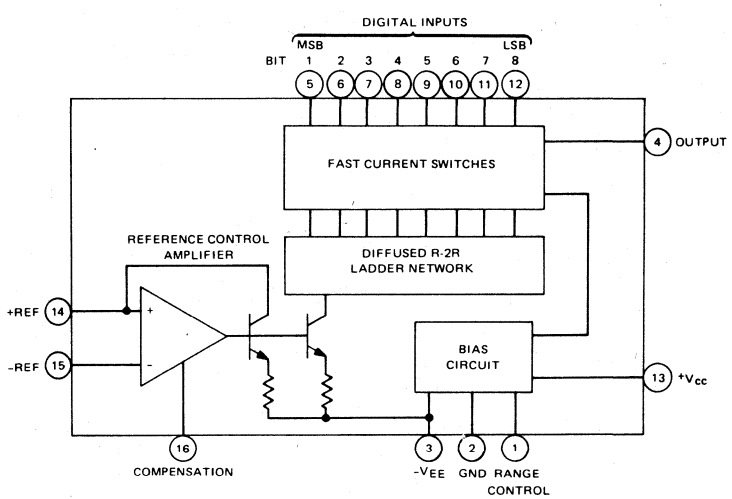
The DAC-IC8BC and DAC-IC8BM are 8 bit monolithic DAC's with fast setting current outputs. The units are housed in a 16 pin ceramic DIP and require only an external reference and output amplifier for fast voltage output operation. A full scale output change settles in only 300 nanoseconds for current output operation and 600 nanoseconds for voltage output operation using a fast monolithic output amplifier (Datel-Intersil's AM-452). Digital input coding is straight binary for unipolar operation and offset binary for bipolar operation and is compatible with standard DTL/TTL logic.

The DAC-IC8B converters consist of 8 fast-switching current sources, a diffused R-2R resistor ladder network, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of −20ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling, and low cost. Linearity is ±½LSB.

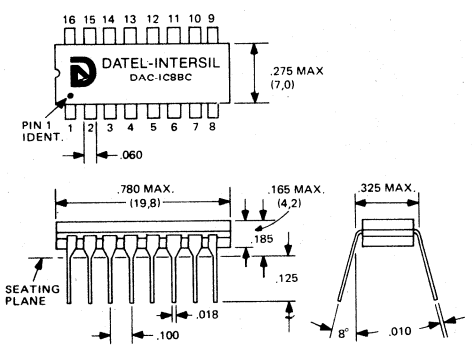
An external reference current of 2mA nominal programs the scale factor for the DAC; this is done by means of an external voltage reference source (such as Zener diode) and a resistor. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar depending on whether an external offsetting current (derived from the reference) is used. Output voltage compliance of the DAC is −0.6V to +0.5V; this can be made as large as −5V to +0.5V by external pin connection for cases where direct voltage output from a load resistor is desired.

Power supply requirement is +5VDC and −5V to −15VDC. Model DAC-IC8BC has an operating temperature range of 0°C to 70°C while DAC-IC8BM operates over −55°C to +125°C. The two models are pin compatible with industry standard devices 1408L-8 and 1508L-8 respectively.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	RANGE CONTROL
2	GROUND
3	V_{EE}
4	OUTPUT
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (LSB)
13	V_{CC}
14	+ REFERENCE
15	− REFERENCE
16	COMPENSATION

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-IC8BC & DAC-IC8BM (Typical at 25°C, V_{CC} = +5V, V_{EE} = −15V, and I_{REF} = 2mA unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltage, V_{CC}	+5.5V
V_{EE}	−16.5V
Digital Input Voltage	+5.5V
Reference Current	5.0mA
Reference Amp. Inputs	$+V_{CC}$, $-V_{EE}$
Power Dissipation	1.0 watt
INPUTS	
Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+2.0V to +5.5V @ 40μA
Input Logic Level, bit OFF ("0")	0V to +0.8V @ −0.8mA
Logic Loading	1 TTL load
Nominal Reference Current (+ Ref.)	2.0mA
Reference Current Range (+ Ref.)	0 to 4.2mA
Reference Bias Current (− Ref.)	−3μA max.
OUTPUTS	
Output Current, I_{REF} = 2.0mA	2.0mA ±0.1mA
Output Current Range, V_{EE} = −5V	0 to 2.1mA
Output Current Range, V_{EE} = −6 to −15V	0 to 4.2mA
Output Current, all bits OFF	4μA maximum
Output Voltage Compliance, pin 1 gnded	−0.6 to +0.5V
Output Voltage Comp., pin 1 open, V_{EE} < −10V	−5.0V to +0.5V
PERFORMANCE	
Relative Accuracy[1]	±½LSB (±0.19%) maximum
Nonlinearity	±½LSB (±0.19%) maximum
Differential Nonlinearity	±½LSB (±0.19%)
Temp. Coefficient of Gain	−20ppm/°C
Power Supply Rejection (V_{EE})	2.7μA/V max.
Settling Time, 2mA to ½LSB	300 nsec.
Update Rate	3.3MHz
Reference Current Slew Rate	4.0mA/μsec
POWER REQUIREMENT	
V_{CC} Voltage	+5VDC ±0.5V
V_{CC} Current	22mA maximum
V_{EE} Voltage	−4.5V to −16.5VDC
V_{EE} Current	13mA maximum
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range, DAC-IC8BC	0°C to 70°C
Operating Temp. Range, DAC-IC8BM	−55°C to +125°C
Storage Temp. Range, either model	−65°C to +150°C
Package, DAC-IC8BC	16 Pin Plastic DIP
Package, DAC-IC8BM	16 Pin Ceramic DIP

[1] With zero and full scale adjustments made.

ORDERING INFORMATION

DAC-IC8B —

OPER. TEMP. RANGE
C = 0°C TO 70°C
M = −55°C TO +125°C

PRICES **(1-24)**
DAC-IC8BC
DAC-IC8BM

Trimming Potentiometers: TP500, TP1K, and TP20K are available from Datel-Intersil at $3.50 each

The DAC-IC8BC and DAC-IC8BM converters are covered under GSA contract.

TECHNICAL NOTES

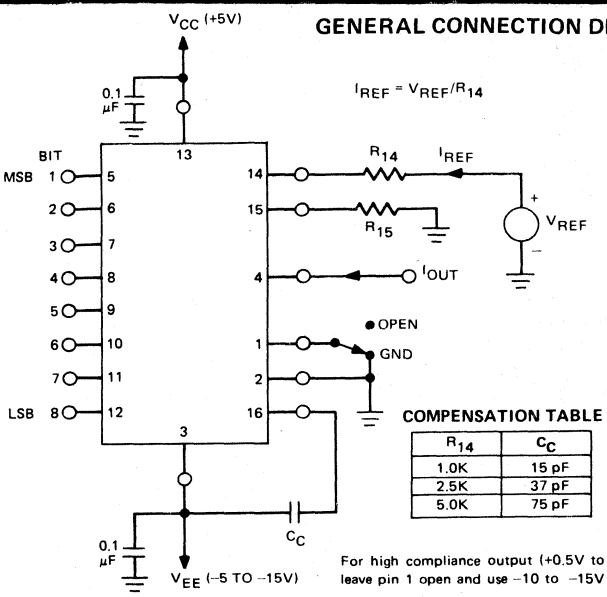
1. The *General Connection Diagram* shows the basic connections for the DAC-IC8B converter. The scale factor is set by a reference current injected into pin 14. Pins 14 and 15 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R_{15} and pin 14 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R_{14}: $I_{REF} = V_{REF}/R_{14}$. R_{14} should be a stable metal film resistor. R_{15} is used only to compensate for the input bias current into pin 15 (1 μA typical) and can be shorted out with negligible effect. R_{15}, if used, should be equal to R_{14} and may be a carbon composition type. An I_{REF} of 2.0mA is recommended for most applications.
2. There is a second method of connecting the reference shown in *Two Ways to Connect Reference.* A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 14 is at the negative voltage and I_{REF} still flows into pin 14. Again, R_{15} is used only to compensate for bias current and may be omitted. There is an important requirement for this connection: *the negative reference voltage must always be 3 volts above V_{EE}.*
3. The reference amplifier must be externally compensated, and this is done by capacitor C_C, connected from pin 16 to pin 3 (V_{EE}). C_C may also be connected from pin 16 to ground, but connection to pin 3 improves the negative supply rejection. The value of C_C depends on R_{14}, and typical values are given in the compensation table. Compensation is particularly important when the DAC-IC8B is used as a multiplying D/A converter. Proper compensation assures that output peaking does not occur when the reference voltage steps to a new value. If pin 14 is driven from a high impedance current source such as a transistor collector, then much larger values of C_C must be used and the bandwidth of the reference amplifier is significantly reduced.
4. The *Alternative Compensation Diagram* shows another way of achieving the desired compensation. Here a 1.0K resistor is always used at pin 14, but it is in series with another R to the reference voltage. The junction of the two resistors is bypassed to ground by a 0.1μF capacitor. For high frequencies pin 14 always "sees" a 1K resistance, thus allowing a 15pF capacitor for C_C. R_{15}, if used, should be the sum of 1.0K and R. This compensation scheme is useful with voltage references such as 6.2 or 6.4 volt Zener diodes.
5. It is recommended that pin 13 (V_{CC}) and pin 3 (V_{EE}) always be bypassed to ground with at least 0.1μF capacitors located close to the pins.
6. As shown in the *General Connection Diagram,* pin 1 may be either connected to ground or left open. This connection determines the voltage compliance at pin 4 (I_{OUT}). For pin 1 grounded, the output compliance is −0.6 to +0.5 volt. This is satisfactory when pin 4 is used to drive a current to voltage converter and pin 4 is held at virtual ground. It is also satisfactory for low values of R_L connected to pin 4 to directly convert the output current to a voltage. The voltage compliance may be extended to −5.0 volts by leaving pin 1 open and using a V_{EE} more negative than −10 volts. In this way a 2.5K load resistor may be used at pin 14 to give an output voltage range of 0 to −5 volts (with reference current of 2mA). As shown in the table of *Settling Time vs R_L*, the output settling time is constant (300 nsec.) for R_L values from 0 to 500 ohms; thereafter it increases to 1.2μsec for R_L = 2.5K.
7. The accuracy of the DAC-IC8B is specified for a reference current of 2.0mA; the accuracy, however, is essentially constant for reference currents from 1.5mA to 2.5mA. Typically, this device is monotonic for all values of reference current above 0.5mA. Reference currents up to 4.2mA may be used. *When using a 4mA reference current, V_{EE} must be more negative than −6 volts.*

TECHNICAL NOTES (Cont'd)

8. For fastest voltage output settling times in either unipolar or bipolar modes, two circuits using Datel Intersil's AM-452 monolithic operational amplifiers are recommended. These circuits, with the compensation shown, result in output settling times of typically 600 nsec. for a 10 volt change to 1 LSB. This is the worst case settling time which occurs when all bits are turned on. For current output and R_L less than 500 ohms, this time is 300 nsec.; when all bits are turned off the time is shorter, typically 100 nsec. The two circuits shown also illustrate a simple method of deriving both reference current and offset current from a precision 6.4 volt Zener reference diode.
9. Both one and two quadrant multiplication are also possible with the DAC-IC8B as shown in the two diagrams. V_{IN} is shown operating into pin 14; this results in an input impedance of 2.5K. Alternatively, V_{IN} can be applied to pin 15 for a high impedance input as explained previously. The range of V_{IN} is then 0 to −10V. For two quadrant multiplication V_{IN} is unipolar and the digital input is bipolar with offset binary coding. V_{OUT} then varies over the bipolar range of ±5 volts. In multiplication applications, it is recommended that full scale I_{REF} be set to 4.0mA; the output is then monotonic as the reference current varies over 0.5mA to 4.0mA.

CONNECTION DIAGRAMS

GENERAL CONNECTION DIAGRAM

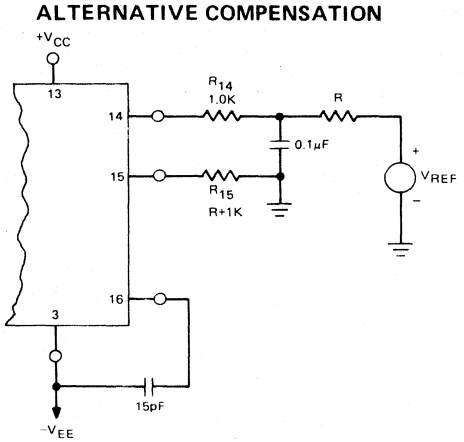


COMPENSATION TABLE

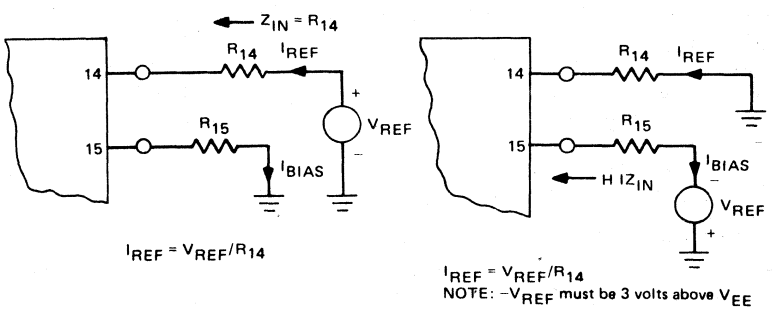
R_{14}	C_C
1.0K	15 pF
2.5K	37 pF
5.0K	75 pF

For high compliance output (+0.5V to −5.0V) leave pin 1 open and use −10 to −15V for V_{EE}.

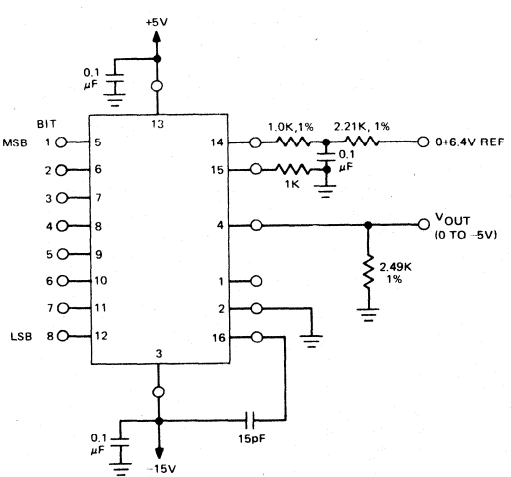
ALTERNATIVE COMPENSATION



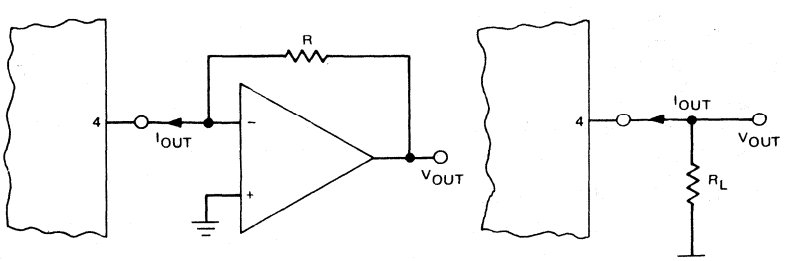
TWO WAYS TO CONNECT REFERENCE



HIGH COMPLIANCE OUTPUT



OUTPUT CONNECTIONS

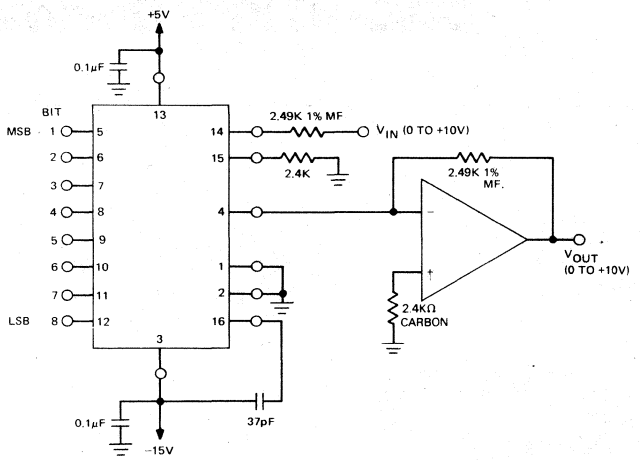


SETTLING TIME VS. R_L

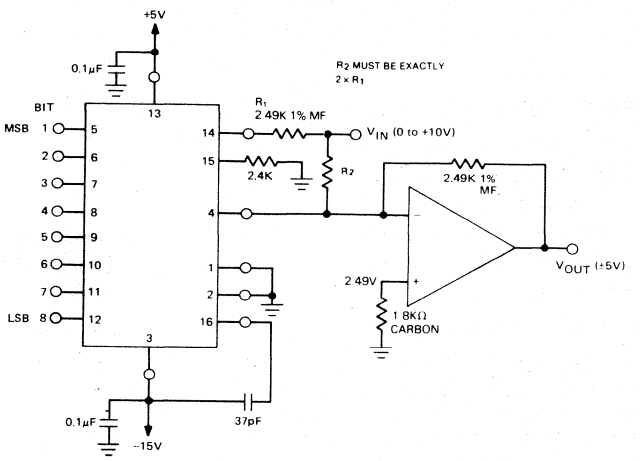
R_L	S.T.
0	300 nsec.
500	300 nsec.
1 K	400 nsec.
2.5 K	1.2 μsec.

APPLICATION DIAGRAMS

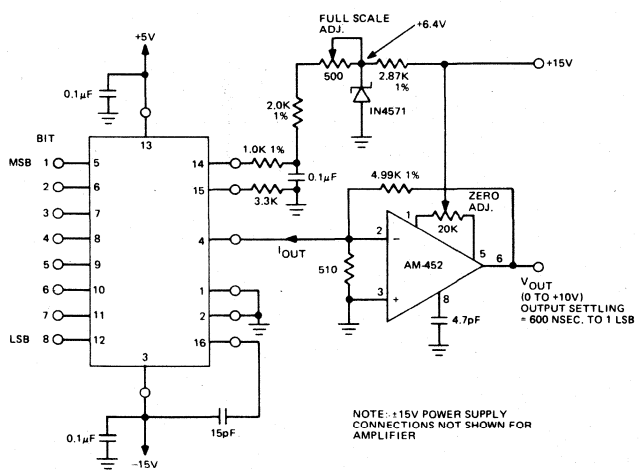
ONE QUADRANT MULTIPLICATION



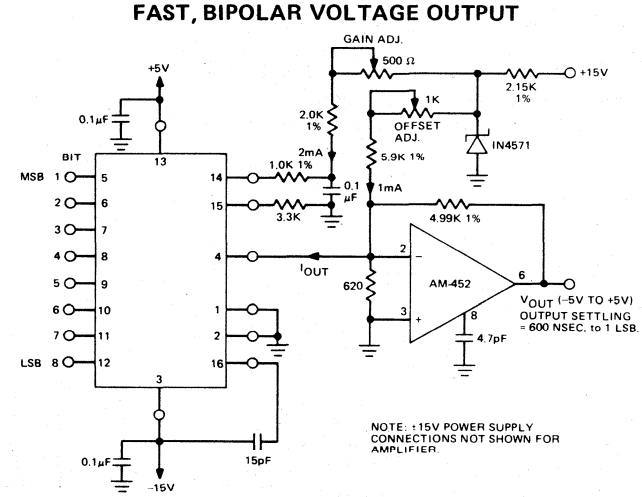
TWO QUADRANT MULTIPLICATION



FAST, UNIPOLAR VOLTAGE OUTPUT



FAST, BIPOLAR VOLTAGE OUTPUT



CALIBRATION AND CODING TABLES

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. *Zero and Offset Adjustments*
   For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.
3. *Gain Adjustment*
   For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the Coding Table.

UNIPOLAR OPERATION–STRAIGHT BINARY CODING

INPUT CODE	UNIPOLAR OUTPUT RANGES			
MSB LSB	0 TO +5V	0 TO +10V	0 TO −2MA	0 TO −4MA
1111 1111	+4.980	+9.961V	−1.992MA	−3.984MA
1110 0000	+4.375	+8.750	−1.750	−3.500
1100 0000	+3.750	+7.500	−1.500	−3.000
1000 0000	+2.500	+5.000	−1.000	−2.000
0100 0000	+1.250	+2.500	−0.500	−1.000
0000 0001	+0.020	+0.039	−0.008	−0.016
0000 0000	0.000	0.000	0.000	0.000

BIPOLAR OPERATION–OFFSET BINARY CODING

INPUT CODE	BIPOLAR OUTPUT RANGES			
MSB LSB	±5V	±10V	±1MA	±2MA
1111 1111	+4.961V	+9.922V	−0.992MA	−1.984MA
1110 0000	+3.750	+7.500	−0.750	−1.500
1100 0000	+2.500	+5.000	−0.500	−1.000
1000 0000	0.000	0.000	0.000	0.000
0100 0000	−2.500	−5.000	+0.500	+1.000
0000 0001	−4.961	−9.922	+0.992	+1.984
0000 0000	−5.000	−10.000	+1.000	+2.000

Low Cost, 10 Bit Monolithic Digital-to-Analog Converter DAC-IC10B Series

FEATURES

- 10 Bit Resolution
- Straight Binary Coding
- Current Output
- 250 nsec. Settling Time
- TTL/CMOS Compatible
- Low Cost

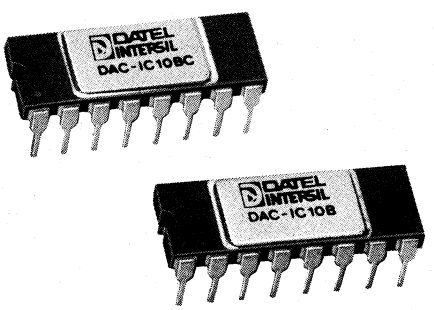
GENERAL DESCRIPTION

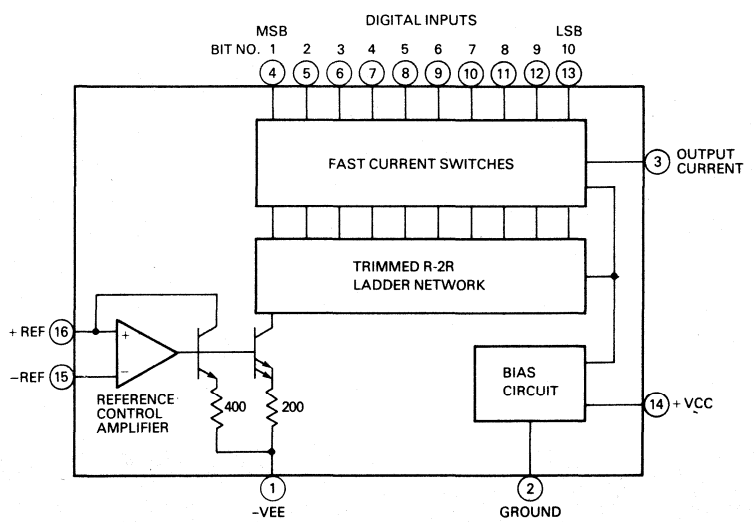
The DAC-IC10B is a low cost, 10 bit monolithic DAC with fast output current settling time. It is packaged in a 16 pin ceramic DIP and requires only an external reference and operational amplifier for voltage output operation. A full scale change in output current settles in 250 nanoseconds, and with a fast I.C. op amp (such as Datel-Intersil's AM-452) a 10V output change can settle within 1 microsecond. Digital input coding is straight binary for unipolar operation, and offset binary for bipolar operation; the logic inputs are compatible with TTL or CMOS.

This converter is manufactured with monolithic bipolar technology. The circuit incorporates 10 fast switching current sources which drive a diffused resistor R-2R network. The ladder network is laser trimmed by cutting aluminum links. The circuit also contains a reference control amplifier and a bias circuit. An external reference current of 2 mA is required at the + Reference input terminal; this is accomplished by an external voltage reference and a metal film resistor.

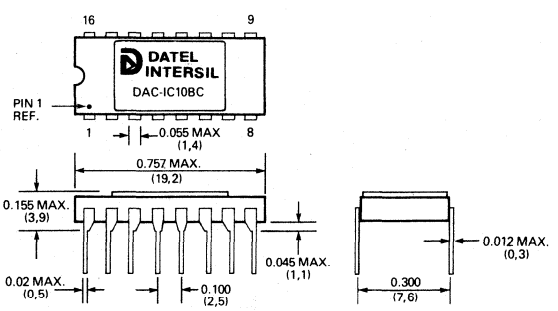
Other characteristics of the DAC-IC10B include linearity to ±½ LSB and guaranteed monotonic performance. The gain temperature coefficient of this unit is typically −20ppm/°C. Output voltage compliance is −2.5V to +0.2V, permitting direct driving of a 625 ohm resistor for a voltage output. The reference input current can be varied from 0.5 mA to 2.5mA to give monotonic operation as a one or two quadrant multiplier.

Power supply requirement is +5VDC and −15VDC. The DAC-IC10B is available in three models covering two temperature ranges, 0°C to +70°C and −55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−VEE
2	GROUND
3	OUTPUT CURRENT
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	+VCC
15	−REFERENCE
16	+REFERENCE

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-IC10B
(Typical at 25°C, V_{CC} = +5V, V_{EE} = −15V, I_{REF} = 2.0 mA)

MAXIMUM RATINGS

V_{CC}	+7.0 Volts
V_{EE}	+18.0 Volts
Digital Input Voltage	+15 Volts
Output Voltage, Pin 3	+0.5, −5.0 Volts
Ref. Current	2.5 mA
Diff. Ref. Voltage	0.7V

INPUTS

Resolution	10 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Level, Logic "1"	+2.0 to +15V @ +40μA
Input Level, Logic "0"	0 to +0.8V @ −0.4 mA
Nom. Ref. Current, Pin 16	2.0 mA
Reference Current Range	0.5 mA to 2.5 mA
Ref. Bias Current, Pin 15	−5 μA max.

OUTPUTS

Output Current	4.0 mA ±0.2 mA
Output Current Range	0 to 5.0 mA
Output Current, All Bits "0"	2.0 μA max.[1]
Output Voltage Compliance	−2.5 to +0.2V
Output Capacitance	25 pF

PERFORMANCE

Linearity Error, B, BM	±½ LSB, max.
BC	±1 LSB, max.
Diff. Linearity Error	±½ LSB
Monotonicity, B, BM	Full Temp. Range[2]
BC	At 25°C
Gain Tempco	−20 ppm/°C, 60 ppm/°C max.[3]
Ref. Current, Slew Rate	20 mA/μsec.
Ref. Current Settling	2.0 μsec.[4]
Output Current Settling	250 nsec.[5]
Update Rate	4 MHz
Power Supply Sensitivity	.02%/% max.

POWER REQUIREMENT

V_{CC} Voltage	+5 VDC ±0.25V
V_{CC} Current	18 mA max.
V_{EE} Voltage	−15 VDC ±0.75V
V_{EE} Current	−20 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	
DAC-IC10B, BC	0°C to +70°C
DAC-IC10BM	−55°C to +125°C
Storage Temp. Range	−65°C to +125°C
Package	16 Pin Ceramic DIP

NOTES:
1. 4.0 μA max. for DAC-IC10BC only.
2. All converters in this series typically retain rated monotonicity for values of input reference current from 0.5 mA to 2.5 mA.
3. 70 ppm/°C max. for DAC-IC10BM only.
4. Zero to 4 mA output change to rated accuracy.
5. Full scale change to ½ LSB.

ORDERING INFORMATION

MODEL	OPER. TEMP RANGE
DAC-IC10BC	0°C to +70°C
DAC-IC10B	0°C to +70°C
DAC-IC10BM	−55°C to +125°C

THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. The *General Connection Diagram* shows the basic connections for the converter. The scale factor is set by a reference current injected into pin 16. Pins 15 and 16 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R_{15} and pin 16 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R_{16}: $I_{REF} = V_{REF}/R_{16}$. R_{16} should be a stable metal film resistor. R_{15} is used only to compensate for the input bias current into pin 15 (1 μA typical). R_{15}, if used, should be equal to R_{16} and may be a carbon composition type. An I_{REF} of 2.0 mA is recommended for most applications.

2. There is a second method of connecting the reference shown in *Two Ways to Connect Reference.* A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 16 is at the negative voltage and I_{REF} still flows into pin 16. Again, R_{15} is used only to compensate for bias current. There is an important requirement for this connection: **the negative reference voltage must always be 3 volts above V_{EE}.**

3. I_{OUT} is inversely proportional to the reference input current (I_{REF}) times the digital word. Scaling of the applied reference can be represented as follows:

$$I_{OUT} = -2\left(\frac{V_{REF}}{R_{REF}}\right)\left(\frac{A_n}{2^n}\right)$$

where n = 10 (10 bit DAC)
A_n = digital code

Note: 1) The largest digital code for a 10 bit DAC is 1023.
2) The reference current is scaled by a factor of 2 within the DAC.

Example:

$$I_{OUT}(FS) = -2\left(\frac{2.5V}{1.25K}\right)\left(\frac{1023}{1024}\right)$$
$$= -3.996 \text{ mA (nominal)}$$

$$I_{OUT}(ZERO) = -2\left(\frac{2.5V}{1.25K}\right)\left(\frac{0}{1024}\right)$$
$$= 0 \text{ mA (nominal)}$$

4. The reference amplifier is internally compensated. The minimum reference current supplied from a current source is 0.5 mA for stability.

5. The voltage on pin 3 is restricted to a range of −2.5V to +0.2V. This compliance voltage is guaranteed at 25°C and nearly constant over temperature.

6. Full scale output current of 3.996 mA is guaranteed for input reference currents to pin 16 between 1.9 and 2.1 mA.

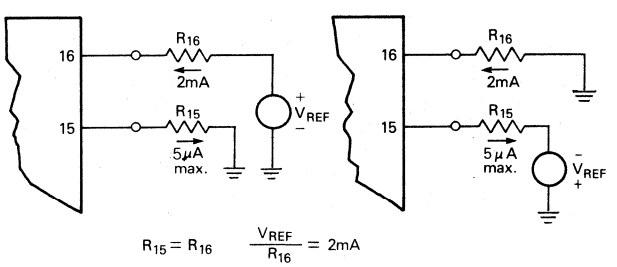
7. It is recommended that pin 14 (V_{CC}) and pin 1 (V_{EE}) always be bypassed to ground with at least 0.1 μF capacitors located close to the pins.

8. The accuracy of the converter is specified for a reference current of 2.0 mA; the accuracy, however, is essentially constant for reference currents from 1.5 mA to 2.5 mA. Typically, this device is monotonic for all values of reference current above 0.5 mA.

TECHNICAL NOTES (cont'd.)

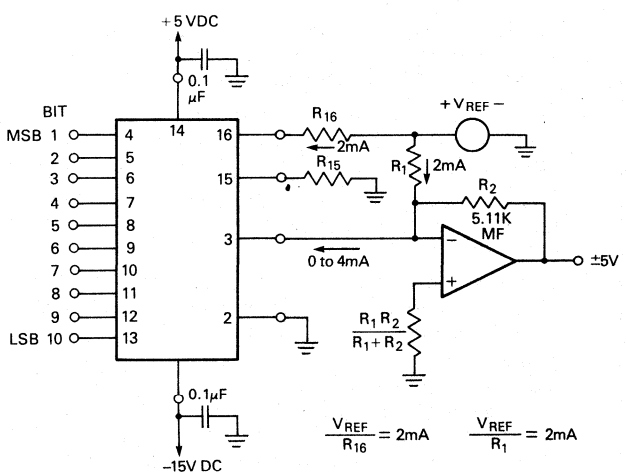
9. For fastest voltage output settling times in either unipolar or bipolar modes, two circuits using Datel-Intersil AM-452 monolithic operational amplifiers are recommended. These circuits, with the compensation shown, result in output settling times of typically 550 nsec. for a 10 volt change to 1 LSB. This is the worst case settling time which occurs when all bits are turned on. For current output and R_L less than 500 ohms, this time is 250 nsec.; when all bits are turned off the time is shorter, typically 100 nsec. The two circuits shown also illustrate a simple method of deriving both reference current and offset current from a precision 6.4 volt Zener reference diode.
10. Both one and two quadrant multiplication are also possible with the converter as shown in the two diagrams. V_{IN} is shown operating into pin 16; this results in an input impedance of 2.5K. Alternatively, V_{IN} can be applied to pin 15 for a high impedance input as explained previously. The range of V_{IN} is then 0 to −10V. For two quadrant multiplication V_{IN} is unipolar and the digital input is bipolar with offset binary coding. V_{OUT} then varies over the bipolar range of ±5 volts. In multiplication applications, it is recommended that full scale I_{REF} be set to 2.0 mA; the output is then monotonic as the reference current varies over 0.5 mA to 2.0 mA.

TWO WAYS TO CONNECT REFERENCE



$R_{15} = R_{16}$ $\quad \frac{V_{REF}}{R_{16}} = 2mA$

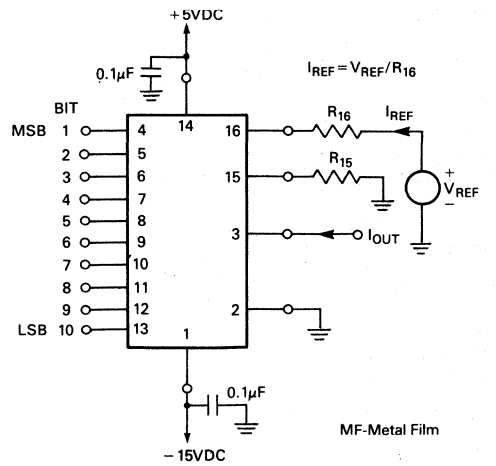
CONNECTION FOR BIPOLAR VOLTAGE OUT



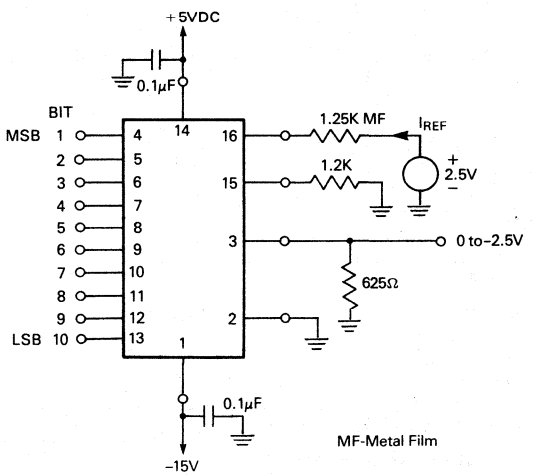
$\frac{V_{REF}}{R_{16}} = 2mA$ $\quad \frac{V_{REF}}{R_1} = 2mA$

CONNECTION DIAGRAMS

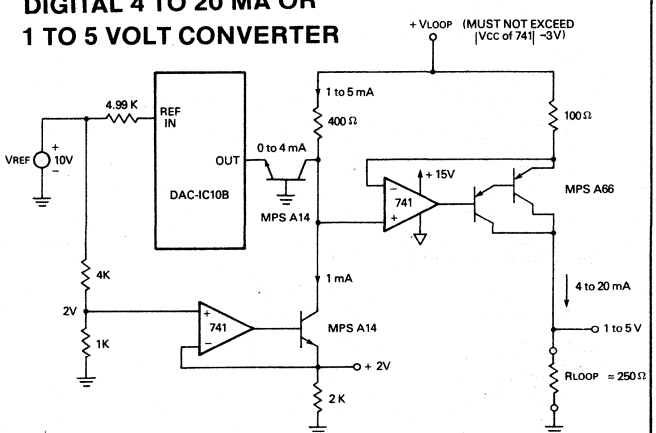
GENERAL CONNECTION DIAGRAM



CONNECTION FOR DIRECT VOLTAGE OUTPUT

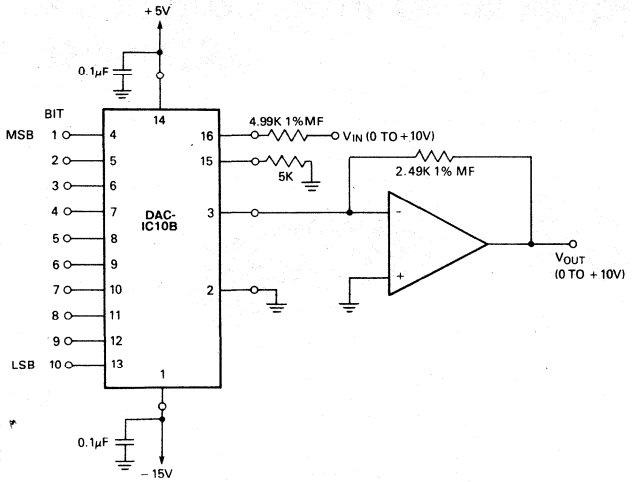


DIGITAL 4 TO 20 MA OR 1 TO 5 VOLT CONVERTER

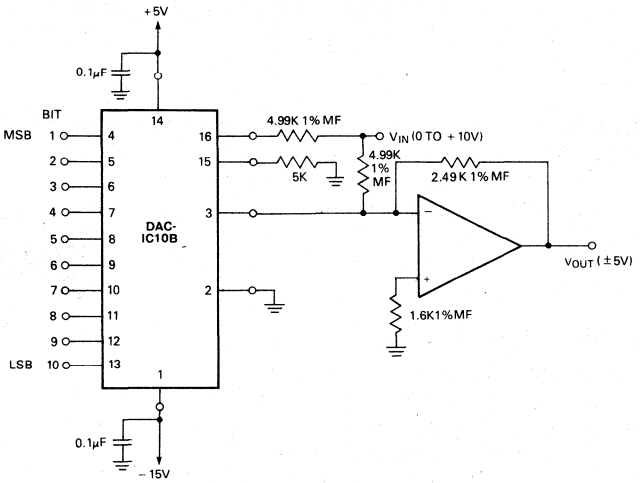


APPLICATION DIAGRAMS

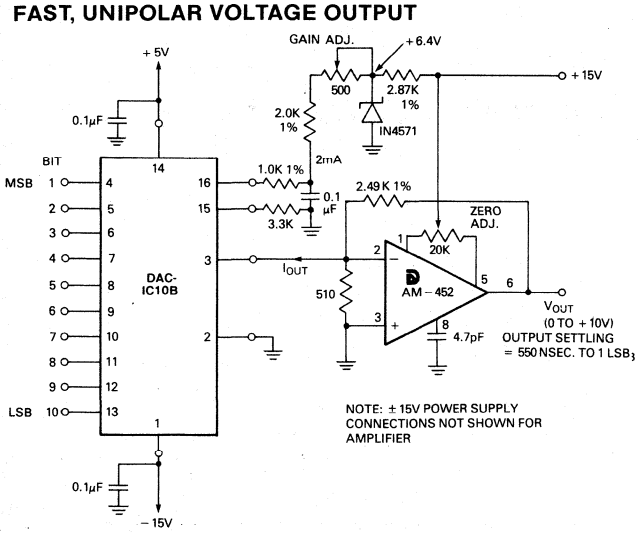
ONE QUADRANT MULTIPLICATION



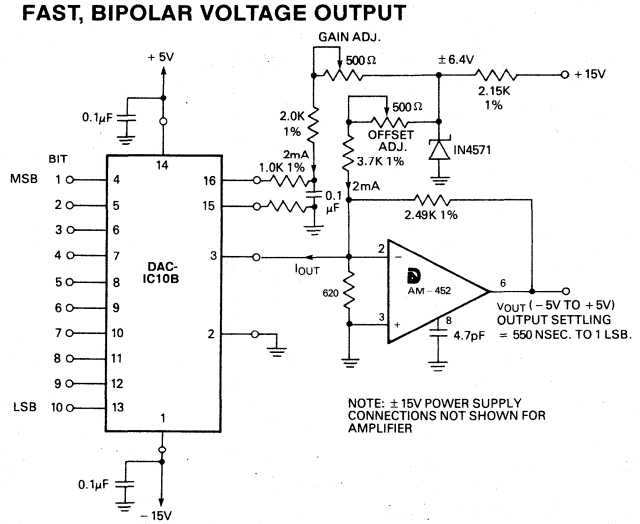
TWO QUADRANT MULTIPLICATION



FAST, UNIPOLAR VOLTAGE OUTPUT



FAST, BIPOLAR VOLTAGE OUTPUT



CALIBRATION AND CODING TABLE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. *Zero and Offset Adjustments*/ For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.
3. *Gain Adjustment*/ For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the Coding Table.

INPUT CODE MSB LSB	UNIPOLAR OPERATION—STRAIGHT BINARY 0 TO +5V	0 TO +10V	0 TO −2MA	0 TO −4MA
1 1 1 1 1 1 1 1 1 1	+4.995V	+9.990	−1.998 MA	−3.996
1 1 1 0 0 0 0 0 0 0	+4.375	+8.750	−1.750	−3.500
1 1 0 0 0 0 0 0 0 0	+3.750	+7.500	−1.500	−3.000
1 0 0 0 0 0 0 0 0 0	+2.500	+5.000	−1.000	−2.000
0 1 0 0 0 0 0 0 0 0	+1.250	+2.500	−0.500	−0.100
0 0 0 0 0 0 0 0 0 1	+0.005	+0.010	−0.002	−0.004
0 0 0 0 0 0 0 0 0 0	0.000	0.000	0.000	0.000

INPUT CODE MSB LSB	BIPOLAR OPERATION—OFFSET BINARY CODING ±5V	±10V	±1MA	±2MA
1 1 1 1 1 1 1 1 1 1	+4.990V	+ 9.980V	−0.998MA	−1.996MA
1 1 1 0 0 0 0 0 0 0	+3.750	+ 7.500	−0.750	−1.500
1 1 0 0 0 0 0 0 0 0	+2.500	+ 5.000	−0.500	−1.000
1 0 0 0 0 0 0 0 0 0	0.000	0.000	0.000	0.000
0 1 0 0 0 0 0 0 0 0	−2.500	− 5.000	+0.500	+1.000
0 0 0 0 0 0 0 0 0 1	−4.990	− 9.980	+0.998	+1.996
0 0 0 0 0 0 0 0 0 0	−5.000	−10.000	+1.000	+2.000

High Speed, 8 Bit Monolithic Digital-to-Analog Converter DAC-08B

FEATURES

- **85 nsec Settling Time**
- **−10 to +18 Volt Compliance**
- **±4.5 to ±18 Volt Supply**
- **8 Bit Resolution**
- **1 or 2 Quadrant Multiplication**
- **Low Cost**

GENERAL DESCRIPTION

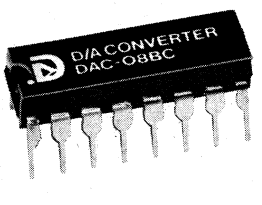
The DAC-08BC and DAC-08BM provide very high speed performance coupled with low cost and application flexibility. These units have guaranteed full 8-bit monotonicity with nonlinearity of 0.19% over the full operating temperature range. High speed current steering switches achieve 85 nanosecond settling time with a very low glitch for full scale changes. A large output voltage compliance range (−10 to +18 Volts) allows direct current to voltage conversion with just an output resistor, omitting the need for an op amp in many cases.

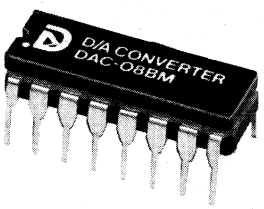
The DAC-08 consists of 8 fast-switching current sources, a diffused R-2R resistor ladder, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of 10 ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling and low cost. Linearity is ±½ LSB.

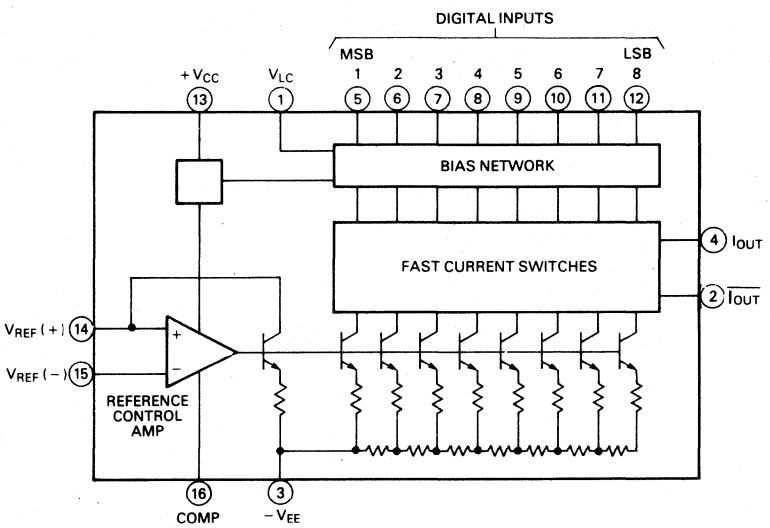
An external reference current of 2 mA nominal programs the scale factor of the DAC. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar dependent upon the connection of the two complementary output sink currents.

DAC-08 applications include fast A/D converters, waveform generators, audio encoder and attentuators, CRT display drivers, and high speed modems.

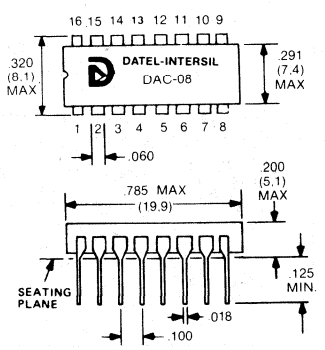
Power supply requirements are ±4.5V to ±18V. Operating temperature range is 0°C to 70°C for the DAC-08BC and −55°C to +125°C for the DAC-08BM. These models have equivalent specs and pinouts to industry standard DAC-08's.







MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	THRESHOLD CONTROL (VLC)
2	$\overline{IOUT}$
3	VEE
4	IOUT
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (LSB)
13	VCC
14	VREF+
15	VREF−
16	COMPENSATION

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SPECIFICATIONS. DAC-08BC & DAC-08BM

(Typical at 25°C, Vs = ±15V, I_{REF} = 2.0 mA unless otherwise noted)

MAXIMUM RATINGS

V_{CC} Supply to V_{EE} Supply	36V
Digital Input Voltage	$-V_{EE}$ to $-V_{EE}$ plus 36V
V_{LC}	$-V_{EE}$ to $+V_{CC}$
Reference Input Voltage	$-V_{EE}$ to $+V_{CC}$
Reference Input Current	5.0 mA

INPUTS

Resolution	8 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Logic Level, Bit ON ("1")	+2.0V min. @ +10.0μA
Input Logic Level, Bit OFF ("0")	+0.8V max. @ −10.0μA[1]
Nominal Reference Current	2.0 mA
Reference Bias Current	−1.0 μA
Reference Input Slew Rate	8 mA/μsec

OUTPUTS

Output Current, I_{REF} = 2.0 mA	1.99 mA ±.05 mA[2]
Output Current Range, V_{EE} = −5V	0 to 2.1 mA
Output Current Range, V_{EE} = −7 to −18V	0 to 4.2 mA
Output Current, all bits OFF	±0.2μA typ. ±2.0μA max.
Full Scale Symmetry	±1.0 μA typ. ±8.0 μA max.
Output Voltage Compliance	−10 to +18V

PERFORMANCE

Relative Accuracy	±½ LSB (±0.19%) max.
Nonlinearity	±½ LSB (±0.19%) max.
Differential Nonlinearity	±½ LSB (±0.19%)
Full Scale Tempco	±10 ppm/°C typ. ±50 ppm/°C max.
Settling Time, 2 mA to ½LSB	85 nsec. typ., 150 nsec. max.
Propagation Delay	60 nsec. max.
Power Supply Sensitivity, I_{REF} = 1 mA	±0.002%/%

POWER REQUIREMENTS

V_{CC}	+4.5V to +18V
V_{EE}	−4.5V to −18V
Power Supply Current, I_{REF} = 1.0mA	
V = ±5V	+3.8, −5.8 mA max.
Power Supply Current, I_{REF} = 2.0mA	
V = +5V, −15V	+3.8, −7.8 mA max.
V = ±15V	+3.8, −7.8 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp Range	
DAC-08BC	0°C to 70°C
DAC-08BM	−55°C to 125°C
Storage Temp Range	−65°C to −150°C
Package	16 Pin Dip

NOTES

1. For TTL, DTL Interface, V_{LC} = 0V. For other digital interfaces see TECHNICAL NOTE 3.
2. I_{OUT} (Pin 4) + I_{OUT} (Pin 2) = Output Current.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PACKAGE
DAC-08BC	0°C to 70°C	Plastic
DAC-08BM	−55°C to +125°C	Ceramic

THESE D/A CONVERTERS ARE COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. The DAC-08 series is a multiplying D/A converter in which the output current is a product of the digital word and the input reference current. Excellent performance is obtained for I_{REF} from 4.0 mA to 4.0 μA. Monotonic operation is maintained from 4.0 mA to 100 μA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \quad (I_{REF} \text{ is current at Pin 14})$$

2. **Reference Amplifier Set-up.** If a regulated power supply is used as the reference, a resistor divider should be used with the junction by-passed to gnd with a 0.1 μf capacitor. TTL logic supplies are not recommended to be used as the reference. AC and DC reference applications will require the reference amplifier to be compensated using a capacitor (C_C) from pin 16 to V_{EE}. For fixed reference application (DC). a 0.01 μF capacitor is recommended. For AC reference applications, the value of C_C depends on the impedance present at pin 14. For R_{REF} values of 1.0, 2.5 and 5.0 KΩ, minimum values of C_C are 15, 37 and 75 pf respectively. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin. See Graph on Reference Input Frequency Response. Low R_{REF} values enable small C_C achieving highest throughput on V_{REF}. If pin 14 is driven by a high impedance such as a transistor current source, the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{REF} = 1.0 KΩ and C_C = 15 pf, the reference amplifier slews at 4.0 mA/μsec. enabling a transition from I_{REF} = 0 to I_{REF} = 2.0 mA in 500 nsec.

3. **Interfacing Various Logic Families.** The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. A large input swing capability allows adjustable logic threshold voltage and 200 μA max source current on pin 1. Minimum input logic swing and minimum logic threshold voltage is given by V_{EE} + (I_{REF} x 1.0 kΩ) +2.5V. Logic threshold is adjusted by appropriate voltage at V_{LC}. Interfacing Various Logic Families Diagram shows appropriate connections. Fastest settling times are obtained when V_{LC} sees a low impedance. Use .01 μF by-pass capacitors whenever possible.

4. **Analog Output Currents.** Both true and complemented output sink currents are provided, $I_O + \overline{I_O} = I_{FS}$. Both outputs can be used simultaneously. If one of the outputs is not required, it must be connected to ground or a point capable of sourcing I_{FS}. **Do not leave unused output pin** (I_O or $\overline{I_O}$) **open.** The compliance voltage is the voltage swing on output pin without affecting DAC accuracy. Positive compliance is 36V above V_{EE} and is independent of V +. Negative compliance is V_{EE} + (I_{REF} x 1kΩ) +2.5V.

5. **Settling Time.** The DAC-08 is capable of extremely fast settling times, typically 85 nsec. at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance. The output capacitance of the DAC including the package is approximately 15 pf; therefore the output RC time constant dominates at $R_L > 500\Omega$.

   Settling time remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The switching transients (glitches) are very low and may be further reduced by small capacitive loads at the output. Settling time will be increased slightly.

6. **Power Supplies.** The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example,

TECHNICAL NOTES (Cont'd)

operation at −4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network. It is recommended that V_{CC} and V_{EE} always be bypassed to ground with at least 0.1 μf capacitors.

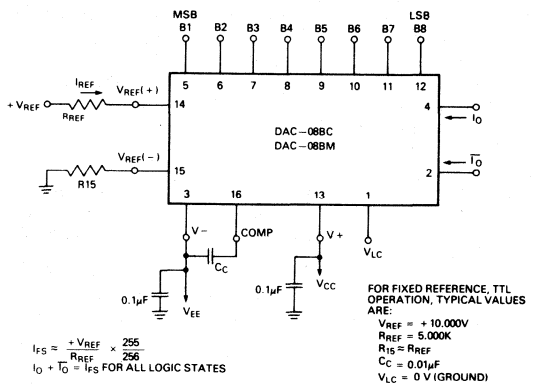
Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible, as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:
$P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

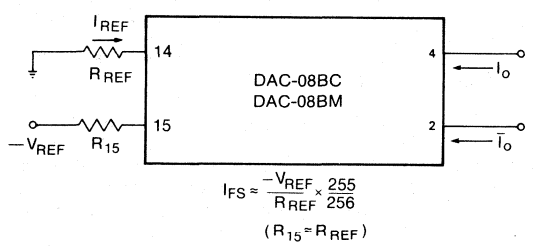
7. **Temperature Performance.** For most applications, a +10.0 Volt reference is recommended for optimum full scale temperature coefficient performance. Full scale trimming may by accomplished by adjusting I_{REF} (changing value of R_{REF}). R_{REF} and R_L should be selected for similar temperature coefficient to minimize accuracy error. Settling time of the DAC decreases approximately 10% at −55°C and increases 15% at 125°C.

APPLICATION DIAGRAMS

BASIC POSITIVE REFERENCE OPERATION

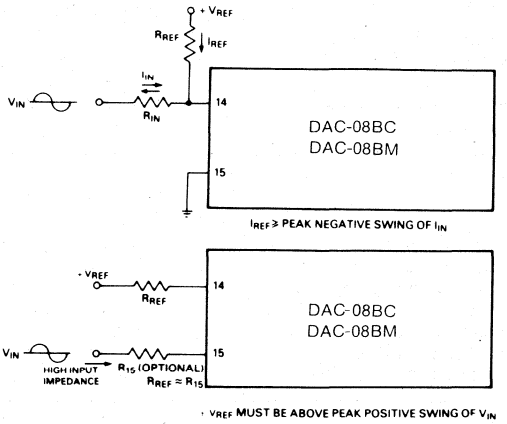


BASIC NEGATIVE REFERENCE OPERATION

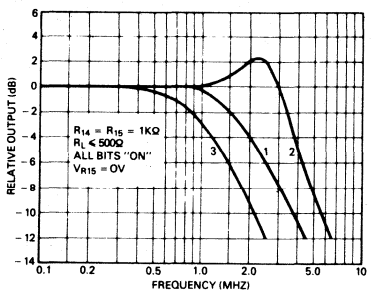


APPLICATION DIAGRAMS (Cont'd)

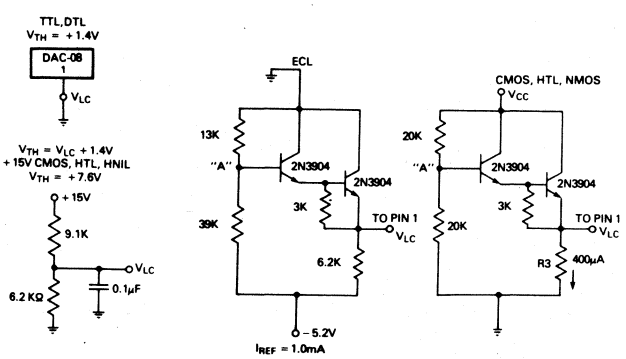
ACCOMMODATING BIPOLAR REFERENCES



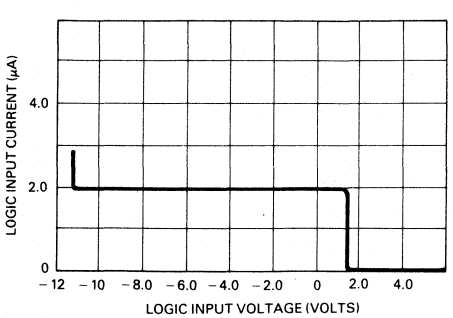
REFERENCE INPUT FREQUENCY RESPONSE



INTERFACING VARIOUS LOGIC FAMILIES

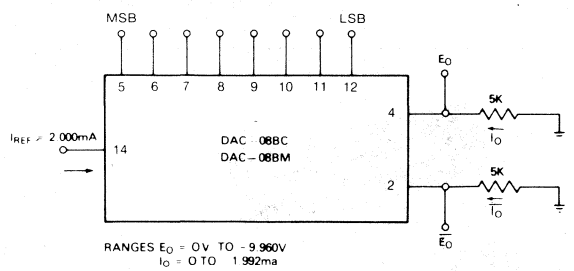


LOGIC INPUT CURRENT VS. INPUT VOLTAGE



APPLICATION DIAGRAMS (Cont'd)

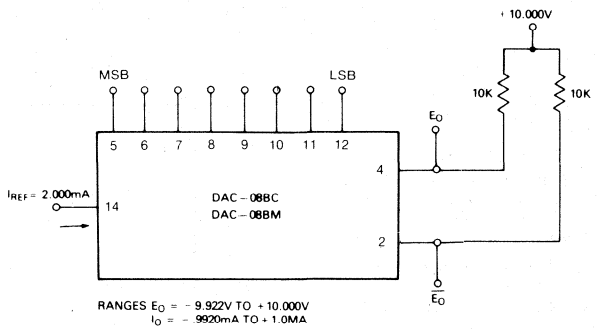
BASIC UNIPOLAR NEGATIVE OPERATION



RANGES E_O = 0V TO −9.960V
I_O = 0 TO 1.992ma

SEE CODING TABLE

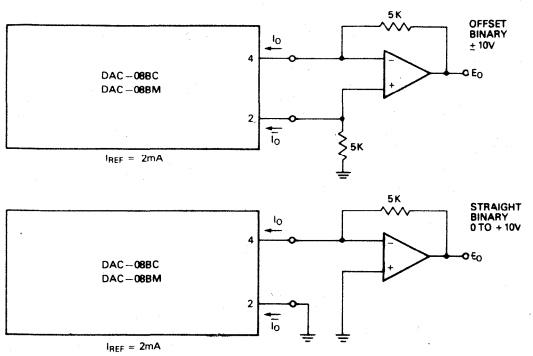
BASIC BIPOLAR OUTPUT OPERATION



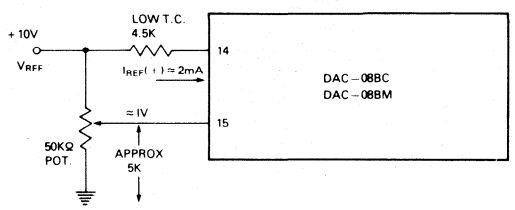
RANGES E_O = −9.922V TO +10.000V
I_O = −.9920mA TO +1.0MA

SEE CODING TABLE

VOLTAGE OUTPUT OPERATION



RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



CALIBRATION AND CODING TABLES

CALIBRATION PROCEDURE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.

2. **Zero and Offset Adjustments**
   For unipolar operation, set all digital inputs to "0" and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.

3. **Gain Adjustment**
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the DAC-08B Coding Table.

UNIPOLAR OPERATION—STRAIGHT BINARY CODING

For 5k load resistors at pins 2 and 4

INPUT CODE	E_O	$\overline{E_O}$	I_O	$\overline{I_O}$
1111 1111	−9.961	0.000	1.992	0.000
1110 0000	−8.750	−1.211	1.750	0.242
1100 0000	−7.500	−2.461	1.500	0.492
1000 0000	−5.000	−4.961	1.000	0.992
0100 0000	−2.500	−7.461	0.500	1.492
0000 0001	−0.039	−9.922	0.008	1.984
0000 0000	0.000	−9.961	0.000	1.992

BIPOLAR OPERATION—OFFSET BINARY CODING

For 10k load resistors from pins 2 and 4 to +10V.

INPUT CODE	E_O	$\overline{E_O}$
1111 1111	− 9.922	+10.000
1110 0000	− 7.500	+ 7.578
1100 0000	− 5.000	+ 5.078
1000 0000	0.000	+ 0.078
0100 0000	+ 5.000	− 4.922
0000 0001	+ 9.922	− 9.844
0000 0000	+10.000	− 9.922

8-Bit Monolithic D/A Converter with Input Register DAC-UP8B

FEATURES

- **Input Register**
- **Internal Reference**
- **Voltage Output**
- **Low Cost**
- **8-Bit Resolution**

GENERAL DESCRIPTION

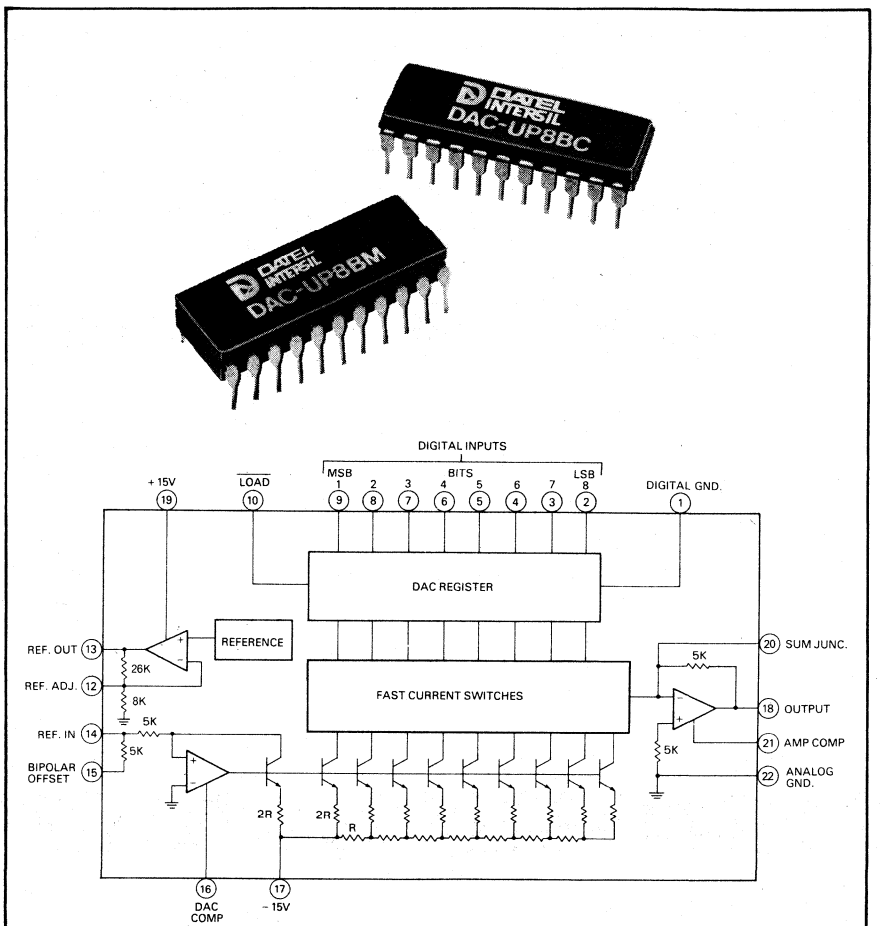
The DAC-UP8BC and DAC-UP8BM are 8-bit monolithic DAC's with internal registers. Contained in the 22 pin DIP is a 8-bit DAC, stable reference, a high-speed output amplifier and an 8-bit input latch. These microprocessor compatible converters are ideal for low cost applications.

The output voltage range is 0 to + 10V for unipolar mode and ± 5V for bipolar. Typical settling time is 2 μsec for a full scale change. Either the internal reference or an external reference can be used to bias the current switching network. The converter can function as a multiplying DAC by varying the reference input voltage. The reference and output amplifier are short circuit protected.

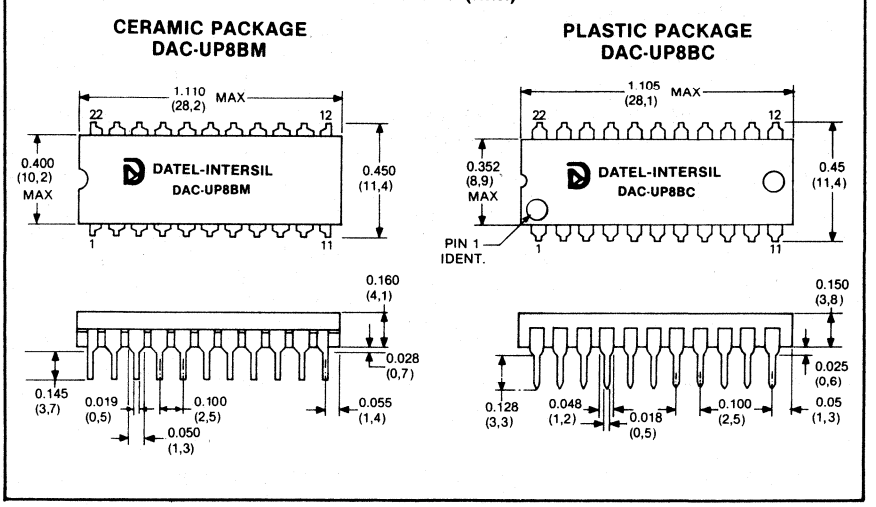
The input register is controlled by an enable line (LOAD). When low, the registers are transparent and any change on the digital input pins will be reflected on the analog output. A high state level will latch this digital information, and the data is retained until this enable line goes low. The data and latch enable input lines have low input load currents.

The DAC design consists of 8 fast-switching current sources, a diffused R-2R resistor ladder network and a control amplifier. The diffused resistor network gives excellent temperature tracking resulting in a gain temperature coefficient of 30 ppm/°C. This bipolar monolithic fabrication results in excellent linearity and temperature coefficient.

With an accuracy of .19% the device is monotonic (no missing codes) over the entire operating temperature range. Power supply requirements are ± 12V to ± 18V. The operating temperature range of the DAC-UP8BC is 0 to + 70 °C while the DAC-UP8BM operates from − 55 °C to + 125 °C.



MECHANICAL DIMENSIONS INCHES (MM)



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-UP8BC & DAC-UP8BM

(Typical at 25°C, ±15V Supply. Ref. In = +5V unless otherwise noted)

MAXIMUM RATINGS

Positive Supply, pin 19	+ 18V
Negative Supply, pin 17	− 18V
Digital Input Voltage, pins 2-10	+ 18V
Reference Input, pin 14	+ 12V
Summing Junction, pin 20	+ 12V

INPUTS

Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+ 2.0V to + 5.5V @ 10 μA
Input Logic Level, bit OFF ("0")	0V to + 0.8V @ − 50 μA
Load Input	HI ("1") = Hold Data LO ("0") = Transfer Data
Load Pulse Width[1]	200 nsec min.
Reference Input Voltage	+ 5V ± 10%
Reference Input Resistance	5K
Reference Input Slew Rate	25V/μsec.

OUTPUT

Output Voltage Range, unipolar	0 to +10V
Output Voltage Range, bipolar	± 5V
Output Current	5mA
Output Resistance	5 ohms
Reference Output Voltage	+ 5V ± 10%
Reference Output Current	5mA

PERFORMANCE

Linearity Error	± ½ LSB max.
Differential Linearity Error	± ½ LSB
Monotonicity	8 Bits over oper. temp. range
Gain Error	Adjustable to zero
Zero Error	Adjustable to zero
Gain Tempco	20 ppm/°C
Zero Tempco, Unipolar	5 ppm/°C of FS.
Offset Tempco, Bipolar	10 ppm/°C of FS.
Reference Tempco	60 ppm/°C
Settling Time to ½ LSB[2]	2 μsec
Power Supply Rejection	± 1mV/V

POWER REQUIREMENT

Rated Power Supply Voltage	± 15V DC
Power Supply Voltage Range	± 12 to ± 18V DC
Supply Current, quiescent	+ 7mA, − 10mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to + 70°C (BC) 55°C to +125°C (BM)
Storage Temperature Range	− 65°C to +150°C
Package Type	22 pin plastic (BC) 22 pin ceramic (BM)

NOTES:

1. See Timing Diagram
2. For 10V change

TECHNICAL NOTES

1. It is recommended that the ± 15V power input pins both be bypassed to ground with 0.1 μf ceramic capacitors. This precaution will assure noise free operation of the converter.

2. Both the Output (pin 18) and Reference Output (pin 13) are short circuit protected. Output short circuit current is typically 40 mA for the Output and 15 mA for the Reference Output.

3. The "LOAD" control pin is a level triggered input which causes the register to hold data with a logic "1" input state and transfer data to the DAC with a logic "0" input.

4. A Setup Time of 200 nsec. minimum must be allowed for the input data before the LOAD input goes from LO to HI. In addition, a 50 nsec. minimum Hold Time must be allowed for the input data after the LOAD input goes from LO to HI. The minimum pulse width for the LOAD input is 200 nsec. The maximum update rate is determined by the output settling time. See Timing Diagram.

5. The output settling time may be decreased somewhat by decreasing the value of the 50 pF feedback capacitor from the amplifier Output (pin 18) to the Summing Junction (pin 20). The minimum capacitance value is 10 pF.

6. The gain temperature coefficient of the DAC-UP8B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm typical results for the converter. If greater temperature stability is required, a more stable external reference should be used.

7. The data inputs (Bits 1 through 8) are high impedance inputs which give minimal logic loading. For an input LO, the current that must be sinked is only 50 μA maximum, or about 1/32 of a standard TTL load. This minimizes the loading of the DAC-UP8B on a data bus.

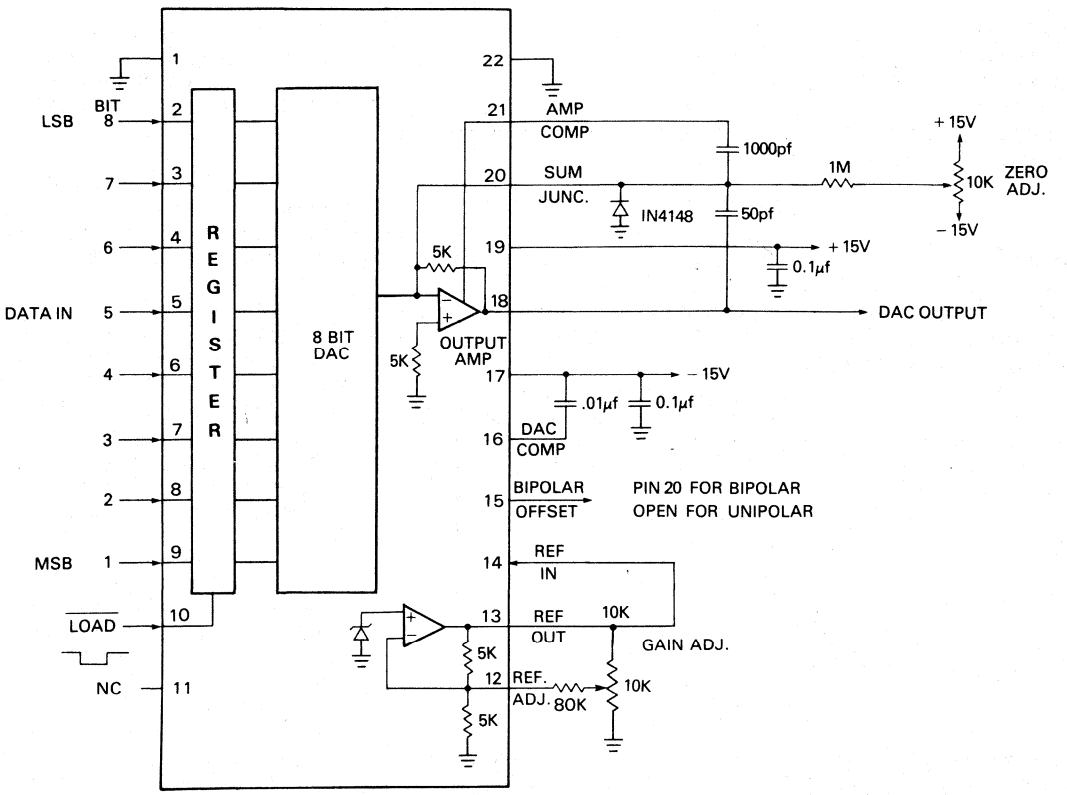
ORDERING INFORMATION

MODEL	OPERATING TEMP RANGE	CASE
DAC-UP8BC	0 to 70°C	Plastic
DAC-UP8BM	− 55 to 125°C	Ceramic

Trimming Potentiometers: TP10K

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CONNECTION AND CALIBRATION



CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION table.
2. Apply a logic "0" to $\overline{\text{LOAD}}$ (pin 10).
3. **Zero and Offset Adjustments**
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for negative full scale voltage. of −5.000V.
4. **Gain Adjustment**
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust FULL SCALE ADJ for the positive full scale voltage of +9.961V (unipolar) or +4.961V (bipolar).

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	DIGITAL GND
2	BIT 8 IN (LSB)
3	BIT 7 IN
4	BIT 6 IN
5	BIT 5 IN
6	BIT 4 IN
7	BIT 3 IN
8	BIT 2 IN
9	BIT 1 IN (MSB)
10	$\overline{\text{LOAD}}$
11	NC

PIN	FUNCTION
12	REF ADJ
13	REF OUT
14	REF IN
15	BIPOLAR OFFSET
16	DAC COMP
17	−15V
18	OUTPUT
19	+15V
20	SUM JUNCTION
21	AMP COMP
22	ANALOG GND

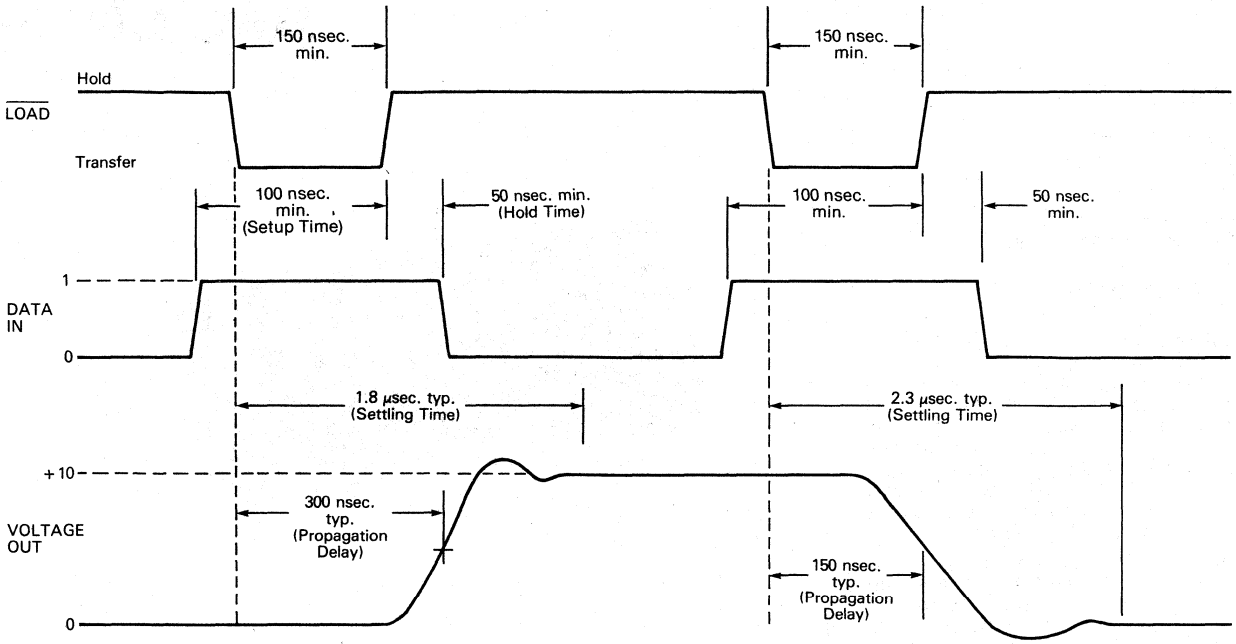
CODING TABLE

INPUT CODE MSB				LSB				OUTPUT RANGES 0 to +10V	±5V
1	1	1	1	1	1	1	1	+9.961V	+4.961V
1	1	1	0	0	0	0	0	+8.750	+3.750
1	1	0	0	0	0	0	0	+7.500	+2.500
1	0	0	0	0	0	0	0	+5.000	0.000
0	1	0	0	0	0	0	0	+2.500	−2.500
0	0	0	0	0	0	0	1	+0.039	−4.961
0	0	0	0	0	0	0	0	0.000	−5.000

OUTPUT RANGE SELECTION

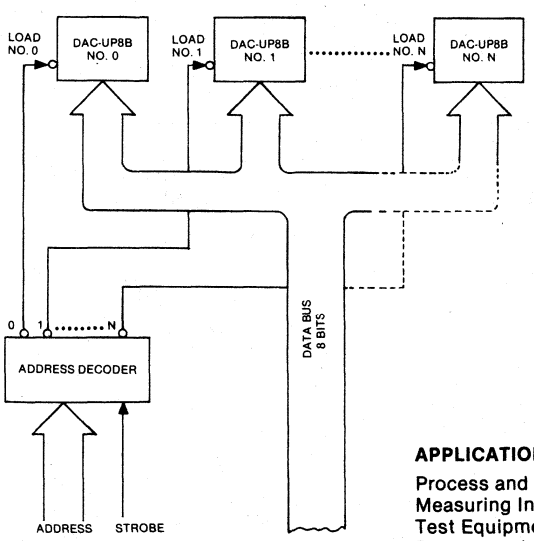
MODE	RANGE	CONNECTION
Unipolar	0 to +10V	Pin 15 open
Bipolar	±5V	Pin 15 to 20

TIMING DIAGRAM



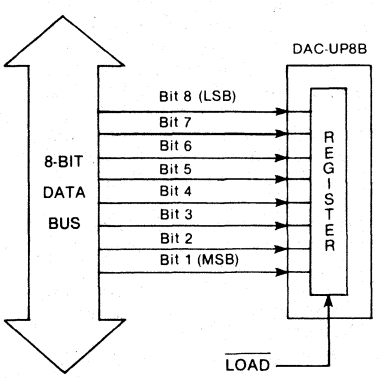
APPLICATIONS

INTERFACING TO 8 BIT DATA BUS



APPLICATIONS

Process and Control
Measuring Instruments
Test Equipment
Programmable Power Supplies
Computer I/O Equipment



This illustrates the connection for loading parallel data into the input register. The register circuit is a static latch and is controlled by the $\overline{\text{LOAD}}$, active low. When the data is stable on the data inputs (bits 1-8), it can be transferred on the positive edge of the $\overline{\text{LOAD}}$ pulse. The voltage levels on the data bus should be stable for at least 200 nsec before $\overline{\text{LOAD}}$ goes HI. The minimum pulse width of the $\overline{\text{LOAD}}$ command is 200 nsec.

NEW

DATEL

10 Bit Monolithic DAC With Input Registers DAC-UP10B

FEATURES

- **Input Registers**
- **10-Bit Resolution**
- **Voltage Output**
- **Internal Reference**
- **Guaranteed Monotinicity**

GENERAL DESCRIPTION

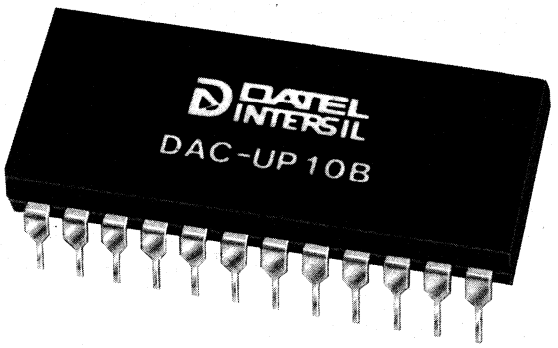
The DAC-UP10B is a low cost, monolithic 10 bit D/A converter with internal registers. The device also includes a high speed output amplifier, stable internal reference, and an input reference amplifier. Low loading latches, adjustable logic thresholds and addressing capability allow the DAC-UP10B to directly interface with many microprocessor and logic controlled systems.

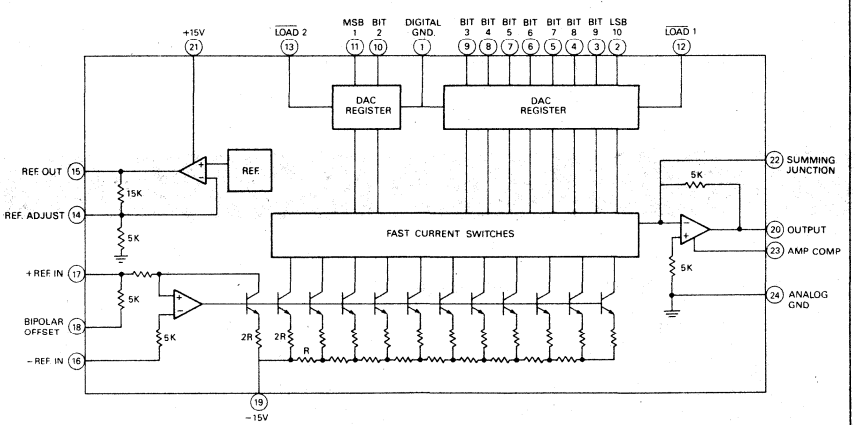
The input registers are controlled by two enable lines ($\overline{\text{LOAD}}$ 1, $\overline{\text{LOAD}}$ 2). When the enable inputs are low, the registers are active, and any change on the digital inputs will be reflected on the analog output. When the enable inputs are high, the digital inputs become very high impedances and the data present is retained until the enable lines go low. The two enable inputs allow the converter to be directly interfaced with an 8 bit data bus.

The output voltage range is 0 to + 10V for unipolar mode, ± 5V for bipolar. A full scale output change settles to within 0.05% in 5 μsec. The internal band gap reference is buffered and amplified to provide the 5V reference output. Either the internal reference or, for increased accuracy, an external reference can be used to bias the current switching networks.

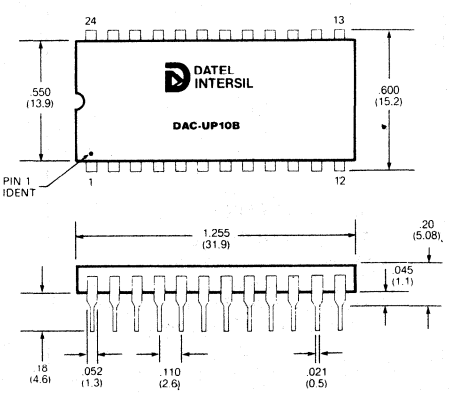
Other characteristics of the DAC-UP10B include guaranteed monotonic performance, a Gain Temperature Coefficient of only 20 ppm/°C, and Zero Tempco of 5 ppm/°C. The power supply voltage range is ± 11.4 VDC to ± 16.5 VDC.

The DAC-UP10B is packaged in a 24 pin plastic DIP, and operation is specified over the 0 to + 70°C operating temperature range.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIG. GRND	13	$\overline{\text{LOAD}}$ 2
2	BIT 10 IN (LSB)	14	REF. ADJ
3	BIT 9 IN	15	REF. OUT
4	BIT 8 IN	16	– REF IN
5	BIT 7 IN	17	+ REF IN
6	BIT 6 IN	18	BIPOLAR OFF.
7	BIT 5 IN	19	– 15 VDC
8	BIT 4 IN	20	OUTPUT
9	BIT 3 IN	21	+ 15 VDC
10	BIT 2 IN	22	SUM. JUNC.
11	BIT 1 IN	23	AMP. COMP.
12	$\overline{\text{LOAD}}$ 1	24	ANALOG GRND.

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-UP10B
(Typical at +25°C, ± 15 VDC supplies, ref in = +5V unless otherwise noted).

MAXIMUM RATINGS	
Positive Supply, Pin 21	+18V
Negative Supply, Pin 19	−18V
Digital Input Voltage, Pins 2-11	+18V
Reference Input, Pin 17	+12V
Summing Junction, Pin 22	+12V
INPUTS	
Resolution	10 Bits
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary
Input Logic Level, Bit ON ("1") min.[1]	+2V @ 10 μA
BIT OFF ("0") max.[1]	+0.8V @ 10 μA
$\overline{\text{Load}}$ Inputs	HI ("1") = Hold Data
	LO ("0") = Transfer Data
$\overline{\text{Load}}$ Pulse Width, min.	150 nsec
Reference Input Voltage	5V ± 10%
Reference Input Resistance	5 kΩ
OUTPUT	
Output Voltage Range, Unipolar	+10V
Bipolar	±5V
Output Current	5 mA
Reference Output Voltage[2]	5V ± 10%
Reference Output Current, max.	3 mA
PERFORMANCE	
Linearity Error, max.	± 1 LSB
Differential Linearity Error	± 1 LSB
Monotinicity	Over Operating Temp. Range.
Gain Error	Adjustable to Zero
Zero Error	Adjustable to Zero
Gain Tempco[3]	20 ppm/°C
Zero Tempco, Unipolar[3]	5 ppm/°C
Reference Tempco[2]	60 ppm/°C
Settling Time, 10V to .05%	5 μsec
Power Supply Sensitivity, max.	± 0.01% FS/%VS
POWER REQUIREMENT	
Rated Power Supply Voltage	± 15 VDC
Power Supply Voltage Range	± 11.4 VDC to ± 16.5 VDC
Supply Current, Quiescent max.[4]	+14 mA, −15 mA
Power Dissipation, max.[4]	435 mW
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package	24 Pin Plastic Dip

NOTES:
1. Bias circuits are shown on page 3 that will provide the proper threshold voltage levels for various logic families. See technical note 3.
2. Ref. output current = 1 mA
3. Ref. in = + 5V
4. V_S = ± 15VDC, Iref = 1mA

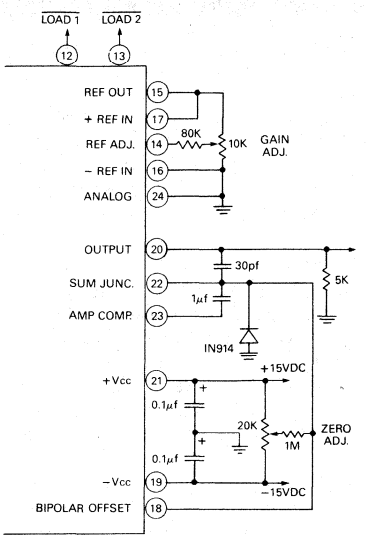
TECHNICAL NOTES

1. The $\overline{\text{Load}}$ control inputs (pins 12,13) are level triggered inputs. The $\overline{\text{Load}}$ 2 input (pin 13) controls the two most significant bits while the $\overline{\text{Load}}$ 1 input (pin 12) controls the eight least significant bits. When the $\overline{\text{Load}}$ inputs are "Logic 1", the input registers will hold the data present, a "Logic 0", activates the registers, transferring data to the converter output.
2. A set-up time of 100 nsec. minimum must be allowed before the $\overline{\text{Load}}$ inputs go from LO to HI. In addition, a 50 nsec minimum Hold Time must be allowed for the input data after the $\overline{\text{Load}}$ inputs go from LO to HI. The minimum pulse width for the $\overline{\text{Load}}$ inputs is 150 nsec. The maximum update rate is determined by the output settling time. See Timing Diagram.
3. The digital inputs of the DAC-UP10B utilize a differential logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (pin 1). Bias circuits are shown that will provide the proper threshold voltage levels for various logic families.
4. The −Ref input (pin 16) is uncommitted to allow utilization of negative polarity reference voltages. In this mode, the +Ref input (pin 17) is grounded and the negative reference is tied directly to the −Ref pin.
5. It is recommended that the ± 15V power input pins both be bypassed to ground with 0.1 μf ceramic capacitors. Also, to minimize capacitance, external resistors should be mounted as close to the ref. adj. pin (pin 14) as possible. These precautions along with good layout practices will insure noise free operation.
6. The gain tempco of the DAC-UP10B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm/°C typical results for the converter. If greater temperature stability is required, a more stable external reference may be used.
7. The output amplifier incorporates output short circuit protection for both positive and negative excursions. Short circuit current is typically limited at ± 15 mA.

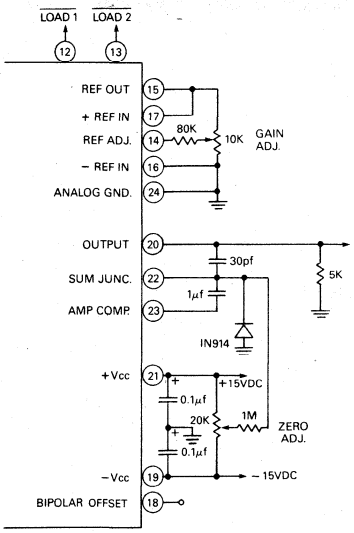
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
DAC-UP10BC	0 to +70°C
Trimming Potentiometers:	TP10K, TP20K

CONNECTION AND CALIBRATION



BIPOLAR OPERATION

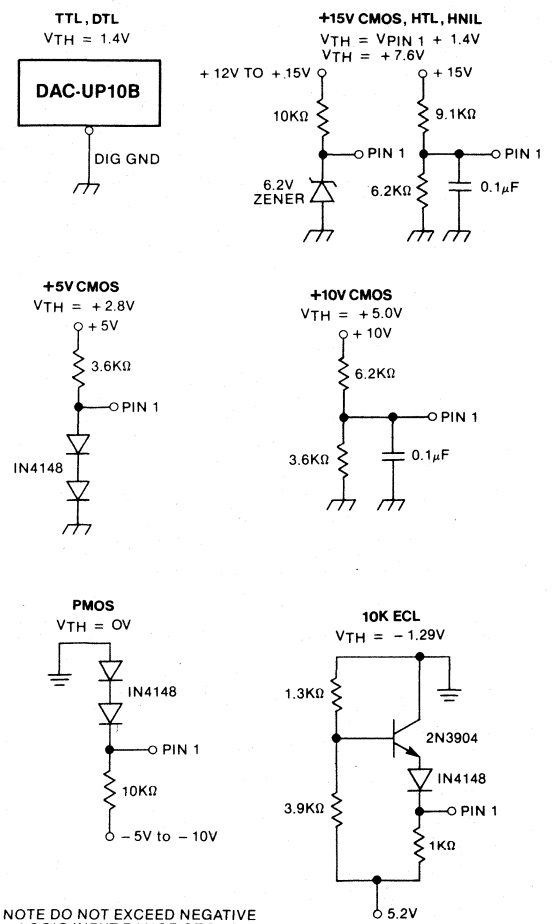


UNIPOLAR OPERATION

CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION TABLE.
2. Apply Logic "0" to $\overline{\text{LOAD}}$ pins (pins 12, 13).
3. Zero and Offset Adjustments
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ potentiometer for zero output voltage.
   For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ potentiometer for negative full scale voltage of –5.000V.
4. GAIN ADJUSTMENT
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust GAIN ADJ potentiometer for the positive full scale voltage of +9.9902V (Unipolar) or +4.9902V (Bipolar).

LOGIC BIAS CIRCUITS



NOTE DO NOT EXCEED NEGATIVE LOGIC INPUT RANGE OF DAC

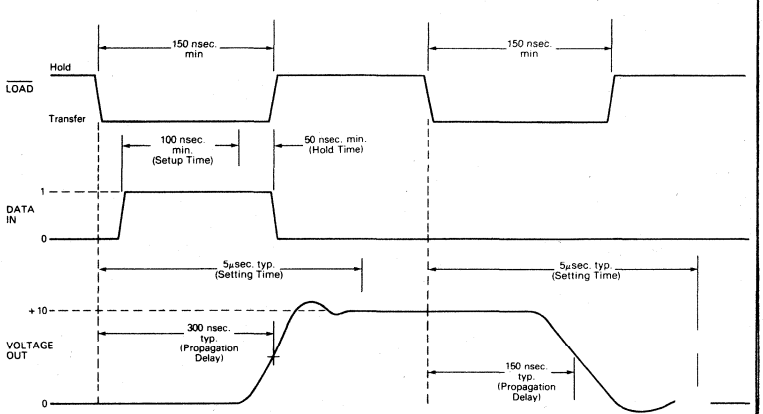
CODING TABLES

INPUT CODE			OUTPUT RANGES	
MSB		LSB	0 to +10V	±5V
1111	11	1111	+9.9902	+4.9902
1110	00	0000	+8.7500	+3.7500
1100	00	0000	+7.5000	+2.5000
1000	00	0000	+5.0000	0.0000
0100	00	0000	+2.5000	–2.5000
0010	00	0000	+1.2500	–3.7500
0000	00	0001	+0.0098	–4.9902
0000	00	0000	0.0000	–5.0000

OUTPUT RANGE SELECTION

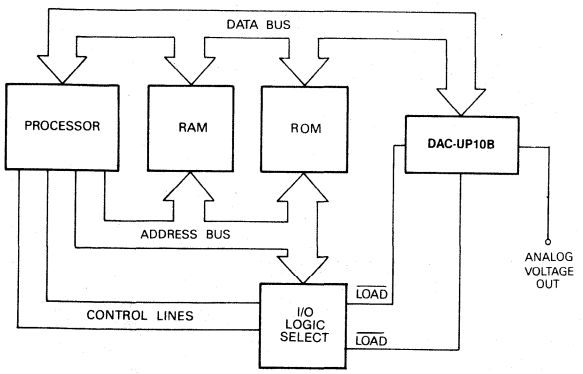
MODE	RANGE	CONNECTION
Unipolar	0 to ±10V	Pin 18 open
Bipolar	±5V	Pin 18 to Pin 20

TIMING DIAGRAM



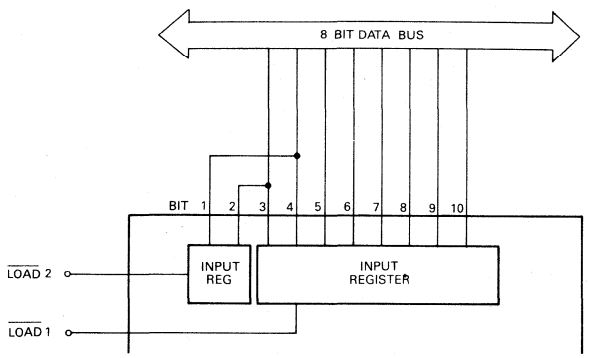
APPLICATIONS

INTERFACING TO A μPROCESSOR



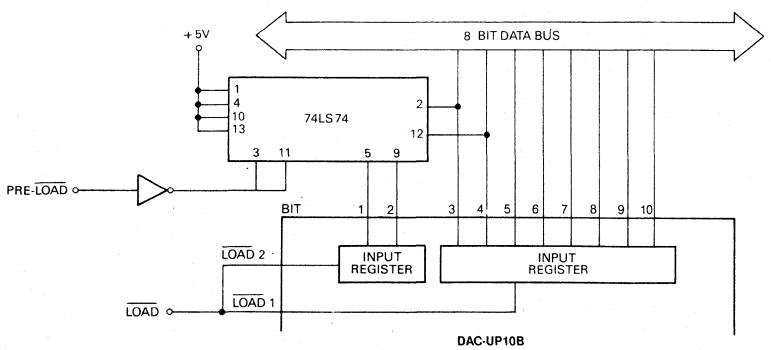
APPLICATIONS
Programmable Power Supplies
Test Equipment
Process and Control
Measurement Instruments
Computer I/O Equipment

INTERFACING TO 8 BIT DATA BUS



NOTE:
The independent $\overline{\text{LOAD}}$ lines allow the DAC-UP10B to be directly interfaced with an 8 bit data bus. Data for the two MSB's is supplied and stored when $\overline{\text{LOAD}}$ 2 is activated low and returned high according to the DAC-UP10B timing requirements. Then $\overline{\text{LOAD}}$1 is activated low and the remaining eight LSB's of data are transferred into the DAC-UP10B. When $\overline{\text{LOAD}}$ 1 returns high, the loading of a ten bit data word from an eight bit data bus is complete.

PRELOADING 2 MSB'S TO PROVIDE SINGLE STEP OUTPUT



NOTE:
Occasionally the analog output must change to its data value within one data address operation. This is no problem when using the DAC-UP10B with a data bus with 10 or more data bits. It can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. After preloading the external latch with the two MSB values, the DAC-UP10B $\overline{\text{LOAD}}$ inputs are activated low and the eight LSB's and two MSB's are concurrently loaded into the DAC-UP10B in one operation.

NEW

DATEL

High Performance, Hybrid 16-Bit Digital To Analog Converters DAC-71, DAC-72

PRELIMINARY

FEATURES

- 16-Bit, 4 Digit Resolution
- ±0.003% Max. Linearity Error
- Current and Voltage Outputs
- ±5 ppm/°C Gain Drift
- Low Cost
- Industry Standard Pin-Out

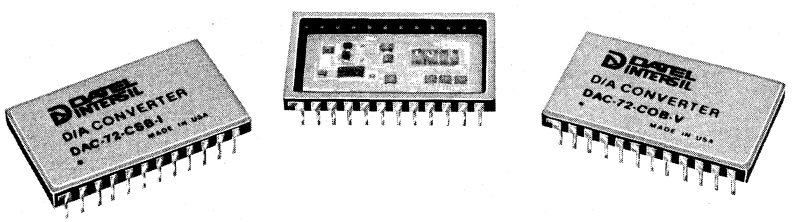
GENERAL DESCRIPTION

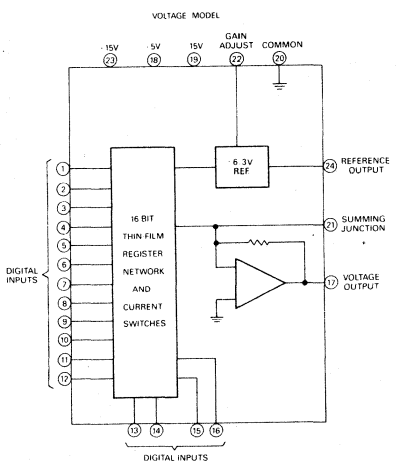
The DAC-71 and DAC-72 are high resolution, low cost hybrid digital to analog converters designed for a broad range of high precision applications involving industrial control and instrumentation. These converters offer 16-bit binary resolution with a maximum linearity error of ±0.003% of FSR and a ±5 ppm/°C maximum gain temperature coefficient.

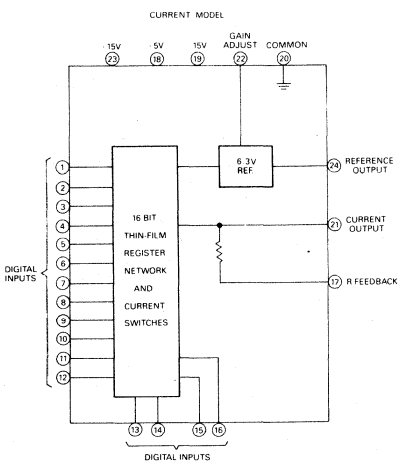
Functionally complete, the DAC-71/72 contain a precision low tempco Zener reference circuit, highly stable thin-film resistor networks, tightly matched quad current switches, and optional output amplifier. Current or voltage output models are available featuring either unipolar or bipolar operation with complementary binary or complementary BCD input coding. All digital inputs are TTL compatible.

Other features include a maximum settling time of only 1 or 10 μsec for current or voltage output models respectively. Total error over the operating temperature range is specified as low as ±0.045% FSR and power supply sensitivity is typically ±0.0001% of FSR/%V supply. The internal +6.3V reference is selected for a maximum temperature coefficient as low as ±5 ppm/°C.

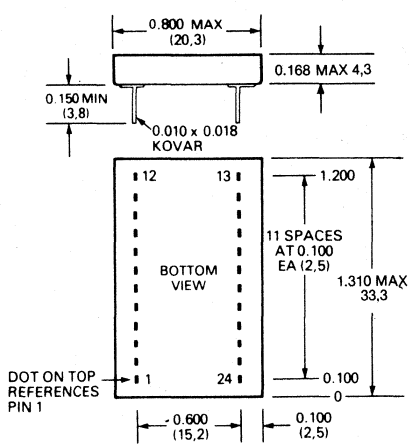
The DAC-71 and DAC-72C are specified for operation over the commercial 0°C to +70°C temperature range, while the DAC-72 operates over the −25°C to +85°C industrial temperature range. All models are packaged in a 24 pin ceramic DIP.







MECHANICAL DIMENSIONS INCHES (MM) 24-PIN CERAMIC



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	BIT 13 IN
2	BIT 2 IN	14	BIT 14 IN
3	BIT 3 IN	15	BIT 15 IN
4	BIT 4 IN	16	BIT 16 IN (LSB)
5	BIT 5 IN	17	OUTPUT
6	BIT 6 IN	18	BIPOLAR OFF.
7	BIT 7 IN	19	−15VDC
8	BIT 8 IN	20	GROUND
9	BIT 9 IN	21	SUM. JUNCTION
10	BIT 10 IN	22	GAIN ADJ.
11	BIT 11 IN	23	+15VDC
12	BIT 12 IN	24	REF. OUT

1. I out for current output models
2. R Feedback for current output models

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SPECIFICATIONS, DAC-71/72 SERIES

Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted.

	DAC-71/72C			DAC-72		
	MIN	TYP	MAX	MIN	TYP	MAX
DIGITAL INPUTS						
Resolution, CCD		4 Digits			4 Digits	
CSB, COB		16 Bits			16 Bits	
Logic Levels, TTL Compatible[1]						
Logical "1" @ +40 A	+2.4V		+5.5V	+2.4V		+5.5V
Logical "0" @ −1.6 mA	0V		+0.4V	0V		+0.4V
TRANSFER CHARACTERISTICS						
Linearity Error, CCD			±0.005% of FSR[2]			±0.005% of FSR
CSB, COB			±0.003% of FSR			±0.003% of FSR
Gain Error,[3] Voltage		±0.01%	±0.5%		±0.01%	±0.5%
Current		±0.05%	±0.25%		±0.05%	±0.25%
Offset Error,[3] Voltage, Unipolar		±0.1 mV	±1 mV		±0.1 mV	±1 mV
Bipolar			±2 mV			±2 mV
Current, Unipolar			±1 mV			±1 mV
Bipolar			±5 mV			±5 mV
Monotonicity Temp. Range (14 Bits)	0°C		+50°C	0°C		+70°C
DRIFT (Over Specified Temp. Range)						
Total Bipolar Drift, Voltage			±15 ppm of FSR/°C		±5 ppm of FSR/°C	±8 ppm of FSR/°C
Current		±15 ppm of FSR/°C	±50 ppm of FSR/°C		±10 ppm of FSR/°C	±40 ppm of FSR/°C
Total Error over Temp. Range[4]						
Voltage, Unipolar		±0.083% of FSR				±0.045% FSR
Bipolar		±0.071% of FSR				±0.05% of FSR
Current, Unipolar			±0.23% of FSR			±0.24% of FSR
Bipolar			±0.23% of FSR			±0.24% of FSR
Gain Drift, Voltage			±15 ppm/°C			±5 ppm/°C
Current			±45 ppm/°C			±35 ppm/°C
Offset Drift, Voltage, Unipolar		±1 ppm of FSR/°C	±2 ppm of FSR/°C		±1 ppm of FSR/°C	±2 ppm of FSR/°C
Bipolar			±10 ppm of FSR/°C			±5 ppm of FSR/°C
Current, Unipolar			±1 ppm of FSR/°C			±1 ppm of FSR/°C
Bipolar			±40 ppm of FSR/°C			±35 ppm of FSR/°C
Differential Linearity over Temperature			±2 ppm of FSR/°C			±1 ppm of FSR/°C
Linearity Error over Temperature			±2 ppm of FSR/°C			±1 ppm of FSR/°C
SETTLING TIME						
Voltage Models (To ±0.003% of FSR)						
Output: 20V Step		5 μsec	10 μsec		5 μsec	10 μsec
1 LSB Step		3 μsec	5 μsec		3 μsec	5 μsec
Slew Rate		20V/μsec			20V/μsec	
Current Models (To ±0.003% of FSR)						
Output: 2 mA Step, 10 to 100 Load			1 μsec			1 μsec
1 k Load			3 μsec			3 μsec
Switching transient		500 mV			500 mV	
ANALOG OUTPUT RANGES:						
Voltage Models						
CSB, CCD		0 to +10V			0 to +10V	
COB		±10V			±10V	
Output Current	±5 mA			±5 mA		
Output Impedance (DC)		0.05Ω			0.05Ω	
Short Circuit Duration		Indefinite to Common			Indefinite to Common	
Current Models						
CSB, CCD		0 to −2 mA			0 to −2 mA	
COB		±1 mA			±1 mA	
Output Impedance, Unipolar		15 kΩ			15 kΩ	
Bipolar		4,4 kΩ			4,4 kΩ	
Compliance			±2.5V		±2.5V	
INTERNAL REFERENCE	6.0 V	6.3 V	6.6 V	6.0 V	6.3 V	6.6 V
Maximum External Current[6]			±5 mA			±5 mA
Temp. Coefficient of Drift			±10 ppm/°C			±5 ppm/°C
POWER SUPPLY SENSITIVITY						
Unipolar Offset, ±15 VDC, +5 VDC		±0.0001% FSR/%V_S			±0.0001% FSR/%V_S	
Bipolar Offset, ±5 VDC		±0.0004% FSR/%V_S			±0.0004% FSR/%V_S	
+5 VDC		±0.0001% FSR/%V_S			±0.0001% FSR/%V_S	
Gain, ±15 VDC		±0.0001% FSR/%V_S			±0.0001% FSR/%V_S	
+5 VDC		±0.0005% FSR/%V_S			±0.0005% FSR/%V_S	
POWER SUPPLY REQUIREMENT						
Voltage	±14.5V, +4.75V	±15 VDC, +5 VDC	±15.5 VDC, +5.25 VDC	±14.5 VDC, +4.75 VDC	±15 VDC, +5 VDC	±15 VDC, +5 VDC
Supply Drain ±15 VDC (no load)		±25 mA	±35 mA		±25 mA	±35 mA
+5 VDC		+20 mA	+30 mA		+20 mA	+30 mA
TEMPERATURE RANGE						
Specification	0°C		+70°C	−25°C	+85°C	
Operating (double above drift specs)	−25°C		+85°C	±55°C		+100°C
Storage	−55°C		+150°C	−55°C		+150°C

NOTES:
1. Adding external CMOS hex buffers CD4009A will provide 15 VDC CMOS input compatibility.
2. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
3. Adjustable to zero with external trim potentiometer.
4. With gain and offset errors adjusted to zero at +25°C.
5. LSB is for 14 bit resolution.
6. Maximum with no degradation of specifications.

Military and Industrial 12 Bit D/A Converters DAC-85, DAC-87

FEATURES

- **DAC-87: Military Version**
- **DAC-85: Industrial Version**
- **MIL-STD-883 Versions Available**
- **Hermetically Sealed**
- **High Performance Design**
- **Industry Standard Pin-Out**

GENERAL DESCRIPTION

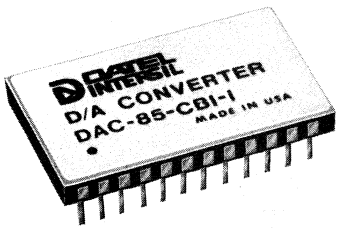
Datel Intersil's DAC-85/87 series are high performance, hybrid 12 bit binary and 3 digit BCD digital-to-analog converters. Pin compatible with standard DAC85/87 converters, these devices offer significantly improved performance.

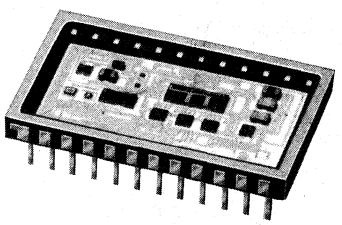
The DAC-87 is specified for operation over the full military operating temperature range of −55°C to +125°C. Versions of this model, screened to MIL STD-883, class B by Datel-Intersil's stringent QL-Program, are available. The DAC-85 is the same converter specified over the commercial, 0 to +70°C, and industrial, −25°C to +85°C, temperature ranges.

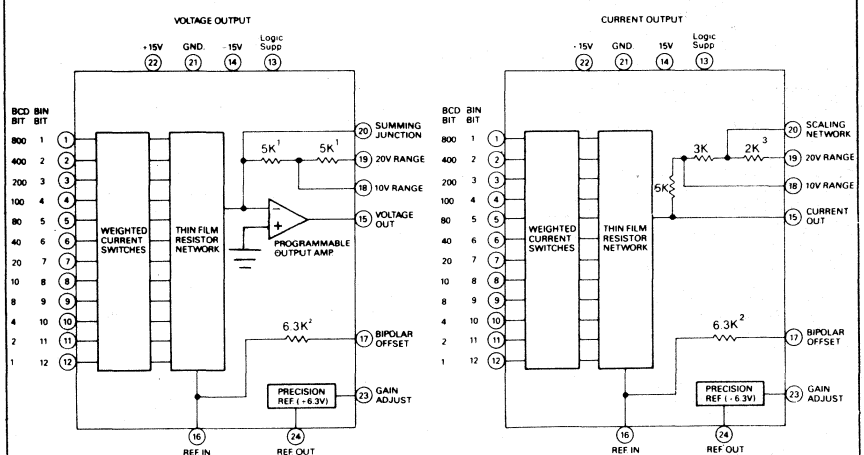
The DAC-85/87 series are complete, self contained units, including a precision internal reference and, on voltage output models, a fast settling output operational amplifier. Active laser trimming of highly stable thin-film resistor networks precisely sets the binary weights of the quad current switches. The excellent tracking of the thin-film resistors in conjunction with the tightly matched current switches results in a differential nonlinearity tempco of only 2 ppm/°C. Other temperature drift specifications include a gain tempco of ±20 ppm/°C max, and a zero tempco of ±5 ppm/°C of FSR max.

The digital inputs of the DAC-85/87 family are both TTL and CMOS compatible, their low input current, 10 μA, permitting them to be connected directly to CMOS logic. Input coding is complementary binary or complementary BCD. On voltage output models, five pin-programmable output ranges are available; 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V with unipolar ranges available on BCD models. Current output versions have pin programmable output ranges of 0 to −2mA or ±1mA with 0 to −1.25 mA for BCD models.

These converters are packaged in a hermetically sealed 24 pin Ceramic Package.

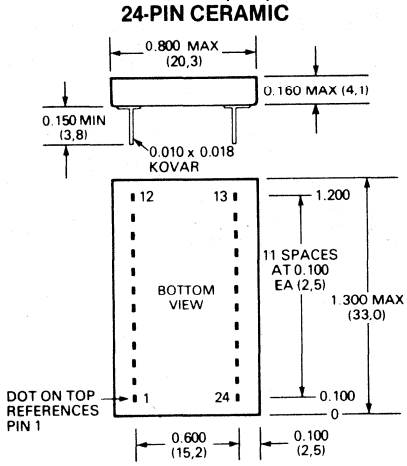






1 FOR BCD MODEL — THESE RESISTORS ARE 4KΩ
2 FOR BCD MODEL — THIS RESISTOR IS OPEN CIRCUIT
3 FOR BCD MODEL — THIS RESISTOR SHORTED (0Ω) PIN 20 HAS NO INTERNAL CONNECTION

MECHANICAL DIMENSIONS INCHES (MM) 24-PIN CERAMIC



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN	13	LOGIC SUPP
2	BIT 2 IN	14	-15VDC
3	BIT 3 IN	15	OUTPUT
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	BIPOLAR OFF.
6	BIT 6 IN	18	10V RANGE
7	BIT 7 IN	19	20V RANGE
8	BIT 8 IN	20*	SUMMING JUNCT.
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15VDC
11	BIT 11 IN	23	GAIN ADJ.
12	BIT 12 IN	24	REF. OUT

*Scaling network on current output models

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SPECIFICATIONS, DAC-85, DAC-87 SERIES

(Typical at +25°C. ± 15 VDC and +5 VDC supplies, unless otherwise noted)

	DAC-85/87 (Binary)	DAC-85/87 (BCD)
MAXIMUM RATINGS		
Supply Voltage (Pins 14,22)	± 18V	
Logic Supply (Pin 13)	± 18V	
Digital Input Voltage	Logic Supp. + 0.5V to − 3V	
INPUTS		
Resolution	12 Binary Bits	3 BCD Digits
Coding, unipolar output	Comp. Binary	Comp. BCD
bipolar output	Comp. Offset Bin.	—
Input Logic Level, bit ON("0")	0V to + 0.8V @ − 1μA	*
bit OFF ("1")	+2.0V to +5.5V @ + 10μA	*
OUTPUTS		
Voltage Models:		
Output Ranges, unipolar	0 to +5V	0 to +2.5V
	0 to +10V	0 to + 5V
		0 to + 10V
Output Ranges, bipolar	±2.5V	—
	±5V	—
	±10V	—
Output current, min.	±5mA	*
Output Impedance	.05Ω	*
Current Models		
Output Range, unipolar	0 to −2mA, ± 10%	0 to −1.25mA, ± 10%
bipolar	± 1mA, ± 10%	—
Voltage Compliance	± 2.5V	*
Output Impedence, unipolar	15KΩ	*
bipolar	4.4KΩ	—
PERFORMANCE		
Nonlinearity, max.	± ½LSB	± ¼LSB
Differential Nonlinearity, max.	± ½LSB	± ¼LSB
Gain Error, before trimming	± 0.1% of FSR[1]	*
Zero Error, before trimming	± 0.1% of FSR[1]	*
Gain Tempco, unipolar max.	± 20 ppm/°C	*
Zero Tempco, unipolar max.	± 5 ppm/°C of FSR[1]	*
Offset Tempco, bipolar max.	± 10 ppm/°C of FSR[1]	*
Diff. Nonlinearity Tempco	± 2 ppm/°C of FSR[1]	*
Monotonicity	Over Operating Temp. Range	*
Power Supply Rejection	± .004% FSR[1]/% supply	*
SETTLING TIME (to ½LSB)		
Voltage Models		
R_F = 2.5 or 5KΩ[2]	3μsec	*
R_F = 10KΩ[3]	4μsec	*
Slew Rate	20V/μsec	*
Current Models		
R_L = 10 to 100Ω	300 nsec	*
R_L = 1KΩ	1μsec	*
POWER REQUIREMENT		
Analog Supply, Pin 22	+ 15V ± 0.5V @ 20 mA max.	
Pin 14	− 15V ± 0.5V @ 40 mA max.	
Logic Supply, Pin 13[4]	+ 5V ± 0.25V @ 25 mA max.	
Power Dissipation	770 mW	
PHYSICAL ENVIRONMENTAL		
Operating Temp. Range, DAC-85C	0 to + 70°C	
DAC-85...	− 25 to + 85°C	
DAC-87...	− 55 to +125°C	
Storage Temperature Range	− 65 to +150°C	
Package Type	Hermetically Sealed 24 Pin Ceramic	
Pins	Gold Plated Kovar, 0.010 x 0.018 inches	
Weight	0.22 oz. (63 g.)	

NOTES

1. FSR is Full Scale range.
2. On BCD models R_F = 2KΩ or 4KΩ.
3. On BCD Models R_F = 8KΩ.
4. The Logic Supply may be operated between +5V and +15V.

*Specifications same as first column

TECHNICAL NOTES

1. Due to their low input current, DAC-85/87 inputs can be connected directly to CMOS logic. When connected in this manner, the Logic Supp. Pin (Pin 13) of the DAC-85/87 should be connected directly to Logic Supp. of the CMOS system. It is permissible to operate the DAC-85/87 with the Logic Supp. between +5V and +15V; with the Logic Supp. operating at voltage levels above +5V, however, there will be an increase in power consumption.
2. These converters must be operated with local supply bypass capacitors from +15V to ground and −15V to ground. Tantalum type capacitors of 1 μF are recommended and should be mounted as close as possible to the converter. If the converters are used in a high frequency noise environment a .01μF ceramic capacitor should put in parallel with each tantalum capacitor. The logic supply does not require a bypass capacitor.
3. The case-to-ambient thermal resistance for these converters is approximately 30°C per watt. For operation at elevated temperatures, it is recommended that care be taken to insure good thermal contact between the case bottom and the circuit board ground plane and that a sufficient air flow surrounds the converter.
4. The DAC-85/87 series converters are designed and factory calibrated to give ± ½ LSB linearity (binary version) and ± ¼ LSB linearity (BCD version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be ± ½ LSB (± ¼ LSB, BCD) everywhere over the full output range without any additional adjustments to achieve a best straight line fit. The linearity specification is therefore a conservative one since the user does not have to make more complicated adjustments for a best straight line fit.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
Binary Coding		
DAC-85C-CBI-I	0°C to + 70°C	
DAC-85C-CBI-V	0°C to + 70°C	
DAC-85-CBI-I	− 25°C to + 85°C	
DAC-85-CBI-V	− 25°C to + 85°C	
DAC-87-CBI-I	− 55°C to + 125°C	
DAC-87-CBI-V	− 55°C to + 125°C	
BCD CODING		
DAC-85C-CCD-I	0°C to + 70°C	
DAC-85C-CCD-V	0°C to + 70°C	
DAC-85-CCD-I	− 25°C to + 85°C	
DAC-85-CCD-V	− 25°C to + 85°C	
DAC-87-CCD-I	− 55°C to + 125°C	
DAC-87-CCD-V	− 55°C to + 125°C	

MATING SOCKET DILS-3 (24 pin socket)
Trimming Potentiometers: TP10K or TP100K

For High Reliability versions of the DAC-87, screened to MIL-STD-883 Level B, contact factory.

CALIBRATION AND OUTPUT CONNECTIONS

CALIBRATION PROCEDURE

1. Select the desired output range and connect the converter up as shown in the output range selection tables and external connection diagrams shown below.

2. To calibrate refer to the Coding Tables below. Note that complementary coding is used.

3. **Zero and Offset Adjustments:**
For unipolar operation, set all digital inputs to "1" (+2.0V to Logic Supp.) and adjust the ZERO ADJ. potentiometer for zero output voltage or current. For bipolar operation, (binary models only), set all digital inputs to "1" and adjust the ZERO ADJ. potentiometer for the negative full scale (voltage output models) or positive full scale (current output models) output value shown in Coding Table.

4. **Gain Adjustment:**
For the binary model, set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ. potentiometer for the positive full scale (voltage output models) or negative full scale (current output models) output value shown in coding table. For the BCD model (unipolar only) set each BCD digit to 0110 and adjust GAIN ADJ. potentiometer for the positive full scale (voltage output models) or negative full scale (current output models) output value shown in Coding Table.

OUTPUT RANGES — VOLTAGE OUTPUT MODELS

OUTPUT RANGE	DIGITAL INPUT CODE	CONNECT PIN 15 TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO	CONNECT PIN 16 TO
± 10V	Comp. Off. Bin.[1]	19	20	15	24
± 5V	Comp. Off. Bin.[1]	18	20	N.C.	24
± 2.5V	Comp. Off. Bin.[1]	18	20	20	24
+10V	Comp. Bin.	18	21	N.C.	24
+10V	BCD	19	N.C.	15	24
+5V	Comp. Bin.	18	21	20	24
+5V	BCD	18	N.C.	N.C.	24
+2.5V	BCD	18	N.C.	20	24

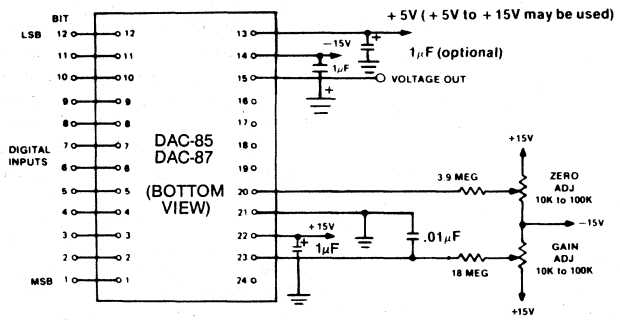
OUTPUT RANGES — CURRENT OUTPUT MODELS[2]

OUTPUT RANGE	DIGITAL INPUT CODE	CONNECT A[3] TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO	CONNECT PIN 16 TO
± 10V	Comp. Off. Bin.[1]	19	15	A	24
± 5V	Comp. Off. Bin.[1]	18	15	N.C.	24
± 2.5V	Comp. Off. Bin.[1]	18	15	15	24
+10V	Comp. Bin.	18	21	15	24
+10V	BCD	19	N.C.	A	24
+5V	Comp. Bin.	18	21	15	24
+5V	BCD	18	N.C.	N.C.	24
+2.5V	BCD	18	N.C.	15	24

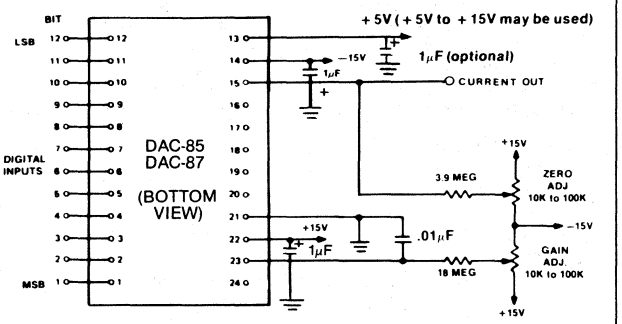
1. For Comp. Two's complement coding invert the MSB of the comp. offset Bin Code with an external inverter.
2. Using external op. amp. and internal feedback resistors.
3. "A" is the output of the external output op. amp. being used.

EXTERNAL ADJUSTMENT AND VOLTAGE SUPPLY CONNECTION DIAGRAMS

VOLTAGE OUTPUT



CURRENT OUTPUT



CODING TABLES

UNIPOLAR OUTPUT – COMPLEMENTARY BINARY

BINARY INPUT CODE MSB LSB	UNIPOLAR OUTPUT RANGES 0 TO +10V	0 TO +5V	0 TO -2MA
0000 0000 0000	+9.9976V	+4.9988V	-1.9995MA
0011 1111 1111	+7.5000	+3.7500	-1.5000
0111 1111 1111	+5.0000	+2.5000	-1.0000
1011 1111 1111	+2.5000	+1.2500	-0.5000
1111 1111 1110	+0.0024	+0.0012	-0.0005
1111 1111 1111	0.0000	0.0000	0.0000

UNIPOLAR OUTPUT – COMPLEMENTARY BCD

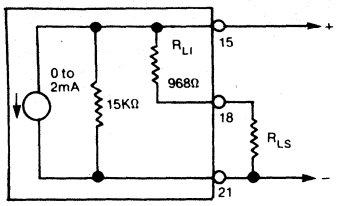
BCD INPUT CODE MSD LSD	UNIPOLAR OUTPUT RANGES 0 TO +10V	0 TO +5V	0 TO +2.5V	0 TO -1.25MA
0110 0110 0110	+9.990V	+4.995V	+2.498V	-1.2488MA
1000 1010 1111	+7.500	+3.750	+1.875	-0.9375
1010 1111 1111	+5.000	+2.500	+1.250	-0.6250
1101 1010 1111	+2.5000	+1.250	+0.625	-0.3125
1111 1111 1110	+0.0100	+0.005	+0.003	-0.0013
1111 1111 1111	0.0000	0.000	0.000	0.0000

BIPOLAR OUTPUT – COMPLEMENTARY OFFSET BINARY

INPUT CODE MSB LSB	BIPOLAR OUTPUT RANGES ±10V	±5V	±2.5V	±1MA
0000 0000 0000	+9.9951V	+4.9976V	+2.4988V	-0.9995MA
0011 1111 1111	+5.0000	+2.5000	+1.2500	-0.5000
0111 1111 1111	0.0000	0.0000	0.0000	0.0000
1011 1111 1111	-5.0000	-2.5000	-1.2500	+0.5000
1111 1111 1110	-9.9951	-4.9976	-2.4988	+0.9995
1111 1111 1111	-10.0000	-5.0000	-2.5000	+1.0000

DRIVING A RESISTIVE LOAD

EQUIVALENT CURRENT MODE OUTPUT CIRCUIT



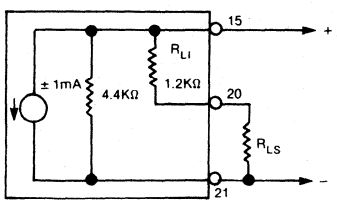
UNIPOLAR OPERATION

$R_L = R_{LI} + R_{LS}$

$V_{out} = -2mA \left(\frac{15K\Omega \times R_L}{15K\Omega + R_L} \right)$

R_L max. = 1.36K

V_{out} max. = −2.5V



BIPOLAR OPERATION

$R_L = R_{LI} + R_{LS}$

$V_{out} = \pm 1mA \left(\frac{4.4K\Omega \times R_L}{4.4K\Omega + R_L} \right)$

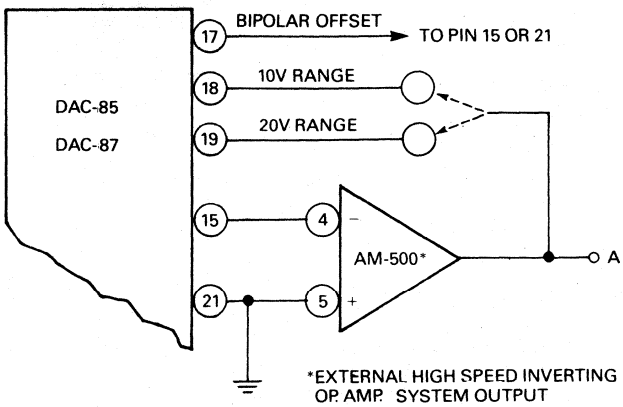
R_L max. = 5.72KΩ

V_{out} max. = ±2.5V

NOTE:
External Resistor R_{LS} is required to produce output ranges of 0 to −2V or ±1V. To maintain output specifications, use metal film resistors with a TCR of ±100 ppm/°C or less.

EXTERNAL OP. AMP CONNECTION

USING INTERNAL FEED BACK RESISTORS



*EXTERNAL HIGH SPEED INVERTING OP AMP. SYSTEM OUTPUT SETTLES IN LESS THAN 1.0 μSEC

MIL-STD-883B PROCESSING QL PROGRAM

Military and Aerospace programs require high reliability devices subjected to rigorous screening procedures. To meet this need, Datel-Intersil has developed its QL program, a high level of screening, strictly in accordance with MIL-STD-883, method 5008, class B. All devices in this program are hermetically sealed and designated with the suffix "QL". The DAC-87 is available with 100% screening to Datel-Intersil's QL program. The following chart briefly summarizes the test procedures followed by the QL program in conformance with MIL-STD-883B.

TEST	METHOD	PURPOSE
HIGH TEMPERATURE STORAGE	Method 1008, Test condition C, 24 hrs @ +150°C	Eliminates device failure due to storage at elevated temperatures.
INTERNAL VISUAL (PRECAP)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical or thermal stress.
SEAL, FINE AND GROSS	Method 1014, test condition A (fine), 5×10^{-7} cc/sec., test condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
THERMAL SHOCK[1]	Method 5011, test condition A, 15 cycles @ 0°C to +100°C.	Determines resistance of device to sudden exposure to extreme temperate changes. Removes potential failures due to thermal stress on bonds, etc.
TEMPERATURE CYCLING	Method 1010, test condition C, −65°C to +150°C	
CONSTANT ACCELERATION	Method 2001, test condition A, Y_1 AXIS, 5 Kg.	Eliminates potential failures due to structural or mechanical weaknesses not detected in shock or vibration tests.
BURN-IN TEST	Method 1015, test condition B, 160 hrs @ +125°C.	Stresses device at or above maximum rated operating temperature in order to eliminate infant mortality failures.
FINAL ELECTRICAL TESTS	Performed at +25°C, and at maximum & minimum operating temperatures.	Verifies that device still meets specified data sheet parameters.
EXTERNAL VISUAL	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

1. Per MIL-STD-883B, Thermal shock may be substituted for temperature cycling.

NEW

DATEL

Monolithic, High Performance 12 Bit D/A Converter DAC-562

FEATURES

- 12 Bit Resolution
- 300 nsec. Settling Time
- ± 10 ppm/°C Max. Tempco
- 5 Output Ranges
- ±¼ LSB Linearity
- 562 Pin Compatibility

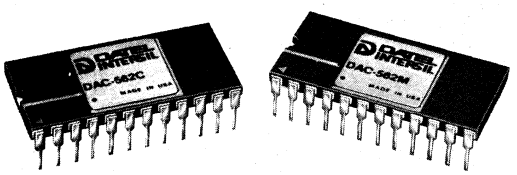
GENERAL DESCRIPTION

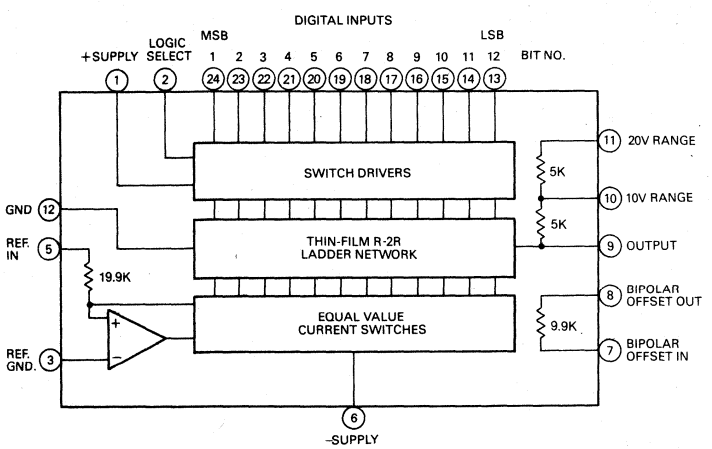
The DAC-562 is a new high performance monolithic 12 bit D/A converter fabricated with advanced bipolar technology. The circuit uses a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources to achieve ¼ LSB typical linearity, 300 nsec. settling time, and ± 10 ppm/°C max. gain tempco.

The DAC-562 operates from TTL or CMOS input logic and provides a 0 to 2 mA or ± 1 mA output current. The converter contains tracking feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to + 5V, 0 to + 10V, ± 2.5, ± 5V, and ± 10V. Since these resistors closely track the R-2R ladder with temperature, gain stability of better than 10 ppm/°C is achieved. Differential linearity error is ¼ LSB typical and ½ LSB maximum, with output monotonicity guaranteed over the operating temperature range.

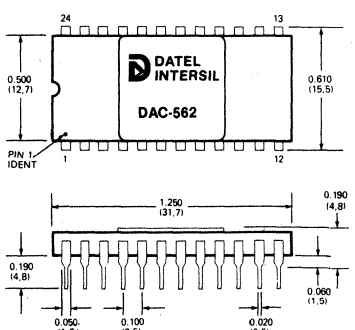
Output settling time for a full scale change to ½ LSB is 300 nsec. typical and 400 nsec. maximum.

The DAC-562 is completely pin and function compatible with industry standard 562 D/A converters. The package is a 24 pin hermetically sealed ceramic DIP; power requirement is + 5V to + 15V and − 15 VDC. There are two basic models: DAC-562C operates over 0°C to 70°C while DAC-562M operates over − 55°C to + 125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+ SUPPLY	13	BIT 12 IN (LSB)
2	LOGIC SELECT	14	BIT 11 IN
3	REF. GROUND	15	BIT 10 IN
4	N.C.	16	BIT 9 IN
5	REFERENCE IN	17	BIT 8 IN
6	− SUPPLY	18	BIT 7 IN
7	BIP. OFF IN	19	BIT 6 IN
8	BIP. OFF OUT	20	BIT 5 IN
9	OUTPUT	21	BIT 4 IN
10	10V RANGE	22	BIT 3 IN
11	20V RANGE	23	BIT 2 IN
12	GROUND	24	BIT 1 IN (MSB)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-562

Typical at 25°C, +5V & −15V Supplies, +10V Reference unless otherwise noted.

	DAC-562C	DAC-562M
MAXIMUM RATINGS		
Positive Supply, pin 1	+20V	*
Negative Supply, pin 6	−20V	*
Reference Input, pin 5	±Supply	*
Reference Ground, pin 3	0V	*
Digital Inputs, pins 13-24	−1V to +12V	*
Logic Select Input, pin 2	−1V to +12V	*
Output, pin 9	+Supply, −5V	*
Resistors, pins 7, 8, 10, 11	±Supply	*
INPUTS		
Resolution	12 Bits	*
Coding, unipolar output	Straight Binary	*
Coding, bipolar output	Offset Binary	*
Input Logic Level, bit ON ("1")[1]	+2.0 min. @ 100nA max.	*
Input Logic Level, bit OFF ("1")[1]	+0.8V max. @ −100μA max.	
Reference Input Voltage	+10V	*
Reference Input Resistance	20KΩ	*
OUTPUTS		
Output Current, unipolar	0 to −2 mA	*
Output Current, bipolar	±1 mA	*
Output Voltage Ranges, unipolar	0 to +5V	*
	0 to +10V	*
Output Voltage Ranges, bipolar	±2.5V	*
	±5V	*
	±10V	*
Output Voltage Compliance	±1V	*
Output Resistance	2KΩ	*
Output Capacitance	20 pF	*
PERFORMANCE		
Linearity Error, max.	±½ LSB	±¼ LSB
Linearity Error Over Temp., max.	±1 LSB	±1 LSB
Differential Linearity Error, max.	±½ LSB	±¼ LSB
Monotonicity	Over Oper. Temp. Range	*
Gain Error, max.[2]	±0.25%	*
Unipolar Zero Error, max.[2]	±0.05%	*
Bipolar Offset Error, max.[2]	±0.25%	*
Gain Tempco, max.[3]	±10 ppm/°C	*
Zero Tempco, max.[3]	±2 ppm/°C	*
Bipolar Offset Tempco, max.[3]	±4 ppm/°C	*
Settling Time to ½ LSB[4]	300 nsec. typ., 400 nsec. max.	*
Power Supply Sensitivity, max.	±3.5 ppm of FSR/% Supply	*
Reference Slew Rate	6 mA/μsec.	*
Reference Bandwidth	10 MHz	*
POWER REQUIREMENT		
Rated Power Supply Voltage	+5 VDC, −15 VDC	*
Positive Supply Range[5]	+4.75V to +16.5V	*
Negative Supply Range	−15 VDC ±10%	*
Rower Supply Quiescent Current, max.[6]	+15 mA, −23 mA	*
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range	0°C to +70°C	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C	*
Package, Hermetically Sealed	24 pin ceramic DIP	*

*Specifications same as first column

NOTES:

1. + Supply must be +5V ±5% for DAC-562C and +5V ±10% for DAC-562M. For operation with CMOS logic see Technical Note 1.
2. Adjustable to zero using external potentiometers. Specified error is for 100 ohm trim resistors and external op amp using internal feedback resistor.
3. Using external op amp and internal feedback and offset resistor. Zero Tempco and Bipolar Offset Tempco are in ppm/°C of FSR (Full Scale Range)
4. For full scale change: all bits ON-to-OFF, or all bits OFF-to-ON.
5. Maximum Positive Supply Voltage is +16V for high level logic only, i.e. when Pin 2 is tied to Pin 1. SEE Technical Note 1.
6. Allow 30 seconds warm-up time.

TECHNICAL NOTES

1. For TTL input logic, pin 2 should be connected to pin 12 and the + supply must be +5 VDC (±5% for DAC-562C and ±10% for DAC-562M). For CMOS input logic, connect pin 2 to pin 1 and use any + supply voltage from +4.75V to +12 VDC. CMOS threshold levels are then + Vs × 0.7 for bit ON and +Vs × 0.3 for bit OFF. Logic input current is the same as that specified for TTL.
2. Gain and bipolar offset errors are adjustable to zero by means of two 200 ohm trimming pots. The adjustment range is ±0.3% of FSR for gain and ±0.6% of FSR for bipolar offset. The unipolar zero error is adjustable to zero by means of the offset adjustment of the external output amplifier.
3. The output voltage compliance range of ±1V should not be exceeded or else accuracy will be affected. If a resistor load is driven instead of an op amp summing junction then the maximum resistor value is 500 ohms for unipolar operation and 1K ohms for bipolar operation.
4. Output settling time is specified for current output and is measured with a small current sampling resistor to ground (100 ohms). Voltage output settling time depends on the output operational amplifier used. Datel-Intersil's AM-500 is recommended for about 500 nsec. settling and AM-452-2 is recommended for about 1.5 μsec. Settling. Both should be used with a 3-20 pF variable compensating capacitor across the feedback resistor which should be adjusted for optimum settling time.
5. For best high speed performance, both power supplies should be bypassed with 1 μF electrolytics in parallel with 0.01 μF ceramic capacitors as close as possible to the ± supply pins.
6. The gain and bipolar offset temperature coefficients are specified with the internal feedback and offset resistors used in conjunction with an external operational amplifier. This is because these resistors track the R-2R ladder with temperature and therefore the tempco's do not depend on absolute resistor tempco. The tempco of the external +10V reference must also be included in the total converter tempco, however.
7. Because of the DAC-562 circuit which incorporates equally weighted current sources driving an R-2R ladder network, the turn ON and turn OFF times are virtually symmetrical, resulting in low output glitches compared with other DAC's. The major carry glitch typically has an amplitude of 14% of FSR. The time duration to 90% complete is typically 35 nsec.
8. The DAC-562 wideband output noise with all bits ON is typically 100 μV P-P over 0.1 Hz to 5 MHz.

ORDERING INFORMATION

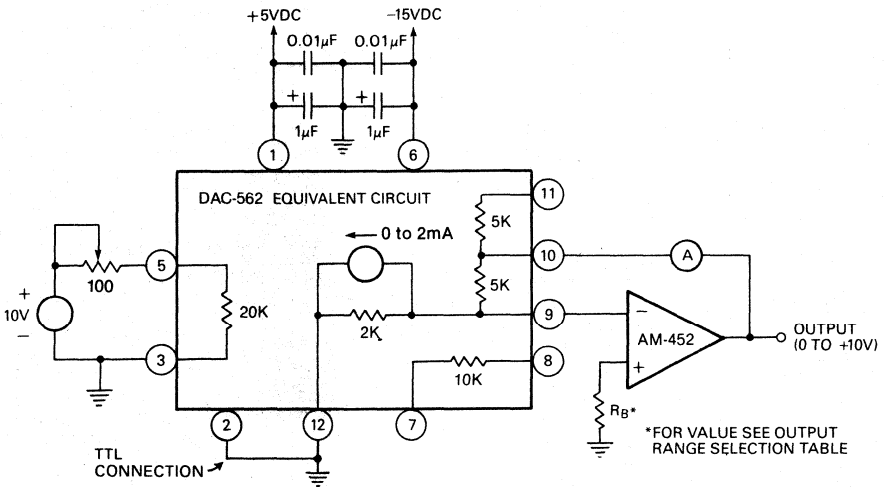
Model	Temp. Range	Price (1-24)
DAC-562C	0 to + 70°C	
DAC-562M	−55 to +125°C	

Trimming Potentiometer: TP50 —

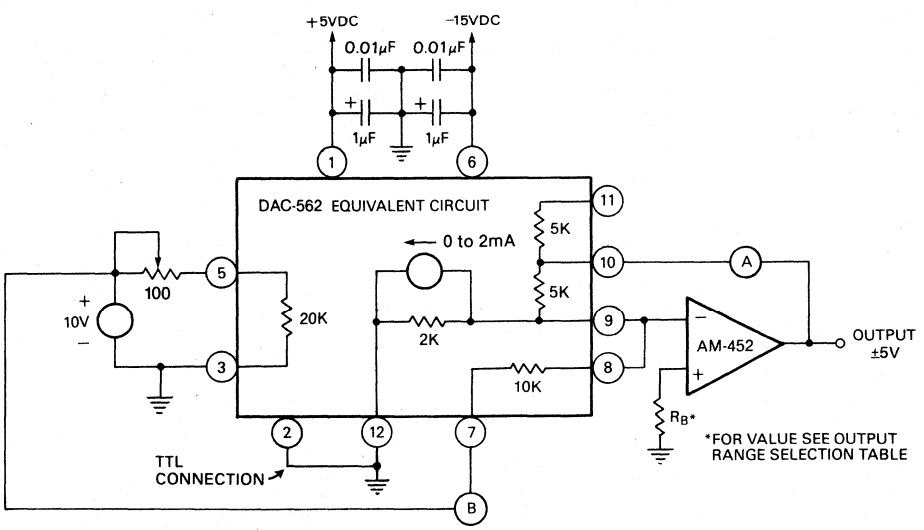
THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

STANDARD CONNECTIONS

UNIPOLAR OPERATION—See Output Range Selection Table



BIPOLAR OPERATION—See Output Range Selection Table



OUTPUT VOLTAGE RANGE SELECTION (See Connection Diagrams Above)

OUTPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER				R_B, BIAS COMP. RESISTOR*
0 to +5V	A & 10	9 & 11			1.11kΩ
0 to +10V	A & 10				1.43kΩ
±2.5V	A & 10	9 & 11	8 & 9	7 & B	1kΩ
±5V	A & 10		8 & 9	7 & B	1.25kΩ
±10V	A & 11		8 & 9	7 & B	1.43kΩ

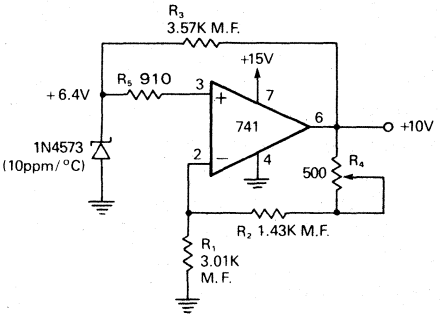
*Carbon composition resistor value used from amplifier + input terminal to ground to compensate for offset due to bias current.

CALIBRATION AND APPLICATION

CODING TABLE—See Calibration Procedure

INPUT CODE	OUTPUT VOLTAGE RANGE				
	0 TO +5V	0 TO +10V	±2.5V	±5V	±10V
1111 1111 1111	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
1100 0000 0000	+3.7500	+7.5000	+1.2500	+2.5000	+5.0000
1000 0000 0000	+2.5000	+5.0000	0.0000	0.0000	0.0000
0100 0000 0000	+1.2500	+2.5000	−1.2500	−2.5000	−5.0000
0000 0000 0001	+0.0012	+0.0024	−2.4988	−4.9976	−9.9951
0000 0000 0000	0.0000	0.0000	−2.5000	−5.0000	−10.0000

+10V REFERENCE CIRCUIT



Adjust R_4 for +10.000V output. For best stability R_1 & R_2 should track each other closely with temperature. R_4 should be a low tempco trimming pot or else a selected metal film trim resistor.

CALIBRATION PROCEDURE

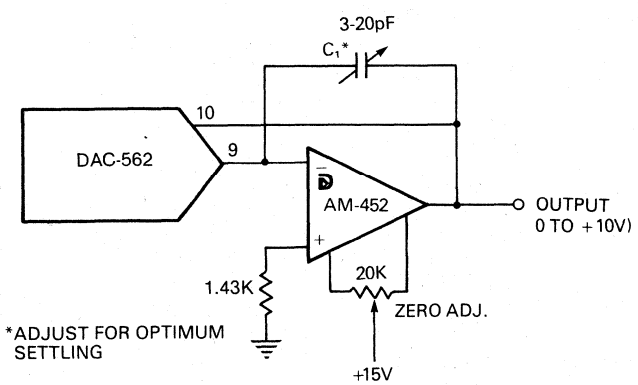
UNIPOLAR OPERATION

1. Set all digital inputs LO. Adjust the output amplifier offset for 0 volts output.
2. Set all digital inputs HI. Adjust Gain trimming pot for an output of +FS-1LSB.
   FS-1LSB = +9.9976V for 0 to +10V range.
   = +4.9988V for 0 to +5V range.

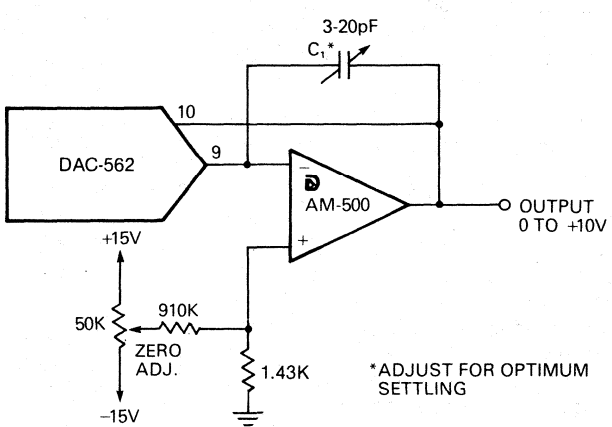
BIPOLAR OPERATION

1. Set all digital inputs LO. Adjust Bipolar Offset trimming pot for one of the following output voltages:
   −2.5V for ±2.5V range
   −5.0V for ±5V range
   −10.0V for ±10V range
2. Set bit 1 (MSB) input HI and all other digital inputs LO. Adjust Gain trimming pot for 0 volts output.

CIRCUIT FOR FAST VOLTAGE OUTPUT (≈1.5 μSEC. SETTLING)



CIRCUIT FOR FAST VOLTAGE OUTPUT (≈0.5 μSEC. SETTLING)



NEW

DATEL

Microprocessor Compatible Double-Buffered D/A Converters DAC-608, DAC-610, DAC-612

FEATURES

- Microprocessor Compatible
- Double-Buffered Inputs
- 8, 10 and 12 Bit Resolution
- 500 nS Settling Time — DAC-610
- 4 Quadrant Multiplication

GENERAL DESCRIPTION

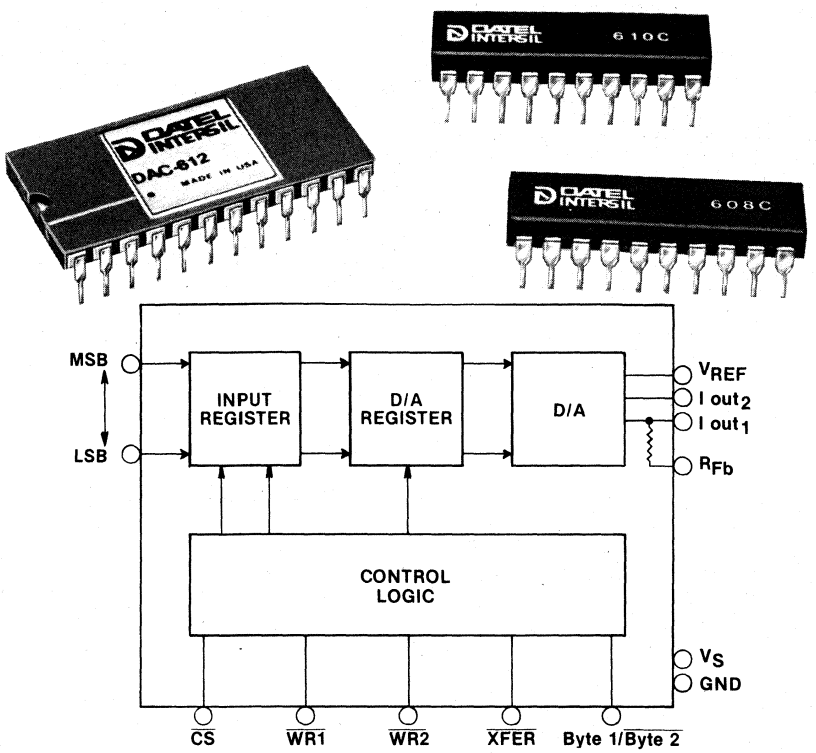
DATEL-INTERSIL's DAC-608, DAC-610 and DAC-612 are low cost monolithic 8, 10 and 12-bit multiplying D/A converters designed to operate directly with most popular microprocessors. Double-buffered inputs allow the converters to output an analog voltage corresponding to one digital word while holding the next, permitting simultaneous updating of multiple D/A's via a common strobe signal. The converters appear as a memory location or I/O port to the microprocessor and thus do not require interfacing logic. All models will operate as normal D/A's for non-microprocessor based applications.

Excellent temperature tracking characteristics are provided by precision silicon-chromium R-2R resistor ladder networks. Output settling time for a full scale change to ½ LSB, is as low as 500 nsec and the maximum linearity error on all models is ± ½ LSB. Monotonicity is guaranteed over the full operating temperature range.

Other features include a low, 3 mV P-P, digital feedthrough error, 30 mW power dissipation and single supply operation. The reference input is selectable over a range of ±10V and may also be used as the analog input for four quadrant multiplication applications.

The DAC-612 is specified for operation over the industrial −25°C to +85°C temperature range and is packaged in a 24 pin ceramic DIP. The DAC-608 and DAC-610 are specified over the commercial 0°C to +70°C temperature range and are packaged in a 20 pin plastic DIP. These devices are an ideal choice for innumerable applications involving industrial process control, programmable attenuators, audio signal processing and low frequency sine wave generation.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.



INPUT/OUTPUT CONNECTIONS

DAC-608

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR1}$ (WRITE 1)
3	ANALOG GROUND
4	DI3
5	DI2
6	DI1
7	DI0 (LSB)
8	REFERENCE IN
9	FEEDBACK
10	DIGITAL GROUND
11	OUTPUT 1
12	OUTPUT 2
13	DI7 (MSB)
14	DI6
15	DI5
16	DI4
17	$\overline{XFER}$ (Trans. Contl.)
18	$\overline{WR2}$ (Write 2)
19	ILE (In. Latch ENB)
20	V_S

DAC-610

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR}$ (WRITE)
3	BYTE 1/$\overline{BYTE\ 2}$
4	$\overline{XFER}$ (Trans. Contl.)
5	DI5
6	DI6
7	DI7
8	DI8
9	DI9 (MSB)
10	GROUND
11	OUTPUT 2
12	OUTPUT 1
13	REFERENCE IN
14	FEEDBACK
15	DI0 (LSB)
16	DI1
17	DI2
18	DI3
19	DI4
20	V_S

DAC-612

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR1}$ (Write 1)
3	ANALOG GROUND
4	DI5
5	DI4
6	DI3
7	DI2
8	DI1
9	DI0 (LSB)
10	REFERENCE IN
11	FEEDBACK
12	DIGITAL GROUND
13	OUTPUT 1
14	OUTPUT 2
15	DI11 (MSB)
16	DI10
17	DI9
18	DI8
19	DI7
20	DI6
21	$\overline{XFER}$ (Trans. Contl.)
22	$\overline{WR2}$ (Write 2)
23	BYTE 1/$\overline{BYTE\ 2}$
24	V_S

DATEL-INTERSIL, 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL., (617) 339-9341/ TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-608/610/612

Typical @ 25°C, 15V Supply, Ref. In = +10V unless otherwise noted.

	DAC-608	DAC-610	DAC-612
MAXIMUM RATINGS			
Power Supply Voltage	+17 VDC		
Logic Input Voltage	V_S to GND.		
Reference Input Voltage	±25V		
Output Voltage	V_S to 100 mV		
Package Dissipation	500 mW		
INPUTS			
Resolution	8 bits	10 bits	12 bits
Coding, Unipolar operation	Straight Binary		
Bipolar operation	Offset Binary		
Input Logic Level, bit ON ("1")	+2V min. @ +10 µA max.		
Input Logic Level, bit OFF ("0")	+0.8V max. @ −200 µA max.		
$\overline{CS}$ (Chip Select)	Active low state in combination with ILE enables the D/A for Write 1 operation. Minimum pulse duration is 320 nS. $\overline{CS}$ must remain low an additional 10 nS after Write Pulse returns high.		
ILE (Input Latch Enable)[1]	Active high state in combination with $\overline{CS}$ enables the D/A for Wr ɜ 1 operation. Minimum Pulse duration is 320 nS. ILE must remain high an additional 10 nS after Write Pulse returns high.		
$\overline{WR1}$ (Write 1)	Active low state is used to load the digital data bits into the input latch. A high ON $\overline{WR1}$, and a high on ILE will update the input latch. Minimum Pulse duration is 320 nS.		
$\overline{WR2}$ (Write 2)	Active low in combination with $\overline{XFER}$ transfers available data in the input latch to the D/A register. The data in the D/A register is latched when $\overline{WR2}$ is high. Minimum Pulse Duration is 320 nS.		
Byte 1/$\overline{Byte\ 2}$ (Byte Sequence Control)[2]	All locations of the input latch are enabled when this control is high. When low, only least significant bits are enabled. Pulse Duration is 320 nS.		
$\overline{XFER}$ (Transfer Control Signal)	Active low in combination with $\overline{WR2}$, will transfer the data available in the input latch to the D/A register.		
OUTPUTS			
Output Capacitance, Output 1[3]	70 pF	60 pF	70 pF
Output 2[3]	200 pF	250 pF	200 pF
Output 1[4]	200 pF	250 pF	200 pF
Output 2[4]	70 pF	60 pF	70 pF
Output 1, Current Range[5]	$\left(\frac{V_{REF}}{15k\Omega}\right)\left(\frac{D}{256}\right)$	$\left(\frac{V_{REF}}{15k\Omega}\right)\left(\frac{D}{1024}\right)$	$\left(\frac{V_{REF}}{15k\Omega}\right)\left(\frac{D}{4096}\right)$
Output 2, Current Range[5]	$\left(\frac{V_{REF}}{15k\Omega}\right)\left(\frac{256-D}{256}\right)$	$\left(\frac{V_{REF}}{15k\Omega}\right)\left(\frac{1024-D}{1024}\right)$	$\left(\frac{V_{REF}}{15k\Omega}\right)\left(\frac{4096-D}{4096}\right)$
Feedthrough Error[3]	3 mV P-P	90 mV P-P	3 mV P-P
PERFORMANCE			
Linearity Error Max.	± ½ LSB		
Differential Linearity Error Max.	± ½ LSB		
Monotonicity	Over operating temperature range		
Gain Error[6]	Adjustable to Zero		
Zero Error[6]	Adjustable to Zero		
Gain Tempco Max.	±6 PPM/°C	±10 PPM/°C	±6 PPM/°C
Settling Time, Full Scale change to ± ½ LSB	1 µsec	500 nsec	1 µsec
Power Supply Rejection[4]	±2 PPM/V	±30 PPM/V	±3 PPM/V
POWER REQUIREMENT			
Rated Power Supply Voltage	+15 VDC		
Power Supply Voltage Range	+4.7 VDC to +15.75 VDC		
Supply Current Max.	2 mA		
PHYSICAL-ENVIRONMENTAL			
Operating Temp. Range DAC-608/610	0°C to 70°C		
DAC-612	−25°C to +85°C		
Storage Temperature Range	−65°C to +150°C		
Package Type: DAC-608/610	20 pin plastic DIP		
DAC-612	24 pin ceramic DIP		

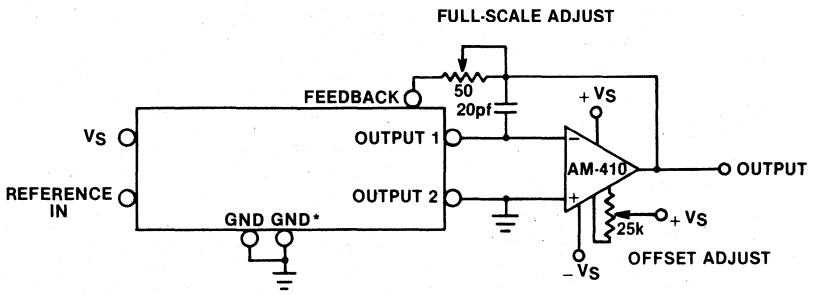
NOTES:
1. DAC-608 only.
2. DAC-610/612 only.
3. All data inputs latched low. To achieve this low feedthrough on the DAC-612, the metal lid must be grounded. If the lid is left floating the feedthrough is typically 6 mV.
4. All data inputs latched high.
5. "D" stands for digital input.
6. Using internal feedback resistor.

TECHNICAL NOTES

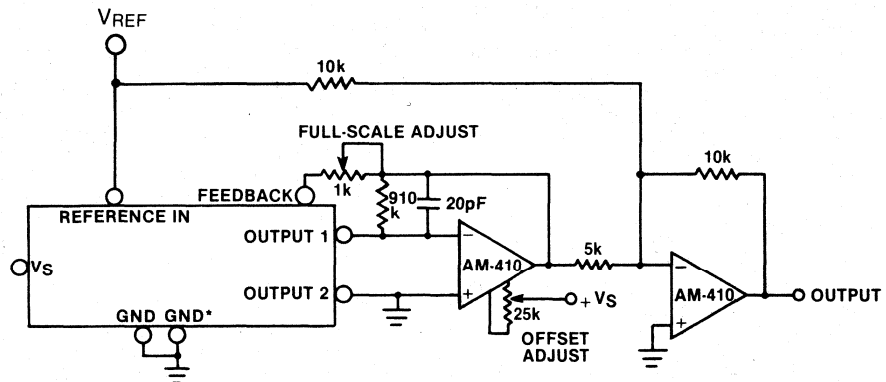
1. The output op amp to be used, should have as low a value of input bias current as possible. DATEL-INTERSIL'S AM-410 op amps are highly recommended for use with these devices.
   In order to maintain the specified temperature tracking specifications, the D/A's internal feedback resistor should be used in the op amp feedback loop.
2. The voltage at the current outputs must be as close to ground potential as possible so that the changes in the applied digital codes do not affect the output current linearity.
3. In fast data acquisition applications, the addition of a 10 to 22 pF capacitor (Cc) in parallel with the feedback resistor of the op amp may be required to minimize overshoot and ringing at the output.
4. Due to the rapid switching of internal logic gates that respond to the input changes, a narrow spike could flow out from the current output terminals. In order to minimize this effect, the input register must always be used as the data latch. Reducing V_S from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, however, this causes a loss of internal switching speed. Also, increasing capacitor Cc (if being used) to a value consistent with the actual circuit bandwidth requirements, can provide a substantial damping effect on any output spikes.
5. For flow through operation, (operation with the buffers continuously enabled) $\overline{CS}$, $\overline{WR1}$, $\overline{WR2}$ and $\overline{XFER}$ must be tied to ground and Byte 1/$\overline{Byte\ 2}$ (ILE for DAC-608) must be high. This will allow both internal registers to follow the applied digital inputs, directly affecting the device output.
6. For stand alone operation where control signals are generated by discrete logic, double buffering can be controlled by applying a logic "0" to $\overline{CS}$ and $\overline{XFER}$ and a logic "1" to ILE and pulling $\overline{WR1}$ low to load data in the input latch. Pulling $\overline{WR2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.
7. All unused digital inputs should be tied to V_S or ground in order to prevent damage to the chip from static discharge. If any of the digital inputs are inadvertently left floating, the D/A will interpret the pin as a logic "1".
8. The input registers of the DAC-610 and DAC-612 are arranged to accept a left justified data word from the microprocessor with 8 bits coming first and the lower bits second. Left justified means that the binary point is assumed to be located to the left of the most significant bit.
9. The use of good circuit board layout techniques are required for rated performance. Minimization of lead lengths around analog circuitry is recommended. It is important that a good ground be used. A single point ground distribution technique for analog signals and supply returns will prevent other devices in the system from affecting the output of the D/A's. V_S should be bypassed as close to the V_S pin as possible with a low inductance 1 µF tantalum capacitor.

CODING AND CALIBRATION

CALIBRATION PROCEDURE



UNIPOLAR CONFIGURATION



BIPOLAR CONFIGURATION

*ONE GROUND ON DAC-610

UNIPOLAR

Zero Adjust — Set all data bits to logic "0" (logic "1" if using output 2) and adjust the OFFSET ADJUST pot on the external OP Amp for 0.000V.

Full Scale — Set all data bits to logic "1" (logic "0" if using output 2) and set the FULL Scale ADJUST for an output equal to: Vout = −Vref (N-1)/N, where "N" is equal to: 256 (DAC-608), 1024 (DAC-610) or 4096 (DAC-612).

BIPOLAR

Zero Adjust — Set all data bits to logic "0" and adjust the OFFSET ADJUST for an output voltage equal to Vref.

Full Scale — Set all data bits to logic "1" and adjust the FULL SCALE ADJUST for an output voltage equal to: Vout = Vref (N-X)/X where "N" is equal to: 255 (DAC-608), 1023 (DAC-610) or 4095 (DAC-612); and "X" is equal to: 128 (DAC-608), 512 (DAC-610) or 2048 (DAC-612).

OUTPUT CODING TABLES

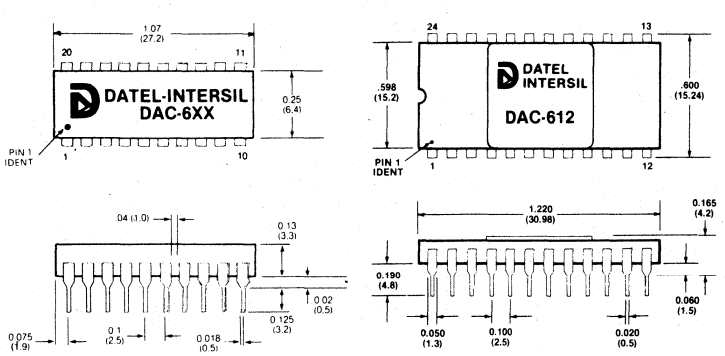
UNIPOLAR OPERATION

INPUT CODE MSB ..... LSB	IDEAL OUTPUT
111 111	−(VREF + 1LSB)
110 000	−.75 (VREF)
100 000	−.5 (VREF)
010 000	−.25 (VREF)
000 000	0

BIPOLAR OPERATION

INPUT CODE MSB ..... LSB	IDEAL OUTPUT	
	+VREF	−VREF
111 111	+VREF-1LSB	−VREF + 1LSB
110 000	.5 (+VREF)	.5 (−VREF)
100 000	0	0
010 000	.5 (−VREF)	.5 (+VREF)
000 000	−VREF	+VREF

MECHANICAL DIMENSIONS INCHES (MM)

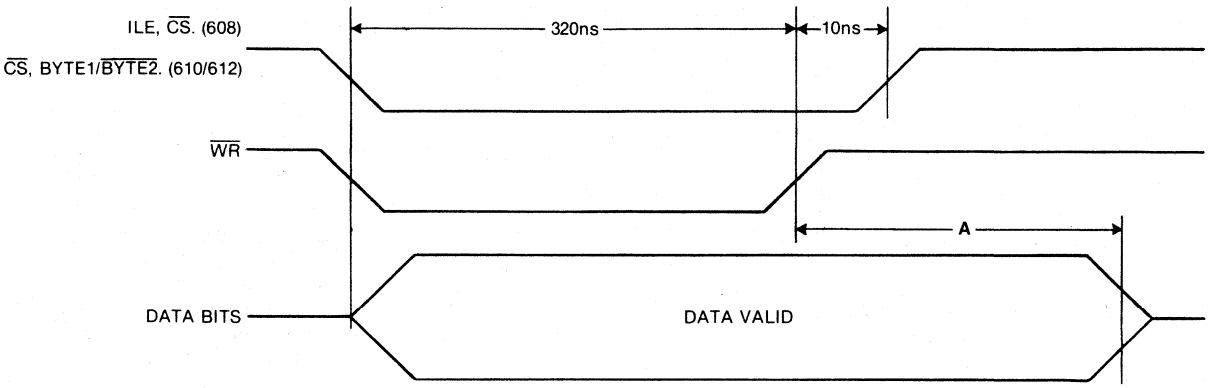


ORDERING INFORMATION

Model	Resolution	Operating Temp. Range	Price (1-24)
DAC-608	8 Bits	0°C to +70°C	
DAC-610	10 Bits	0°C to +70°C	
DAC-612	12 Bits	−25°C to +85°C	

TIMING AND PERFORMANCE

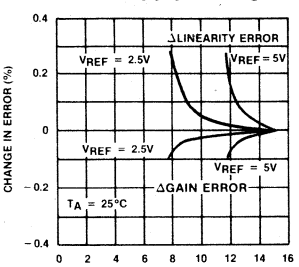
TIMING DIAGRAM



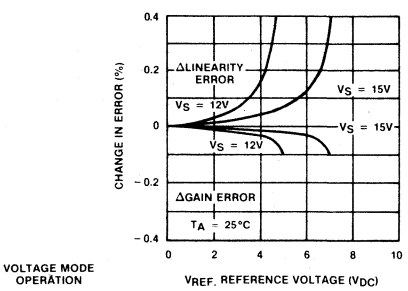
MODEL	A
DAC-608	90ns
DAC-610	200ns
DAC-612	90ns

NOTE:
1. Settling time is measured from the leading edge of the WR pulse.
2. All digital controls are level actuated.

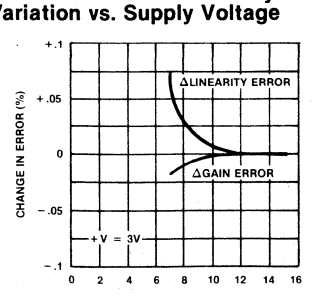
DAC-608 Gain and Linearity Error Variation vs. Supply Voltage



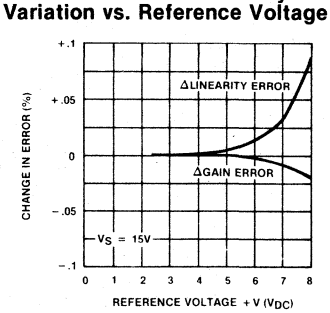
DAC-608 Gain and Linearity Error Variation vs. Reference Voltage



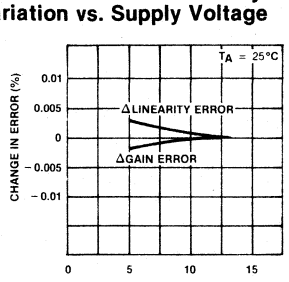
DAC-610 Gain and Linearity Error Variation vs. Supply Voltage



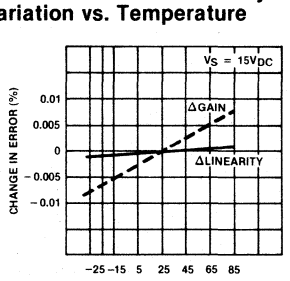
DAC-610 Gain and Linearity Error Variation vs. Reference Voltage



DAC-612 Gain and Linearity Error Variation vs. Supply Voltage

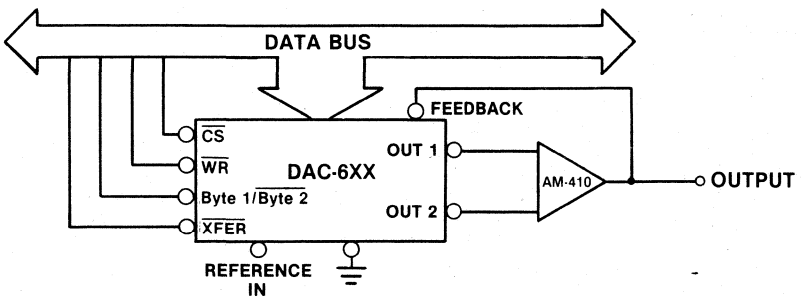


DAC-612 Gain and Linearity Error Variation vs. Temperature



APPLICATIONS

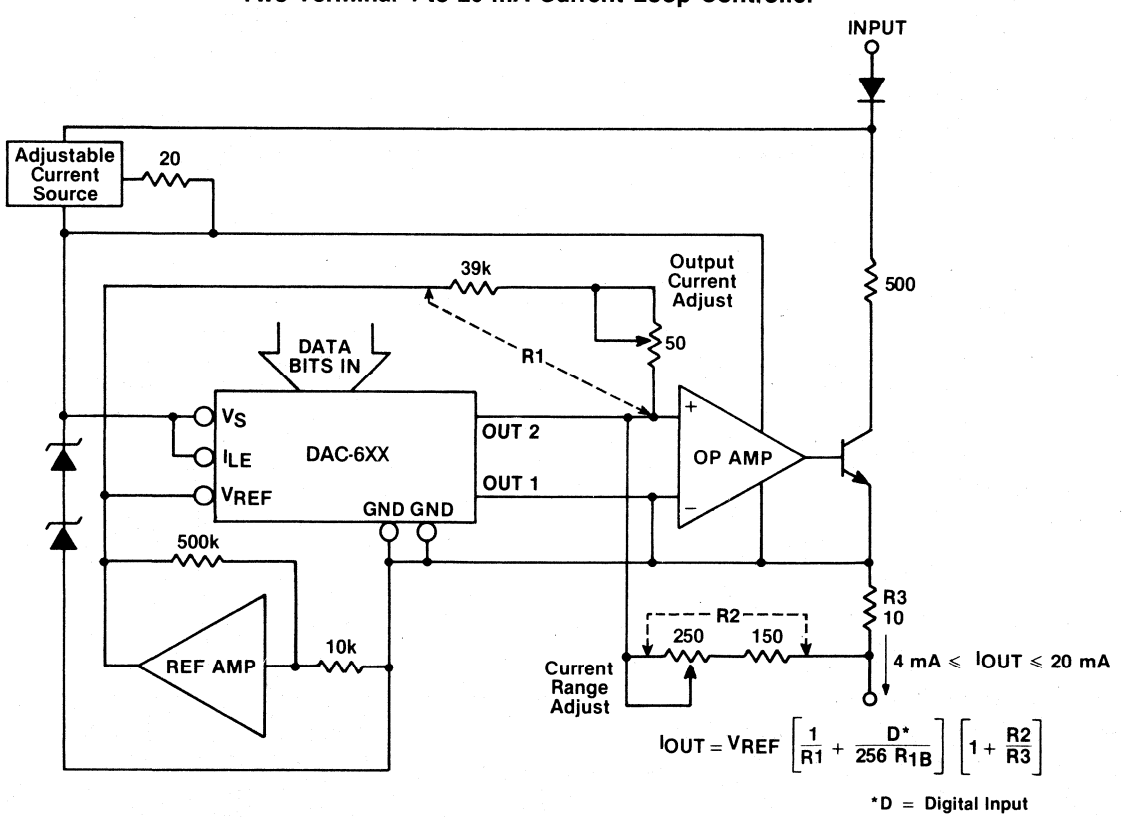
Typical Connection to Popular Microprocessor Data Bus



The logic functions of the DAC-608/610/612 have been oriented towards an ease of interface with all popular microprocessors.

The devices are treated as a typical memory device or I/O peripheral requiring no external logic in most systems due to the timing and logic level convention of the input control signals.

Two Terminal 4 to 20 mA Current Loop Controller



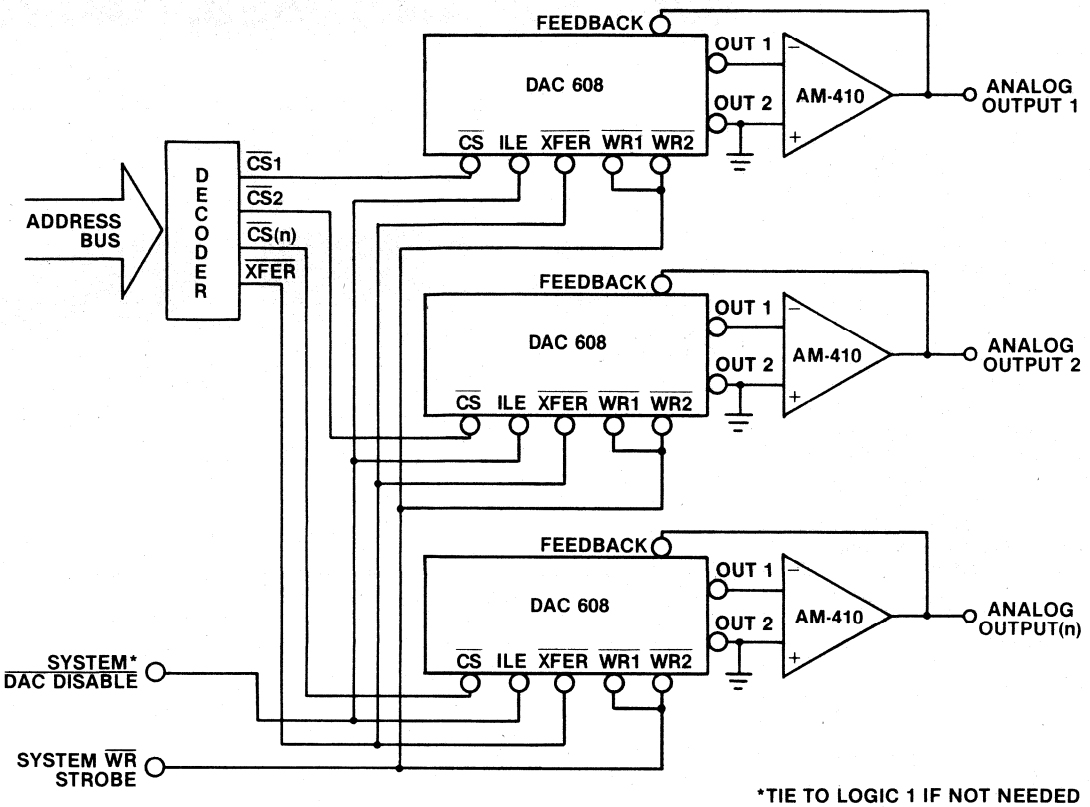
The standard 4 mA to 20 mA industrial process current loop controller is an application where automatic, microprocessor controlled operation is often required. The circuit shown, linearly controls the current flow from input to output to be 4 mA (all bits OFF) to 20 mA (all bits ON).

The low power requirements of the DAC-608/610/612 allow the design of a controller that is powered directly from the loop it is controlling.

In non-microprocessor based systems where loop control is accomplished by thumbwheel switches, the input data to the D/A can be derived from BCD to binary CMOS logic circuitry.

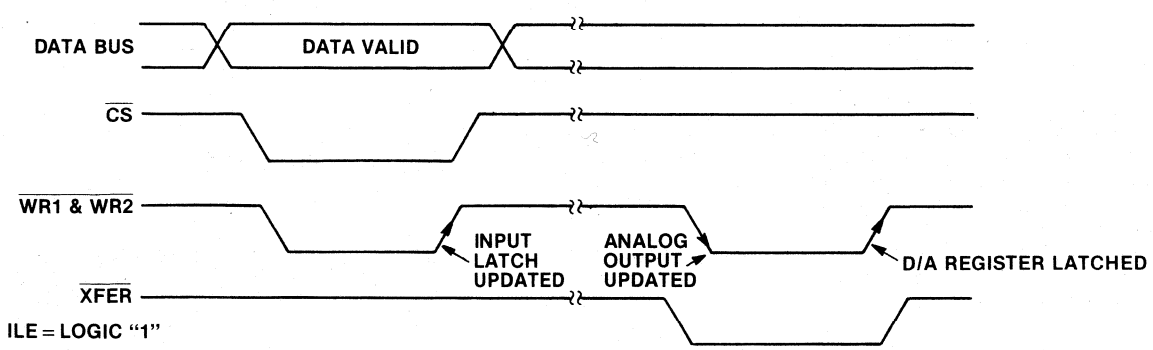
APPLICATIONS

MULTIPLE D/A SYSTEM



*TIE TO LOGIC 1 IF NOT NEEDED

TIMING DIAGRAM



For simultaneous updating of multiple D/A's, the $\overline{CS}$ line of each device is decoded individually. However, the converter can share a common $\overline{XFER}$.

The ILE function is very useful in applications where more than one processor is being used. If another processor took control of the data bus and control lines using the same addresses as the first, a low on the ILE pin would latch the data in the input register holding the outputs at their present state.

NEW

DATEL

Monolithic 8, 10, And 12 Bit Multiplying D/A Converters DAC-7523, DAC-7533, DAC-7541

FEATURES

- **8, 10 and 12 Bit Resolution**
- **150 nsec Settling Time — DAC-7523**
- **4 Quadrant Multiplication**
- **Low Gain and Linearity Tempco's**
- **Single Supply Operation**
- **DTL/TTL/CMOS Compatible**
- **Industry Standard Pin-out**

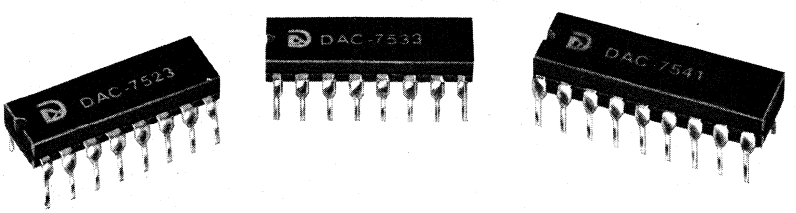
DESCRIPTION

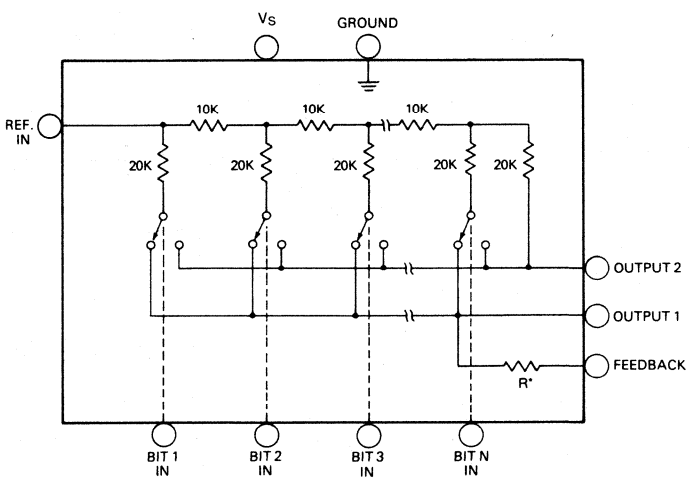
DATEL-INTERSIL's DAC-7523, DAC-7533 and DAC-7541 are monolithic 8, 10 and 12 bit multiplying digital to analog converters. These devices use advanced thin-film-ON-CMOS technology to fabricate a highly stable thin-film R-2R resistor ladder network and NMOS SPDT switches. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. All that is required for most voltage output applications are an external voltage or current reference and output operational amplifier. All models are capable of four quadrant multiplication and the inputs are fully static protected.

Important features include a settling time for the DAC-7523, DAC-7533 and DAC-7541 of 150 nS, 600 nS and 1 μS respectively to $\pm$ ½ LSB max. Maximum linearity error tempco is 2ppm/°C nA and feedthrough error is $\pm$ ½ LSB maximum. Power supply rejection is as low as 0.005% of FSR/%. The devices require only a single supply for operation. Power supply range is +5V to +15V.

The combination of low cost, four quadrant multiplication, full input protection and low power dissipation make these devices an ideal choice for many applications including digitally controlled gain circuits, attenuators, CRT character generation, programmable power supplies, motor speed controls and low noise audio gain control circuits.

The DAC-7523 and DAC-7533 are packaged in 16 pin plastic cases with the DAC-7541 being packaged in an 18 pin plastic case. All models are specified for operation over the commercial, 0°C to +70°C temperature range.





INPUT/OUTPUT CONNECTIONS

DAC-7523

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 (MSB)
5	BIT 2
6	BIT 3
7	BIT 4
8	BIT 5
9	BIT 6
10	BIT 7
11	BIT 8 (LSB)
12	N.C.
13	N.C.
14	V_S
15	REFERENCE IN
16	FEEDBACK

DAC-7533

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 (MSB)
5	BIT 2
6	BIT 3
7	BIT 4
8	BIT 5
9	BIT 6
10	BIT 7
11	BIT 8
12	BIT 9
13	BIT 10 (LSB)
14	V_S
15	REFERENCE IN
16	FEEDBACK

DAC-7541

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 (MSB)
5	BIT 2
6	BIT 3
7	BIT 4
8	BIT 5
9	BIT 6
10	BIT 7
11	BIT 8
12	BIT 9
13	BIT 10
14	BIT 11
15	BIT 12 (LSB)
16	V_S
17	REFERENCE IN
18	FEEDBACK

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-7523/7533/7541
Typical at 25°C, +15V Supply, +10V Reference unless otherwise noted.

MAXIMUM RATINGS	DAC-7523	DAC-7533	DAC-7541
Supply Voltage, (V_S)		+ 17V	
Logic Input Voltage Range		V_S to GND	
Reference Input Voltage Range		± 25V	
Output Voltage Compliance	− 0.3V to V_S	− 0.3V to V_S	− 100mV to V_S
INPUTS			
Resolution	8 Bits	10 Bits	12 Bits
Coding, Unipolar Operation		Straight Binary	
Coding, Bipolar Operation		Offset Binary	
Logic Threshold, Bit ON ("1"), min.		2.4V	
Logic Threshold, Bit OFF ("0"), max.		0.8V	
Logic Input Current, max.[1]		± 1 μA	
Input Capacitance, max.[2]		4 pF	
Reference Input Voltage Range		± 10V	
Reference Input Resistance[3]		10 kΩ	
OUTPUTS			
Output Voltage Compliance		− 100 mV to V_S	
Output Capacitance, output 1, max.[4]	100 pF	100 pF	100 pF
Output Capacitance, output 2, max.[4]	30 pF	35 pF	60 pF
Output Capacitance, output 1, max.[5]	30 pF	35 pF	60 pF
Output Capacitance, output 2, max.[5]	100 pF	100 pF	200 pF
PERFORMANCE			
Non Linearity, max.[6]		± ½ LSB	
Non Linearity Tempco, max.[2,6]		2 ppm/°C	
Gain Error, max.[6]	± 1.5% of FSR	± 1.4% of FSR	± 0.3% of FSR
Gain Error Tempco, max.[2,6]		10 ppm of FSR/°C	
Output Leakage Current, max.[7]		± 50 nA	
Output Current Settling Time, max.[8]	150 nsec	600 nsec	1 μsec
Feedthrough Error, max.[9]		± ½ LSB	
Power Supply Rejection[2]	0.02% FSR/%	0.005% FSR/%	0.01% FSR/%
POWER REQUIREMENT			
Power Supply Voltage Range		+ 5V to + 16V	
Power Supply Current, max.	100 μA	2 mA	2 mA
PHYSICAL-ENVIRONMENTAL			
Operating Temp. Range		0°C to + 70°C	
Storage Temp. Range		− 65°C to + 150°C	
Package Type, Plastic	16 Pin DIP	16 Pin DIP	18 Pin DIP

NOTES:
1. For input voltage = 0V or + 15V.
2. Guaranteed by design not tested.
3. All digital inputs tied high, OUTPUT 1 tied to ground.
4. All digital inputs high.
5. All digital inputs low.
6. Using internal feedback resistor.
7. Accuracy not guaranteed unless outputs at ground potential.
8. Either output. Specified to ± ½ LSB for a full scale change. Load resistance = 100Ω.
9. Reference voltage = ± 10V, 200 kHz for DAC-7523, 100 kHz for DAC-7533, and 10 kHz for DAC-7541. All digital inputs low.

TECHNICAL NOTES

1. The digital control inputs are zener protected, however, permanent damage may occur to unconnected units under high electrostatic fields. All unused devices should be kept in conductive foam at all times.
   Unused digital inputs must be connected to V_S or ground for proper operation of the device. Voltages higher than V_S or less than ground should not be applied to any terminal except V_{ref} or damage may occur.
2. Static performance of these devices depends on output 1 and output 2 (Pins 1 and 2) being exactly at ground potential (Pin 3).
3. The output amplifier should be selected to have a low input bias current (typically less than 75 nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than ± 200 μV). A bias current compensation resistor in the output amplifier's non-inverting input (when used) can cause a variable offset. To prevent this, the non-inverting input should be connected directly to ground with a low resistance wire.
4. To prevent ground loop problems, connect all pins going to ground to a common point using separate connections.
5. The power supply used should have a low noise level and should not have any transients which exceed + 17V.
6. If gain adjustment is required, low tempco (approximately 50 ppm/°C) resistors or trim-pots should be selected.

ORDERING INFORMATION

MODEL	RESOLUTION	PRICE
DAC-7523	8 Bits	$
DAC-7533	10 Bits	$
DAC-7541	12 Bits	$

NEW

DATEL

Ultra-Fast 8 Bit Composite Video D/A's DAC-8308, DAC-8318

FEATURES

- **40 MHz Update Rate**
- **Composite Sync. and Blanking**
- **No Deglitching Required**
- **Direct Drive to 75Ω Load**
- **Adjustable Setup**
- **0°C to +70°C Operation**

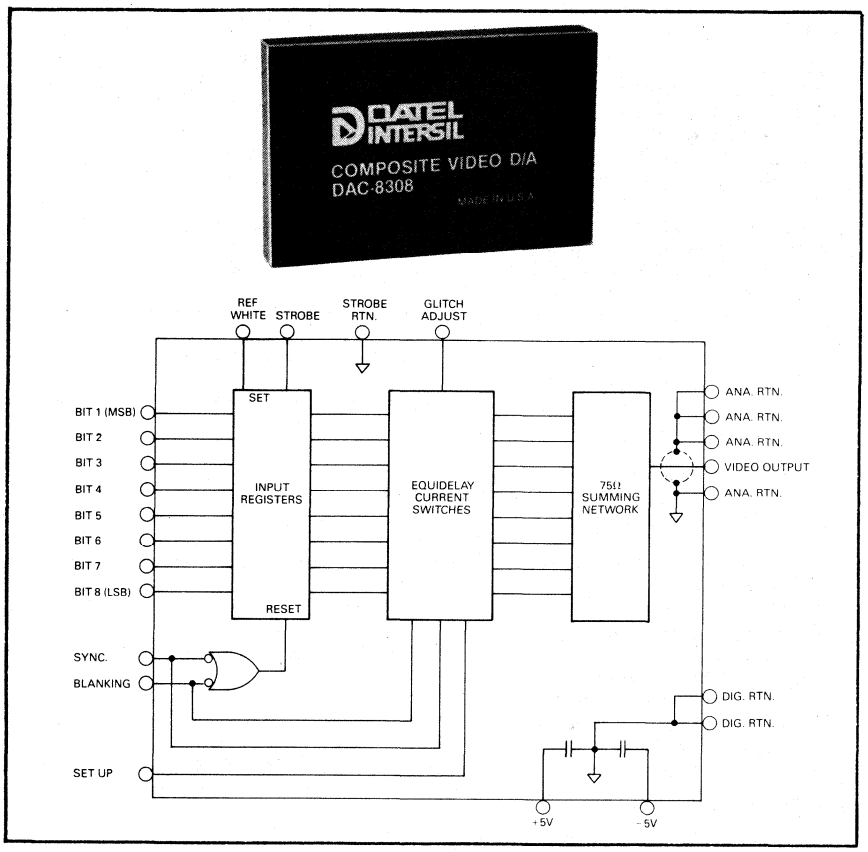
GENERAL DESCRIPTION

Datel-Intersil's DAC-8308 and DAC-8318 are high performance ultra-fast 8 bit digital to analog converters. Functionally complete, including an internal input register, equidelay current switches and a high speed 75Ω summation network; these devices are specifically designed for video and graphic display applications.

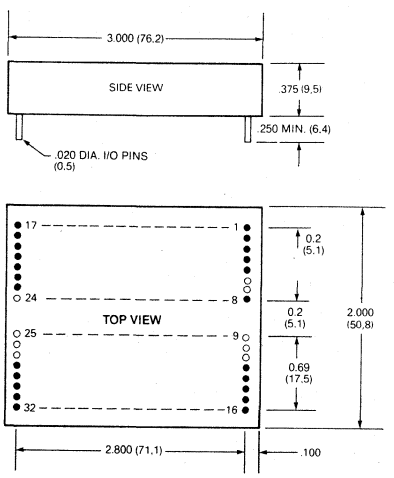
The DAC-8308 accepts 8 bits at throughput rates up to 40 MHz and produces a composite video output signal with 256 gray levels, including setup, blanking and sync., all derived from separate digital inputs. The output will directly drive a terminated 75 coaxial cable giving a 0 to −1.054V output that is in general conformance with EIA standards RS170 and RS343A. Models with a "B" suffix have the output voltage offset by +392 mV so that an input code of 0111 1111 (the middle of the gray scale) produces an output of approximately OV. Output steps are so clean that deglitching is not required.

The DAC-8318 is the same converter without the composite video digital inputs. An ideal choice for time base correction and function generation applications, the DAC-8318 converts 8 bits of data into a 3 nsec rise time output.

Both modules are packaged in 2 × 3 × 0.375 inch cases, allowing ½ inch board spacing and operate over the 0°C to +70°C temperature range. Digital inputs are TTL compatible and power requirement is ±5V. These devices are an excellent choice for applications involving raster scan high resolution video (both color and monochrome), graphic display systems, function generation and time base correction.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS — ON DAC-8318 PINS 8 + 14 are omitted
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	DAC-8308 FUNCTION	DAC-8318 FUNCTION
1	ANALOG RETURN	ANALOG RETURN
2	ANALOG RETURN	ANALOG RETURN
3	ANALOG RETURN	ANALOG RETURN
4	VIDEO OUT	OUTPUT
5	ANALOG RETURN	ANALOG RETURN
8	SETUP	
12	STROBE RETURN	STROBE RETURN
13	STROBE	STROBE
14	SYNC.	
15	PEAK WHITE	SET
16	BLANKING	RESET
17	−5V POWER IN	−5V POWER IN
18	DIGITAL RETURN	DIGITAL RETURN
19	DIGITAL RETURN	DIGITAL RETURN
20	+5V POWER IN	+5V POWER IN
21	BIT 1 (MSB) INPUT	BIT 1 (MSB) INPUT
22	BIT 2 INPUT	BIT 2 INPUT
23	BIT 3 INPUT	BIT 3 INPUT
24	BIT 4 INPUT	BIT 4 INPUT
28	GLITCH ADJUST	GLITCH ADJUST
29	BIT 5 INPUT	BIT 5 INPUT
30	BIT 6 INPUT	BIT 6 INPUT
31	BIT 7 INPUT	BIT 7 INPUT
32	BIT 8 (LSB) INPUT	BIT 8 (LSB) INPUT

DATEL-INTERSIL INC. 11 CABOT BOULEVARD MANSFIELD MA 02048/TEL (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-8308 and DAC-8318
Typical at +25°C, ±5V supplies unless otherwise noted.

OUTPUT CHARACTERISTICS	
Output Voltage Range[1]	0V to −1V ±5% into 75Ω termination.
Output Current	−28 mA short circuit, −14 mA into 75Ω.
Recommended Load Impedance	75Ω ±5%, dc to >10 MHz.
Source (Thevenin) Impedance	75Ω ±5%, dc to 50 MHz.
Output Bandwidth min.	100 MHz @ −3 dB.
LSB Size; DAC-8308	2.52 mV nominal
DAC-8318	3.92 mV nominal
Rise and Fall Time, 10% to 90%	3 ns typ., 4 ns max.
Full Step Settling Time, to 1 LSB	7.5 ns
Glitch Settling Time, to 1 LSB[2]	5 ns
Glitch Area; DAC-8318	Equivalent to 1 LSB step @ 50 MHz update rate
DAC-8308	70 pV. sec. max., 50 pV. sec. typ.
TRANSFER CHARACTERISTICS	
Resolution	8 bits, 256 levels.
Coding[3]	Binary.
Differential Linearity, max.	±1/2 LSB
Monotonicity	Guaranteed, 10°C to 70°C.
Offset[4]	±1/2 LSB max., 0°C to 70°C.
Transfer Gain (Slope) Tempco, max.	±0.02%/°C
Propagation Delay	10 ns typ., strobe to output, 50% points.
INPUT CHARACTERISTICS	
Update Rate	40 MHz.
Input Register[5]	8 ECL Type D Flip-Flops
Strobe Input	Data entered on positive-going edge (timing reference).
Setup, min.	7.0 ns before strobe.
Hold, min.	6.0 ns
Logic Levels	Standard 7400 TTL Levels.
Data Input Loading (Each of 8 Inputs)	Two-unit load.
Strobe Input Loading	Two-unit load.
Control Input Loading, max.[6]	2 units each line.
POWER SUPPLY REQUIREMENTS	
Supply Voltage	+5V and −5V, nominal.
Positive Supply: DAC-83XX	5.0V ±5% @ 50 mA
DAC-83XXB	5.0V ±5% @ 75 mA
Negative Supply	−4.75V to −5.5V @ 400 mA
Supply Regulation	Negative supply should not have more than 5 mV P-P ripple.
Supply Common	Digital Return is the common for the +5V and −5V supplies.
ENVIRONMENTAL AND PACKAGING	
Operating Temp. Range	0°C to +70°C.
Storage Temp.	−25°C to +85°C.
Relative Humidity	0 to 100%, non-condensing.
Mechanical Dimensions	2″ × 3″ × 0.375″ (50 × 75 × 10mm).

NOTES:
1. The output of the DAC-8308 will be 0 to −1.054V.
2. For worst case (MSB) transition.
3. DAC-8318: 1111 1111 input code produces 0V output
   0000 0000 input code produces −1V output
   DAC-8308: 1111 1111 input code produces −71 mV
   0000 0000 input code produces −714 mV with standard setup
   — see "Video Characteristics".
4. DAC-8318 — dc output with 1111 1111 input code
   DAC-8308 — dc output with peak white input
5. Includes built-in TTL to ECL translaters in data input lines and strobe.
6. Refers to blanking, sync, and peak white controls for DAC-8318 and set and reset for DAC-8318.

TECHNICAL NOTES

1. The DAC-8308 has three additional current switches in the equi-delay bank: One to inject the Blanking level and one for the Synchronizing level, as required to generate a composite video signal. The Setup Control provides a means for varying brightness in reproducible steps. TV monitors cut off the picture tube in response to the Blanking level, producing the blackest possible visible picture. The Setup control varies the offset between Reference Black level and Blanking level which produces an apparent shift in the "brightness" of Reference Black.

   The Blanking and Sync. control lines are asynchronous. The DAC output goes to the command level in about 12 nsec. 12 nsec after removal, the DAC output goes to Reference Black until the next strobe command.

   The DAC-8308 has additional user flexibility, achieved by the addition of a Peak White control. Assertion of this input drives the output to its most positive voltage: The whiter than white level, or 110% white to be used for cursors etc.

   Peak White sets the input register which turns off the eight gray scale current switches, and the third additional current switch. The Sync or Blanking inputs reset the input register, producing full scale output from the gray scale current switches; the output from the Sync. or Blanking current switches is added to the full scale output. Obviously, Peak White should not be activated during the Sync. or Blanking intervals.
2. The DAC-8318 fullscale output of 1V peak is fully controlled by the 8-bit data word. The DAC-8318 may be connected to the output of a video A/D to regenerate a TV image on a monitor. Assuming that the input digital data of 8 bits includes the Sync tips.

   The Set and Reset inputs of the input register are available on terminals, they produce zero or full scale outputs respectively when activated.

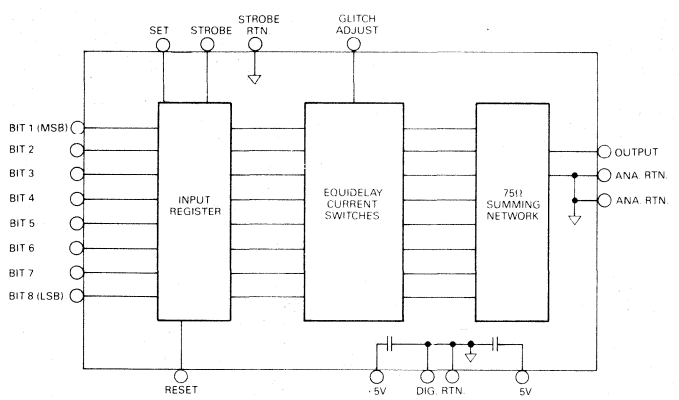
   The DAC-8318 is ideally suited for time base correction and function generation applications.
3. The DAC-8308 and DAC-8318 series are capable of operation from a negative supply voltage between −4.75V to −5.5V. The output amplitudes specified are nominal values set by internal reference. However, if user adjustment is required, the glitch area will vary slightly as a function of the negative supply voltage. The factory trim is carried out at −5.0V, connect a 10K potentiometer to the Glitch Adjust Terminal. Adjust this pot for minimum glitch area at the major carry transition. This pot may be omitted and the Glitch Adjust Terminal left open.
4. EIA Industrial Electronics Tentative Standard No. 1 which will, in the future, become a part of RS170-A, details the exact waveform and timing characteristics of the composite video signal at the output of a color television studio.

   The products described in this data sheet are in general conformance with such needs. Exact compliance requires additional circuitry which would, at a minimum, provide Sin X/X correction and bandwidth filtering.
5. The output bandwidth may be reduced, if desired, by adding a small capacitor across the DAC output. This will result in slower rise times. The absolute glitch amplitude will decrease, but the energy (or net area) of the glitch will be unchanged.
6. The DIG RTN, ANA RTN and STROBE RTN terminals are all tied together internally. The +5V and −5V supply common should be connected to DIG RTN. If a long printed circuit wiring connection is required for integration of the DAC into a video system, stripline wiring techniques may be implemented by taking advantage of the physical arrangement of the output terminals i.e., the ANA RTN terminals are located on each side of the VIDEO OUT terminal. ANA RTN normally connects to the shield of an external 75-ohm coaxial cable. STROBE RTN is included as a convenience and may be used optionally to facilitate connection.
7. The sync and blanking outputs of the MM5320 TV Timing ROM may not be capable of driving the DAC-8308 series, under worst case conditions, without the use of a logic driver.
8. All timing is referenced to the positive edge of the strobe. 7.0 ns and 6.0 ns are required, respectively, for Setup and Hold.

VIDEO CHARACTERISTICS; DAC-8308 ONLY
Typical at +25°C, ±5V supplies unless otherwise noted.

Composite Video Signal	Consists of 256 gray levels plus Peak or 110% white, blanking level and sync level.
Gray Scale Range	0.643V P-P.
Step Size	2.52 mV step.
Peak White Level	0V, absolute; +0.768V (110 IRE Units) relative to blanking level with standard Setup; +0.714V relative to Reference Black, +0.071V (10 IRE units) relative to Ref. White.
Input Code for White Level	11111111.
Peak White Control	Logic "0" (TTL) on Peak White line overrides video input data and drives the output to 0V.
Reference Black Level	−0.714V absolute; +54 mV (7.5 IRE Units) relative to blanking level with standard Setup.
Input Code for Reference Black Level	00000000.
Composite Blanking Level	−0.768V absolute, with standard Setup.
Input Command for Blanking/ Pedestal Level	Logic "0" (TTL) on "Blanking" line simultaneously resets input register to 00000000.
Composite Sync Level	−1.054V absolute with standard Setup; −0.286V (−40 IRE Units) with respect to blanking level (back porch).
Input Command for Sync Level	Logic "0" (TTL) on "Sync" line simultaneously resets input register to 00000000.
Sync and Blanking Rise and Fall Times, max.	100 ns.
Sync and Blanking Overshoot, max.	2%
Setup (Reference Black-to-Blanking)	Externally programmable from 0 mV (0 IRE Units) to 142 mV (20 IRE Units).
Setup Control Line	Input Gnd: Standard 54 mV (7.5 IRE Units). Input Open: 71 mV (10 IRE Units) Setup. Input tied to −5V: 142 mV (20 IRE Units). Input tied to +5V: 0 mV (0 IRE Units).

DAC-8318-BLOCK DIAGRAM



ORDERING INFORMATION

MODEL	OUTPUT	PRICE (1-9)
DAC-8308	Unipolar	
DAC-8308B	Bipolar	
DAC-8318	Unipolar	
DAC-8318B	Bipolar	

GLOSSARY OF VIDEO TERMS

COMPOSITE VIDEO SIGNAL
The combined video signal, with or without Setup, plus the Sync signal.

VIDEO SIGNAL
The visually perceived portion of the composite video signal which varies in gray scale levels from Reference White to Reference Black. Also known as the picture signal.

SYNC OR COMPOSITE SYNC SIGNAL
That portion of the composite video signal which synchronizes the scanning process.

SYNC LEVEL
The level of the peak of the Sync signal.

SETUP
The difference in level between the Reference Black level and the Blanking level. Not to be confused with setup as used in conjunction with digital logic.

RASTER-SCAN
The basic method of sweeping across a CRT, a line at a time, to generate and display pictures such as used in commercial TV in the USA.

MONOCHROME VIDEO
Conventional black-and-white television video in which the Z-axis, or intensity, of the beam is modified during scanning to shade and/or outline images.

BLANKING LEVEL
The level which separates the Sync portion from the video signal, with or without Setup. This level is sometimes also called the pedestal, back porch or front porch. It usually refers to the level which will cut off the TV tube, producing the blackest possible visual picture.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

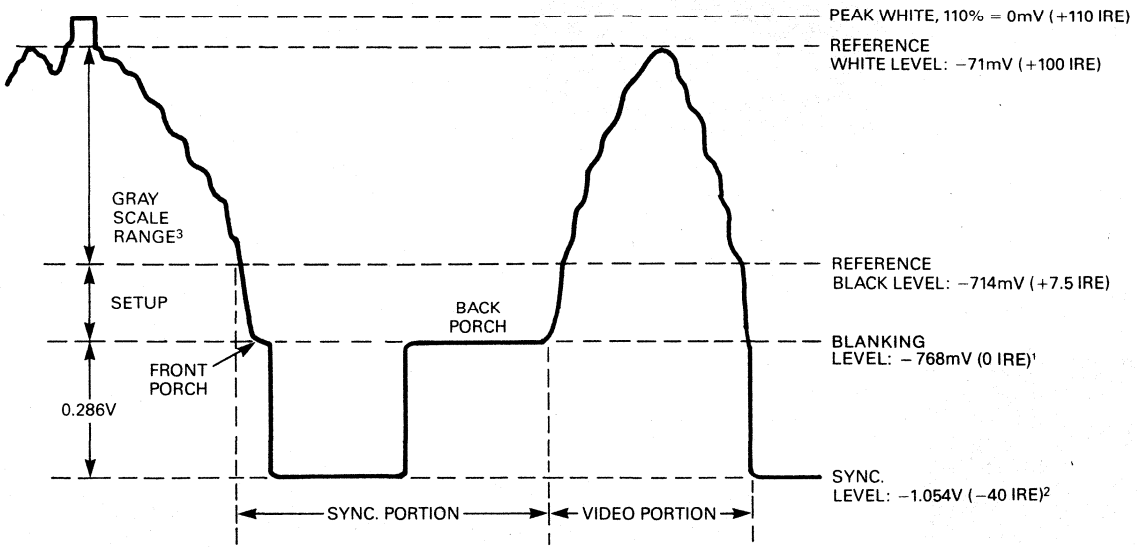
REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

PEAK WHITE LEVEL
A "Whiter than White" Level not within the range of the normal picture. Sometimes used for generating cursors or outlines because it contrasts with all gray shades including white.

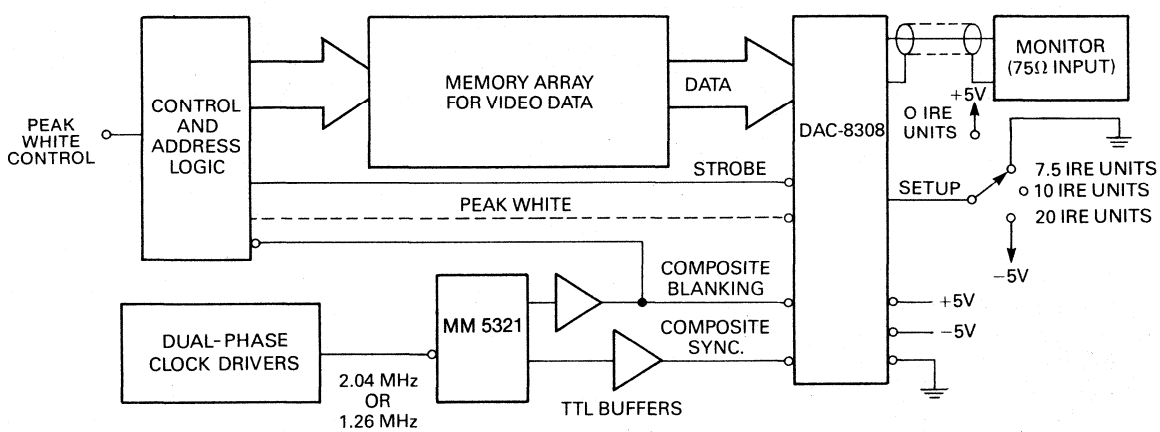
GRAY SCALE
The discrete levels for the video signal between Reference White and Reference Black levels.

COLOR VIDEO (RGB)
As used herein, this refers to the method of generating color images by combining the three primary colors of red-green-blue (RGB). The associated monitor would be identified as an "RGB" monitor. Three DAC-8308 series D/A converters are required to drive such a monitor, one each for red, green and blue.

COMPOSITE VIDEO OUTPUT (NOT TO SCALE)

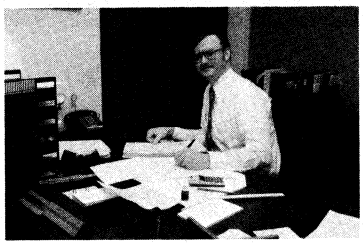


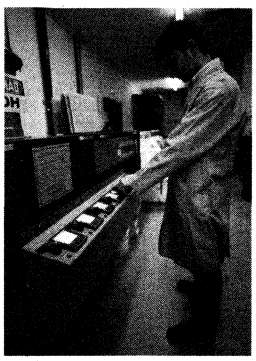
1. For Standard −7.5 IRE Setup. For −10 IRE Setup = −785 mV, −20 IRE = −857 mV.
2. For Standard −7.5 IRE Setup with Blanking present during Sync time.
   For −10 IRE Setup = 1.071V, −20 IRE = −1.143V.
   0 IRE Setup or with Blanking not present during Sync = −1.000V
3. Gray Scale: LSB = 2.52 mV = 0.363 IRE
   MSB = 321 mV = 46.43 IRE

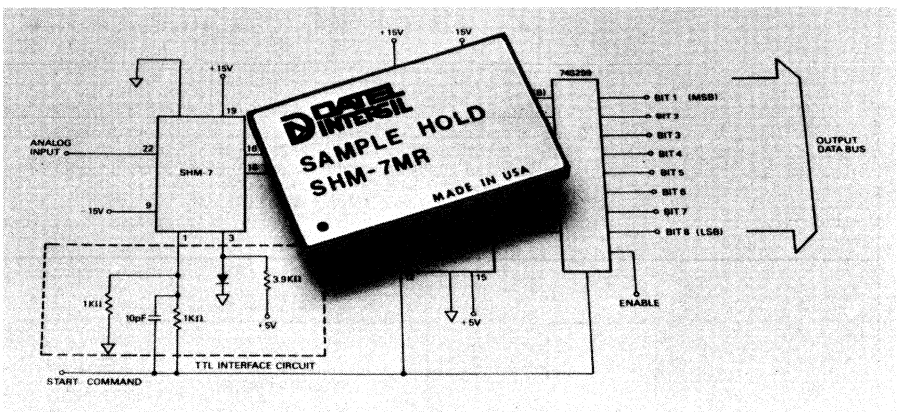


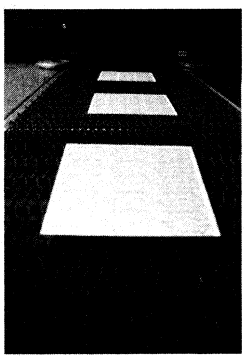
TYPICAL SMALL DISPLAY SYSTEM

With this circuit, digital video data, digital sync. and digital blanking are converted directly to a composite monitor input. Analog mixing and/or generation of the sync/blanking is not required, nor is a separate high power driver amplifier required ahead of the monitor. With the inherently low glitch design of the DAC-8308/8318, a deglitcher is not required and video data need not be "aligned" to achieve low glitch performance.






+15V
15V
DATEL INTERSIL
SAMPLE HOLD
SHM-7MR
MADE IN USA
74S299
BIT 1 (MSB)
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8 (LSB)
OUTPUT DATA BUS
ANALOG INPUT
22
SHM-7
9
1
3
16
15V
1KΩ
10pF
1KΩ
3.9KΩ
+5V
TTL INTERFACE CIRCUIT
START COMMAND
ENABLE



SAMPLE/HOLD AMPLIFIERS

Sample-Hold Amplifiers

Operation of Sample-Holds

Sample-hold circuits are the devices which store analog information and reduce the aperture time of an A/D converter. A sample-hold is simply a voltage-memory device in which an input voltage is acquired and then stored on a high quality capacitor. A popular circuit is shown in Figure 1.

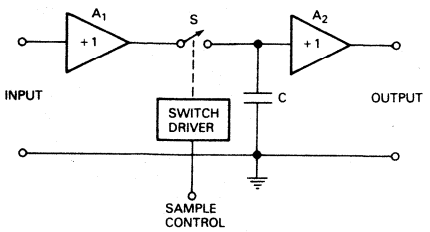


Figure 1. Popular Sample-Hold Circuit

A_1 is an input buffer amplifier with a high input impedance so that the source, which may be an analog multiplexer, is not loaded. The output of A_1 must be capable of driving the hold capacitor with stability and enough drive current to charge it rapidly. S_1 is an electronic switch, generally an FET, which is rapidly switched on or off by a driver circuit which interfaces with TTL inputs.

C is a capacitor with low leakage and low dielectric absorption characteristics; it is a polystyrene, polycarbonate, polypropylene, or teflon type. In the case of hybrid sample-holds, the MOS type capacitor is frequently used.

A_2 is the output amplifier which buffers the voltage on the hold capacitor. It must therefore have extremely low input bias current, and for this reason an FET input amplifier is required.

There are two modes of operation for a sample-hold: *sample* (or tracking) *mode,* when the switch is closed; and *hold mode,* when the switch is open. Sample-holds are usually operated in one of two basic ways. The device can continuously track the input signal and be switched into the hold mode only at certain specified times, spending most of the time in tracking mode. This is the case for a sample-hold employed as a deglitcher at the output of a D/A converter, for example.

Alternatively, the device can stay in the hold mode most of the time and go to the sample mode just to acquire a new input signal level. This is the case for a sample-hold used in a data acquisition system following the multiplexer.

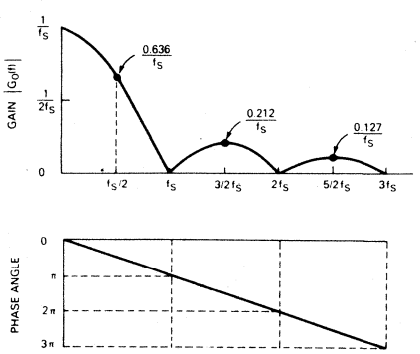


Figure 2. Gain and Phase Components of Zero-Order Hold Transfer Function

The Sample-Hold as a Data Recovery Filter

A common application for sample-hold circuits is *data recovery,* or *signal reconstruction, filters.* The problem is to reconstruct a train of analog samples into the original signal; when used as a recovery filter, the sample-hold is known as a *zero-order hold.* It is a useful filter because it fills in the space between samples, providing data smoothing.

As with other filter circuits, the gain and phase components of the transfer function are of interest. By an analysis based on the impulse response of a sample-hold and use of the Laplace transform, the transfer function is found to be

$$G_0(f) = \frac{1}{f_s}\left[\frac{\sin \pi\left(\frac{f}{f_s}\right)}{\pi\left(\frac{f}{f_s}\right)}\right] \epsilon^{-j\pi f/f_s}$$

where f_s is the sampling frequently. This function contains the familiar (sin x) /x term plus a phase term, both of which are plotted in Figure 2.

The sample-hold is therefore a low pass filter with a cut-off frequency slightly less than $f_s/2$ and a linear phase response which results in a constant delay time of T/2, where T is the time between samples. Notice that the gain function also has significant response lobes beyond f_s. For this reason a sample-hold reconstruction filter is frequently followed by another conventional low pass filter.

Other Sample-Hold Circuits

In addition to the basic circuit of Figure 1, there are several other sample-hold circuit configurations which are frequently used. Figure 3 shows two such circuits which are closed loop circuits as contrasted with the open loop circuit of Figure 1. Figure 3(a) uses an operational integrator and another amplifier to make a fast, accurate inverting sample-hold. A buffer amplifier is sometimes added in front of this circuit to give high input impedance. Figure 3(b) shows a high input impedance non-inverting sample-hold circuit.

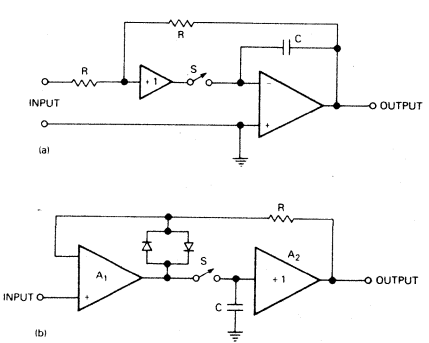


Figure 3. Two Closed Loop Sample-Hold Circuits

The circuit in Figure 1, although generally not as accurate as those in Figure 3, can be used with a diode-bridge switch to realize ultra-fast acquisition sample-holds, such as those shown in Figure 4.

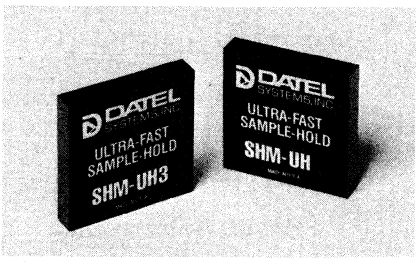


Figure 4. Ultra-Fast Sample-Hold Modules Which Employ Diode-Bridge Switches

Sample-Hold Characteristics

A number of parameters are important in characterizing sample-hold performance. Probably most important of these is *acquisition time.* The definition is similar to that of settling time for an amplifier. It is the time required, after the sample-command is given, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band around final value.

Several hold-mode specifications are also important. *Hold-mode droop* is the output voltage change per unit time when the sample switch is open. This droop is caused by the leakage currents of the capacitor and switch, and the output amplifier bias current. *Hold-mode feedthrough* is the percentage of input signal transferred to the output when the sample switch is open. It is measured with a sinusoidal input signal and caused by capacitive coupling.

The most critical phase of sample-hold operation is the transition from the sample mode to the hold mode. Several important parameters characterize this transition. *Sample-to-hold offset* (or step) *error* is the change in output voltage from the sample mode to the hold mode, with a constant input voltage. It is caused by the switch transferring charge onto the hold capacitor as it turns off.

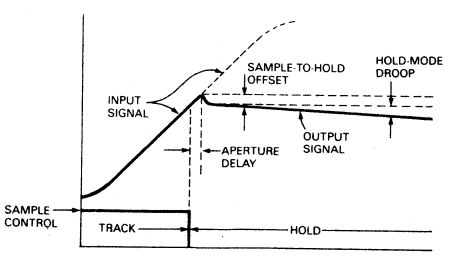


Figure 5. Some Sample-Hold Characteristics

Aperture delay is the time elapsed from the hold command to when the switch actually opens; it is generally much less than a microsecond. *Aperture uncertainty* (or *aperture jitter*) is the time variation, from sample to sample, of the aperture delay. It is the limit on how precise is the point in time of opening the switch. Aperture uncertainty is the time used to determine the aperture error due to rate of change of the input signal. Several of the above specifications are illustrated in the diagram of Figure 5.

Sample-hold circuits are simple in concept, but generally difficult to fully understand and apply. Their operation is full of subtleties, and they must therefore be carefully selected and then tested in a given application.

Glossary of Sample-Hold Amplifier Terms

APERTURE DELAY TIME: in a sample-hold, the time elapsed from the hold command to the actual operating of the sampling switch.

APERTURE JITTER: See *Aperture Uncertainty Time.*

APERTURE TIME: The time window, or time uncertainty, in making a measurement. For an A/D converter it is the conversion time; for a sample-hold it is the signal averaging time during the sample-to-hold transition.

APERTURE UNCERTAINTY TIME: In a sample-hold, the time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample.

CHARGE TRANSFER: In a sample-hold, the phenomenon of moving a small charge from the sampling switch to the hold capacitor during switch turn-off. This is caused by the switch control voltage change coupling through switch capacitance to the hold capacitor. Also called *charge dumping* or *charge injection.*

CREEP VOLTAGE: A voltage change with time across an open capacitor caused by dielectric absorption. This causes sample-hold output error.

DEGLITCHER: A special sample-hold circuit used to eliminate the output spikes (or glitches) from a D/A converter.

DIELECTRIC ABSORPTION: A voltage memory characteristic of capacitors caused by the dielectric material not polarizing instantaneously. The result is that not all the energy stored in a charged capacitor can be quickly recovered upon discharge, and the open capacitor voltage will creep. See also *Creep Voltage.*

EFFECTIVE APERTURE DELAY: In a sample-hold, the time difference between the hold command and the time at which the input signal equalled the held voltage.

EXTRAPOLATIVE HOLD: See *First-Order Hold.*

FIRST-ORDER HOLD: A type of sample-hold, used as a recovery filter, which uses the present and previous analog samples to predict the slope to the next sample. Also called an *extrapolative hold.*

FRACTIONAL-ORDER HOLD: A type of sample-hold, used as a recovery filter, which uses a fixed fraction of the difference between the present and previous analog samples to predict the slope to the next sample.

HOLD CAPACITOR: A high quality capacitor used in a sample-hold circuit to store the analog voltage. The capacitor must have low leakage and low dielectric absorption. Types commonly used include polystyrene, teflon, polycarbonate, polypropylene, and MOS.

HOLD-MODE: The operating mode of a sample-hold circuit in which the sampling switch is open.

HOLD-MODE DROOP: In a sample hold, the output voltage change per unit of time with the sampling switch open. It is commonly expressed in V/sec. or $\mu V/\mu$ sec.

HOLD—MODE FEEDTHROUGH: In a sample-hold, the percentage of input sinusoidal or step signal measures at the output with the sampling switch open.

HOLD-MODE SETTLING TIME: In a sample-hold, the time from the hold command transition until the output has settled within a specified error band.

INTERPOLATIVE HOLD: See *Polygonal Hold.*

INFINITE-HOLD: A sample-hold circuit which converts an analog voltage into digital form which is then held indefinitely, without decay, in a register.

POLYGONAL HOLD: A type of sample-hold, used as a signal recovery filter, which produces a voltage output which is a straight line joining the previous sample value to the present sample. This results in an accurate signal reconstruction but with a one sample-period output delay.

SAMPLE-HOLD: A circuit which accurately acquires and stores an analog voltage on a capacitor for a specified period of time.

SAMPLE-HOLD FIGURE OR MERIT: The ratio of capacitor charging current in the sample-mode to the leakage current off the capacitor in the hold-mode.

SAMPLE-MODE: The operating mode of a sample-hold circuit in which the sampling switch is closed.

SAMPLE-TO-HOLD OFFSET ERROR: For a sample-hold, the change in output voltage from the sample-mode to the hold-mode, with constant input voltage. This error is caused by the sampling switch transferring charge onto the hold capacitor as it opens.

SAMPLE-TO-HOLD STEP: See *Sample-to-Hold Offset Error.*

SAMPLE-TO-HOLD TRANSIENT: A small spike at the output of a sample-hold when it goes into the hold mode. It is caused by feedthrough from the sampling switch control voltage.

SIMULTANEOUS SAMPLE-HOLD: A system in which a series of sample-hold circuits are used to sample a number of analog channels, all at the same instant. This requires one sample-hold per analog channel.

TRACK-AND-HOLD: A sample-hold circuit which can continuously follow the input signal in the sample-mode and then go into hold-mode upon command.

ZERO-ORDER HOLD: A name for a sample-hold circuit used as a data recovery filter. It is used to accurately reconstruct an analog signal from a train of analog samples.

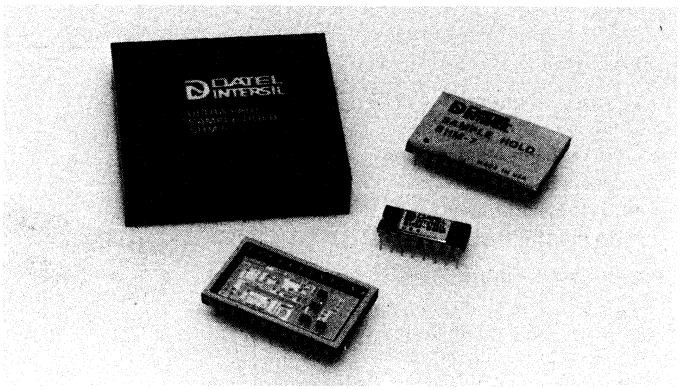
Quick selection: Sample-holds:

	MODEL	DESCRIPTION	ACCURACY	ACQUISITION TIME	APERTURE DELAY	INPUT RANGE	HOLD-MODE DROOP
	SHM-5	Ultra-fast High Accuracy S/H	0.01%	350 ns	20 ns	± 10V	20 μV/μs
	SHM-6MC	High Speed Completely Self-contained S/H	0.01%	1 μs	20 ns	± 10V	10 μV/μs
	SHM-6MR						
	SHM-6MM						
NEW	SHM-9MC	Low cost Completely Self-contained S/H	0.01%	6 μs	200 ns	± 10V	0.2 mV/ms
NEW	SHM-9MR						
NEW	SHM-9MM						
NEW	SHM-20C	High Speed Monolithic S/H with Internal Hold Capacitor	0.01%	1μs	30 ns	± 10V	0.08 μV/μs
NEW	SHM-20M						
	SHM-IC-1	Low cost Monolithic S/H	0.01%	5 μs	50 ns	± 10V	50 μV/ms
	SHM-IC-1M						
	SHM-LM-2	Low cost Monolithic	0.01%	6 μs	200 ns	± 10V	0.2 mV/ms
	SHM-LM-2M						
	SHM-UH3	Ultra-fast	0.05%	30 ns	5 ns	± 5V	50 μV/μs
	SHM-HUMC	Ultra-fast Hybrid S/H	0.1%	25 ns	6 ns	± 2.5V	50 μV/μs
	SHM-HUMR						
	SHM-HUMM						
NEW	SHM-7MC	Ultra fast- Dual-outputs	0.1%	40 ns	3 ns	± 5V ± 2.5V	100 μV/μs
NEW	SHM-7MR						
	SHM-2	High Speed	0.1%	100 ns	10 ns	± 10V	50 μV/μs
	SHM-2E						330 μV/μs
	SHM-UH	Ultra Fast	0.25%	50 ns	10 ns	± 5V	50 μV/μs
NEW	SHM-4860MC	Ultra-Fast High Accuracy S/H	0.01%	200 ns	6 ns	± 10.25V	0.5μV/μs
NEW	SHM-4860MR						
NEW	SHM-4860MM						

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

DATEL-INTERSIL'S broad line of sample-hold amplifiers offer a range of price and performance designed to fit most data acquisition applications.

New models include: the SHM-7, an ultra-high speed, dual output, 0.1% sample-hold; the SHM-9, a low cost, completely self contained 0.01% sample-hold, and the SHM-20, a high speed, 0.01%, monolithic sample-hold featuring an internal, 100 pf MOS hold capacitor.



GAIN	BANDWIDTH	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE	SEE PAGE
−1.00	5 MHz	2 x 2 x 0.375 in (51 x 51 x 10 mm)	Module	0 to +70	218
±1 to ±10	5 MHz	32-pin DIP	Hybrid	0 to +70	220
				−25 to +85	
				−55 to +100	
+1.00	4 MHz	16-pin DIP	Hybrid	0 to +70	228
				−25 to +85	
				−55 to +125	
10^6 V/V	2MHz	14-pin DIP	Monolithic	0 to +70	234
				−55 to +125	
±1.00	2 MHz	14-pin DIP	Monolithic	0 to +70	206
				−55 to +125	
+1.00	1 MHz	8-pin TO-99	Monolithic	0 to +70	212
				−55 to +125	
+0.98	45 MHz	2 x 2 x 0.375 in (51 x 51 x 10 mm)	Module	0 to +70	214
+0.975	50 MHz	24-pin DIP	Hybrid	0 to +70	210
				−25 to +85	
				−55 to +100	
+0.995	40 MHz	24-pin DIP	Hybrid	0 to +70	224
				−25 to +85	
+1.00	10 MHz	2 x 1 x 0.375 in (51 x 25 x 10 mm)	Module	0 to +70	—
+0.95	45 MHz	2 x 2 x 0.375 in (51 x 51 x 10 mm)	Module	0 to +70	214
−1.00	16 MHz	24-pin DIP	Hybrid	0°C to +70°C	238
				−25°C to +85°C	
				−55°C to +125°C	

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

Monolithic Sample-Hold
SHM-IC-1

FEATURES

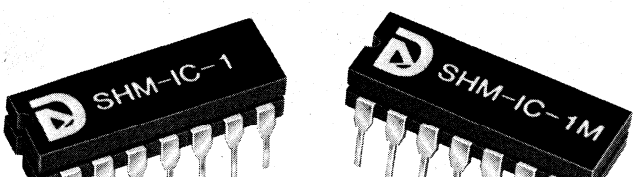
- 5 μsec. Acquisition to .01%
- 50 nsec. Aperture
- Inverting or Noninverting
- 2MHz Bandwidth
- .01% Feedthrough
- 14 Pin DIP Package

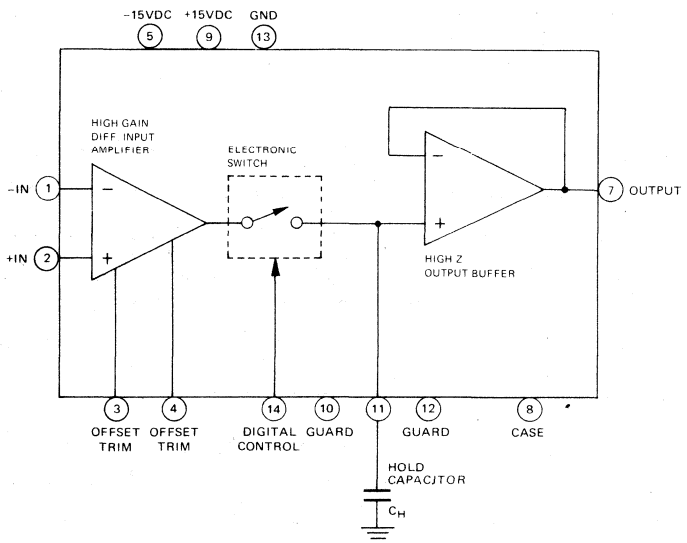
GENERAL DESCRIPTION

The SHM-IC-1 is a new monolithic integrated circuit sample and hold with excellent performance features. It is a self-contained device requiring only an external holding capacitor, the value of which can be chosen by the user to achieve his desired speed and accuracy requirement. The unit consists of a high gain differential input amplifier, a digitally controlled electronic switch, and a high input impedance buffer amplifier. The SHM-IC-1 operates in a closed loop configuration, either inverting or noninverting, with accuracy and speed determined by the input amplifier characteristics and the value of the holding capacitor. The electronic switch is controlled by a DTL/TTL compatible logic input.

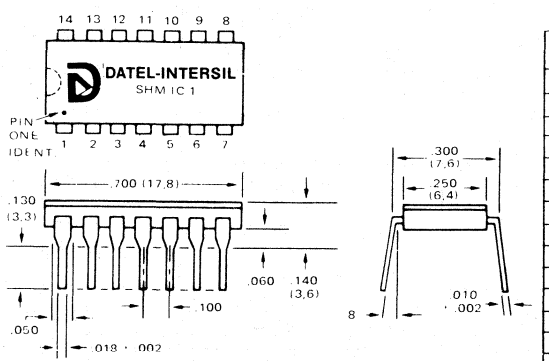
The most common configuration for the SHM-IC-1 is a unity gain, noninverting sample and hold. In this configuration the device has a ±10V input and output range with 10 ohms input impedance. Specifications are given for this unit with two different values of holding capacitor, .001μF and .01μF. The .001μF capacitor gives a 4 μsec. acquisition time to 0.1% for a 10V change, a 2MHz tracking bandwidth and 50mV/sec. maximum hold mode droop. The .01μF capacitor gives a 10 μsec. acquisition time, 1MHz tracking bandwidth, and 5mV/sec. maximum droop. Characteristics for other values of holding capacitor can be determined from graphs which are shown. The SHM-IC-1 can also be configured as either an inverting or noninverting sample and hold with gain by the use of two external resistors.

This device is housed in a 14-pin hermetically sealed dual-in-line package. Operating temperature range is 0°C to +70°C for the SHM-IC-1 and −55°C to +125°C for the SHM-IC-1M.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−IN
2	+IN
3	OFFSET TRIM
4	OFFSET TRIM
5	−15VDC POWER
6	NO CONNECTION
7	OUTPUT
8	CASE
9	+15VDC POWER
10	GUARD
11	HOLD CAPACITOR (C_H)
12	GUARD
13	GROUND
14	DIGITAL CONTROL

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SHM-IC-1

(Typical at 25°C, ±15V Supplies, unless otherwise noted)

INPUT AMPLIFIER SPECIFICATIONS	
DC Gain, volts/volt[1]	50K, 25K min.
Bias Current	50nA, 200nA max.
Offset Current	10nA, 50nA max.
Offset Voltage (adjust. to zero)	3mV, 6mV max.
Offset Voltage Drift	20 μV/°C
Common Mode Voltage Range	±10V min.
Common Mode Rejection Ratio	74dB min.
Power Supply Rejection	±30μV/% max.
Gain Bandwidth Product	2MHz
GENERAL SPECIFICATIONS, SAMPLE & HOLD, G = +1	
Input Voltage Range	±10V min.
Input Impedance	10^6 ohms
Output Voltage Range	±10V min.
Output Current, S.C. protected	±10mA min.
Output Impedance	0.2 ohm
Aperture Delay	50 nsec.
Aperture Uncertainty	5 nsec.
Gain Error, sampling mode	.01% max.
Hold Mode Noise	350μV RMS
Digital Input, Sample Mode, DTL/TTL	0 to +0.8V @ −0.8mA
Hold Mode, DTL/TTL[2]	+2.0 to +5.5V @ +20μA
SAMPLE & HOLD, G = +1, C_H = .001μF	
Acquisition Time, 10V to 0.1%	4 μsec.
Acquisition Time, 10V to .01%	5 μsec.
Bandwidth, small signal, sampling	2.0MHz
Slew Rate	5V/μsec.
Hold Mode Voltage Droop	50mV/sec. max.
Hold Mode Feedthrough	.01% max.
Sample-to-Hold Offset Error, V_{IN} = 0	20mV max.
Sample-to-Hold Gain Error, V_{IN} = ±10V	.05% max. of output
Sample-to-Hold Nonlinearity Error	.01% max. of output
SAMPLE & HOLD, G = +1, C_H = .01μF	
Acquisition Time, 10V to 0.1%	10 μsec.
Acquisition Time, 10V to .01%	12 μsec.
Bandwidth, small signal, sampling	1.0MHz
Slew Rate	3V/μsec.
Hold Mode Voltage Droop	5mV/sec. max.
Hold Mode Feedthrough	.002% max.
Sample-to-Hold Offset Error, V_{IN} = 0	2mV max.
Sample-to-Hold Gain Error, V_{IN} = ±10V	.005% max.
Sample-to-Hold Nonlinearity Error	.001% max.
POWER REQUIREMENT	±15VDC @ 5mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range, SHM-IC-1	0°C to 70°C
Operating Temperature Range, SHM-IC-1M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package, hermetically sealed ceramic DIP	TO-116

NOTES: 1. 40K and 20K respectively at +125°C for SHM-IC-1M.
2. +3.0 to +5.5V at −55°C for SHM-IC-1M.

TECHNICAL NOTES

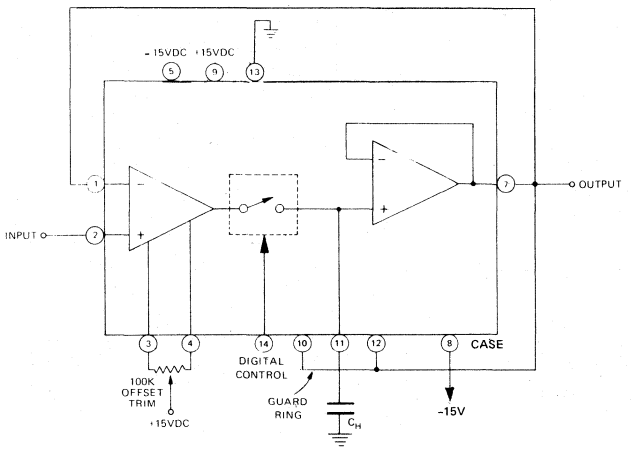
The most commonly used sample and hold configuration for the SHM-IC is the noninverting unity gain circuit. This gives a high input impedance of 10^8 ohms, and the output voltage in the sample mode follows the input. Specifications are given for this configuration for two values of C_H, .001μF and .01μF. The .001μF capacitor gives excellent speed (4 μsec. acquisition) with good hold mode voltage droop (only 50mV/sec. max). For even better speed, a 100 pF capacitor may be used to give an acquisition time of only 2 μsec. The hold mode droop, however, increases by an order of magnitude to 500mV/sec., and the sample-to-hold errors also increase. For excellent accuracy a .01 μF capacitor should be used, giving an acquisition time of 10 μsec., and a hold mode droop of only 5mV/sec. max. Even larger values of holding capacitor can be used with proportionate increases in accuracy but slower speed. The application graphs show the results for the different values.

For best results, C_H should be a good quality capacitor with very high insulation resistance and low dielectric absorption. For temperatures up to +85°C polystyrene type capacitors are recommended. It is also recommended for lowest hold mode droop that a guard ring be used around the C_H terminal (pin 11) in the circuit board layout as shown on the last page. This is done to prevent leakage to other conductors on the circuit board due to board leakage and contamination. If a large value polystyrene capacitor is used, such as 1μF, hold mode droop as low as 20μV/sec. (typical) can be achieved with an acquisition time of about 3 milliseconds.

Three error contributions are specified for sample-to-hold errors: offset error, gain error, and nonlinearity error. These sampling errors are caused by a small amount of charge being dumped to or from the holding capacitor by the sampling switch and are reduced by a larger value of C_H. It is possible to compensate for these errors by changing the gain and offset elsewhere in the external circuitry for the noninverting unity gain case. For the inverting case, the gain can be accomplished by adjusting the external resistor values and an offset can be applied to pin 2 of the input amplifier. When this external compensation is used, the output will be in error during sampling, but will be accurate in the hold mode. Only the nonlinearity error will remain of the sample-to-hold errors. The offset adjustment of the input amplifiers should be used only to zero the device in the sample mode.

In the inverting gain of one operating mode, the feedback and input resistors should be carefully matched or trimmed to give the desired gain of one. In general, the operating parameters are the same as in the noninverting unity gain configuration except that the sampling bandwidth is reduced by a factor of two. Likewise, for higher gain configurations the sampling bandwidth is proportionately reduced.

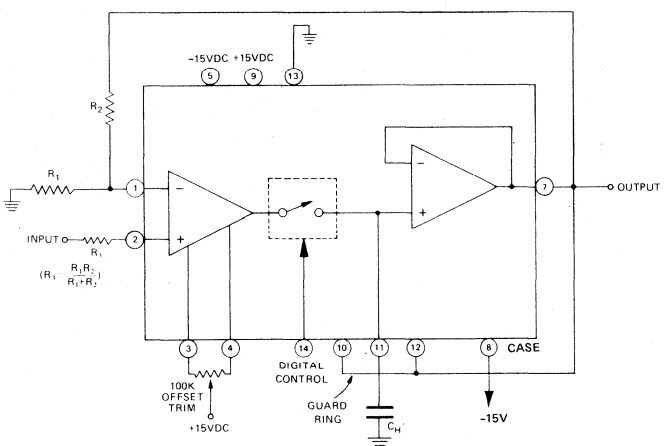
OPERATING MODES



SAMPLE & HOLD, UNITY GAIN, NONINVERTING

GAIN = +1

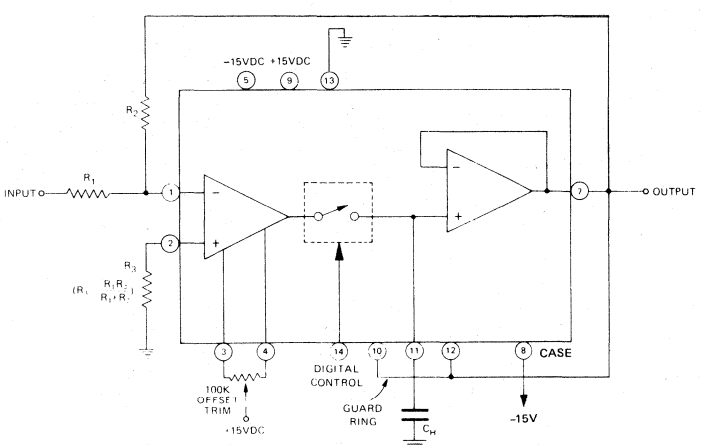
The 100K ohm offset trimming potentiometer should be a 100 ppm/°C cermet 15 turn type. These are available from Datel-Intersil at $3.50 each. To zero, ground input (pin 2) and digital control (pin 14) and adjust 100K offset trim for zero output (pin 7).



SAMPLE & HOLD, NONINVERTING WITH GAIN

$$\text{GAIN} = 1 + \frac{R_2}{R_1}$$

Bandwidth decreases proportionately with gain. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be 100 ppm/°C metal film type resistors.



SAMPLE & HOLD, INVERTING

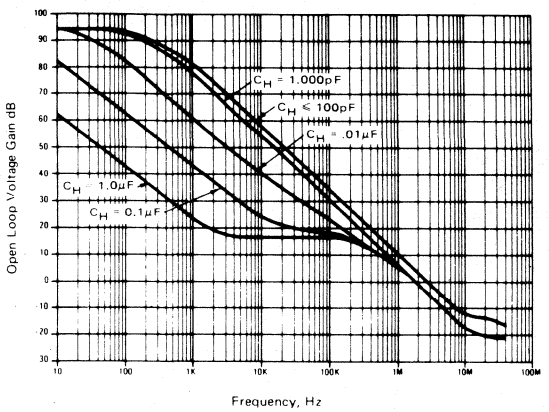
$$\text{GAIN} = -\frac{R_2}{R_1}$$

For a gain of −1 the bandwidth is one half of that given for the noninverting mode. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be matched 100 ppm/°C metal film type resistors for a gain of −1. For higher gains the ratio should be matched closely or trimmed with a small value carbon composition type resistor.

PERFORMANCE PARAMETERS

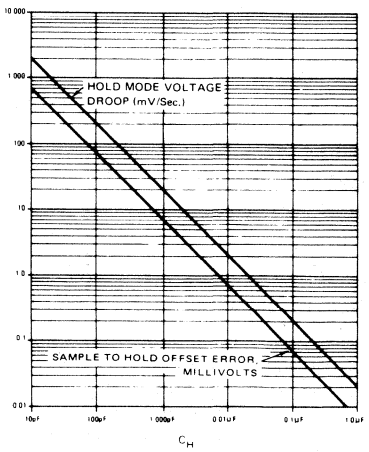
OPEN LOOP FREQUENCY RESPONSE

Typical at 25°C, ±15V Supplies



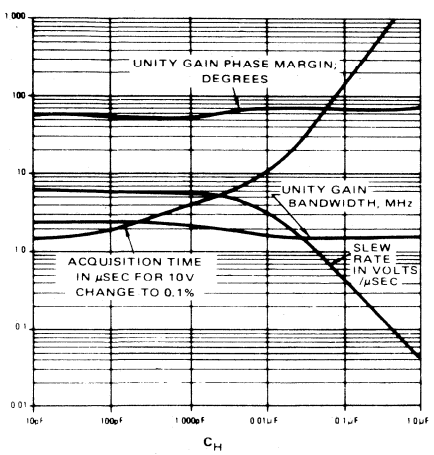
ACCURACY CHARACTERISTICS VS. C_H

Typical at 25°C, ±15V Supplies



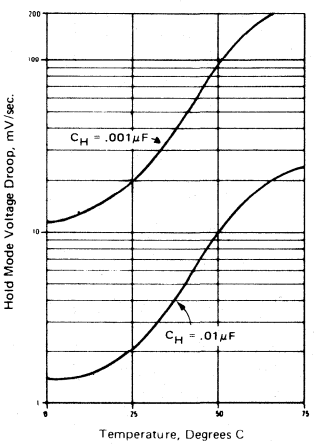
SPEED CHARACTERISTICS VS. C_H

Typical at 25°C, ±15V Supplies

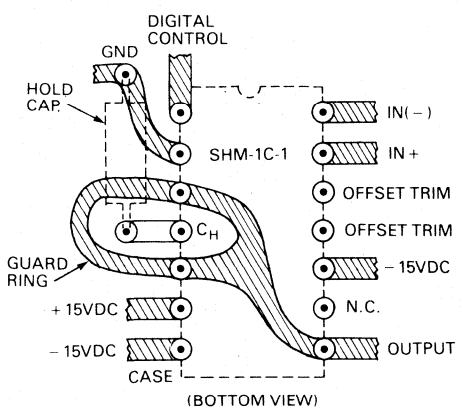


HOLD MODE VOLTAGE DROOP VS. TEMPERATURE

Typical, ±15V Supplies



RECOMMENDED CIRCUIT BOARD LAYOUT USING GUARD RING



ORDERING INFORMATION

PRICE (1-24)

Model SHM-IC-1
Model SHM-IC-1M
Trimming Potentiometer
TP100K (100KΩ)

Contact Factory for Quantity Pricing

The SHM-IC-1 is covered under GSA Contract

DATEL INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

Ultra-Fast, 0.1% Microelectronic Sample-Hold SHM-HU

FEATURES

- **25 nsec Acquisition Time**
- **50 MHz Bandwidth**
- **10 psec Aperture Uncertainty**
- **Up to 8 Bit Accuracy**
- **± 2.5V Input Range**

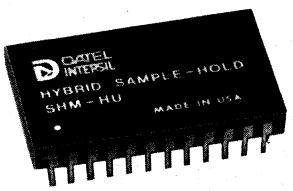
GENERAL DESCRIPTION

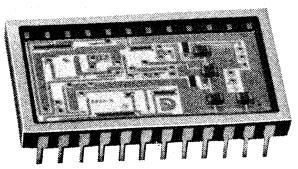
The SHM-HU is an ultra high speed sample-hold capable of video speed signal processing. The SHM-HU acquires a full scale 5V input change in just 25 nsec. and features a 10 psec aperture uncertainty time Bandwidth is 50 MHz and the slew rate is 200V/μsec.

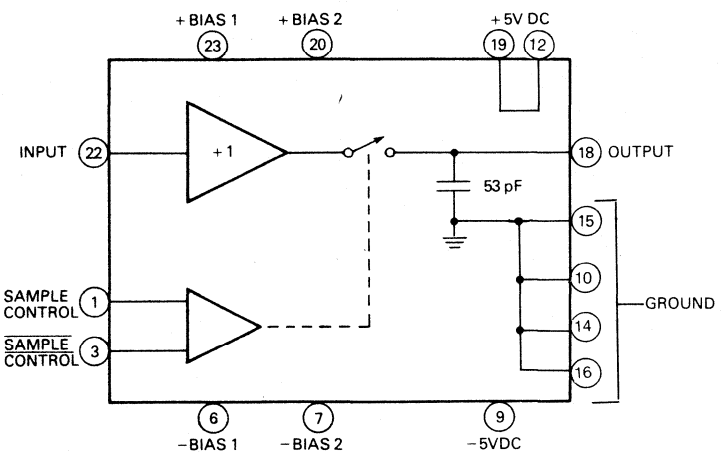
Through the use of thin film hybrid construction, this ultra high speed circuit is contained in a miniature 24-pin ceramic package. A 53 picofarad MOS hold capacitor is incorporated inside the package and provision is made for externally added capacitance when necessary. The sample-hold requires four external resistors and an LH0033 fast buffer amplifier for completion. The circuit is zeroed by adjustment of the LH0033 amplifier.

Other features of this unit include a ± 2.5V input/output voltage range and a fixed gain of 0.955. The sampling switch is controlled by a complementary series 10,000 ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

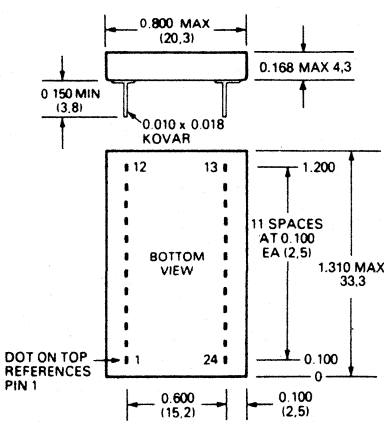
Power requirements are ± 15 VDC at 60 mA and ± 5 VDC at 70 mA. There are three basic models covering three operating temperature ranges, 0 to + 70°C, − 25 to + 85°C and − 55 to + 100°C. For high reliability versions of the SHM-HU, including MIL-STD-883 level B, contact the factory.







MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
3	$\overline{\text{SAMPLE CONTROL}}$
6	−BIAS 1
7	−BIAS 2
9	−5V POWER
15	GROUND
18	OUTPUT
19	+5V POWER
20	+BIAS 2
22	INPUT
23	+BIAS 1

NOTE: ALL OTHER PINS ARE NO CONNECTION

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, SHM-HU

(Typical at 25°C, ±15V and ±5V supplies with external LH0033 Buffer Amp. unless otherwise noted)

MAXIMUM RATINGS

Power Supplies, Pins 9-19	±6V
Analog Input Volatage, Pin 22	±5V
Sample Inputs, Pins 1 & 3	±5V Differential
Current, Pins 6, 7, 20, 23,	50 mA

INPUTS

Input Voltage Range, Min	±2.5V
Input Bias Current	25μA
Maximum Source Impedance	51 Ohms
Input Impedance	10^6 Ohms
Sample Control Inputs[4]	Differential ECL 10,000 Positive Pulse on Pin 1 and Negative Pulse on Pin 2 gives Sample Mode

OUTPUT[1]

Output Voltage Range, Min.	±2.5V
Output Current	±10 mA
Output Impedance	6 Ohms

PERFORMANCE

Accuracy	0.1%
Gain	+0.955
Output Offset Voltage[2], Sample Mode	±100 mV max.
Output Offset Voltage Drift	±100 μV/°C max.
Sample to Hold Offset Error	±100 mV max.
Hold Mode Droop	50 μV/μ sec.
Hold Mode Feedthrough	0.02%

DYNAMIC RESPONSE

Acquisition Time, 5V Step to 0.2%	25 nsec.
Bandwidth, -3 dB, Sample Mode	50 MHz
Slew Rate	200V/μsec.
Aperture Delay Time	6 nsec.
Aperture Uncertainty Time	10 psec.

POWER REQUIREMENTS[3]

±15 VDC ±0.75V @ 60 mA
±5 VDC ±0.25V @ 70 mA

PHYSICAL ENVIRONMENTAL

Operating Temperature Ranges	
SHM-HU, MC	0 to +70°C
SHM-HUMR	-25 to +85°C
SHM-HUMM	-55 to +100°C
Storage Temperature Range	-65 to +150°C
Package Type	24 Pin Ceramic
Pins	.010 x .018 Inch Kovar
Weight	0.2 Oz (6 g)

NOTES

1. Output is from LH0033 amplifier and is not short circuit proof.
2. Output offset voltage adjustable to zero by LH0033 offset adjustment.
3. ±12V supplies can be used if the 360 ohm resistors at the Bias 1 pins are changed to 240 ohms and the 240 ohm resistors at the Bias 2 pins are changed to 160 ohms.
4. The SHM-HU can be driven by TTL logic input by biasing $\overline{\text{SAMPLE}}$ CONTROL input to +1.2V and driving the SAMPLE CONTROL with a positive pulse for sample mode.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
SHM-HUMC	0 to +70°C
SHM-HMUR	−25 to +85°C
SHM-HUMM	−55 to +100°C

Mating Socket: DILS-3 (24-Pin Socket)
Trimming Potentiometer: TP100 (100 ohms)

For high reliability versions of the SHM-HU, including MIL-STD-883 level B, contact factory.

THE SHM-HU IS COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. It is recommended that the ±5V supplies of the SHM-HU be bypassed with 0.1 μF ceramic capacitors as close as possible to pins 9 and 19. The ±15V supplies to the LH0033 should be bypassed with the same value capacitors.

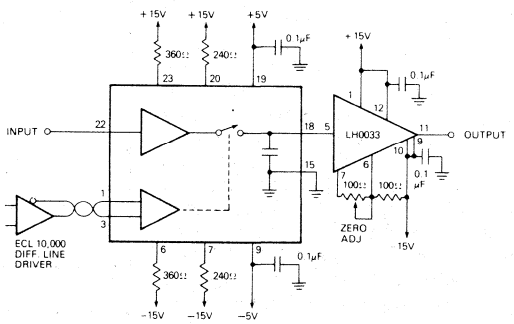
2. It is essential that the output lead from pin 18 to pin 5 of the LH0033 be kept as short and direct as possible. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.

3. With models SHM-HUMC and SHM-HUMR, the LH0033C should be used, and with model SHM-HUMM, model LH0033 should be used.

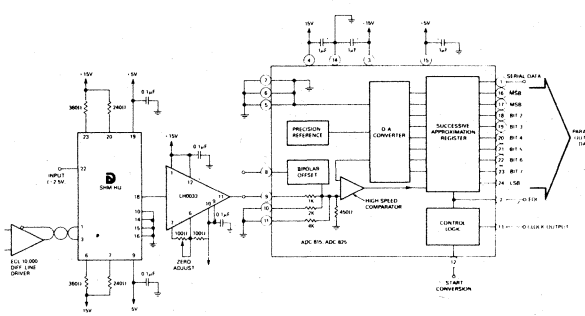
4. An external hold capacitor may be added from pin 18 to pin 15. This capacitor should be an MOS or polystyrene type. Hold mode droop and sample-to-hold offset error will decrease proportionately with the size of this capacitor and acquisition time will increase proportionately.

5. The SHM-HU can be used with model ADC-HZ12B to realize a fast 4 μsec A/D converter with sample-hold. The ultra high speed of the SHM-HU will add negligibly to the conversion time. The ADC-HZ12B in this configuration is connected for ±2.5V input and has its output coding short cycled to 8 bits instead of 12.

CONNECTION DIAGRAM



CONNECTION TO DATEL SYSTEMS ADC-815



Low Cost Monolithic Sample-Hold SHM-LM-2

FEATURES

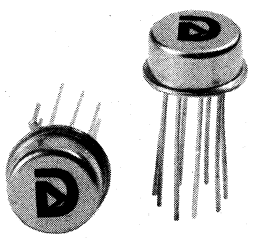
- **5 μsec. Acquisition Time**
- **.01% Gain Accuracy**
- **TTL/CMOS Logic Compatible**
- **±5V to ±18V Supplies**
- **TO-99 Package**
- **Low Cost**

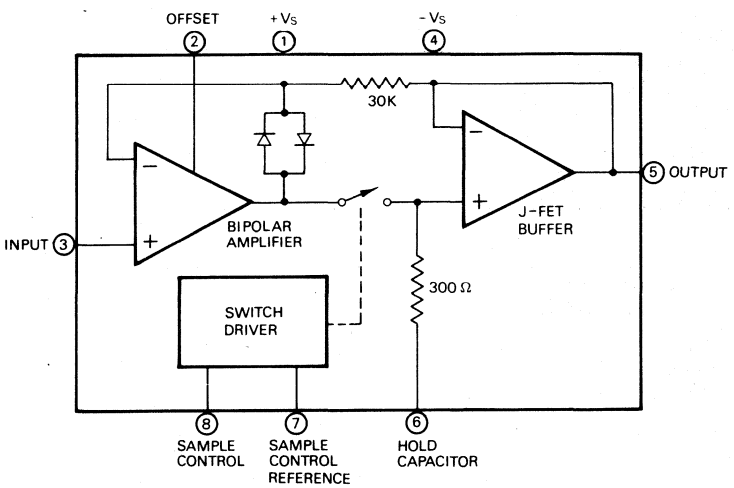
GENERAL DESCRIPTION

The SHM-LM-2 is a low cost monolithic sample-hold circuit with excellent performance features. It is self-contained requiring only an external hold capacitor with the value selected by the user for desired speed and accuracy characteristics. Acquisition time is 6 μsec. for a 10V change to .01% using a 1000pF capacitor and 25 μsec. using a .01 μF capacitor. It is 5 μsec. and 20 μsec. respectively for a 10V change to 0.1%. This device is internally configured as a unity gain follower with a gain error of less than .01% in the sample mode.

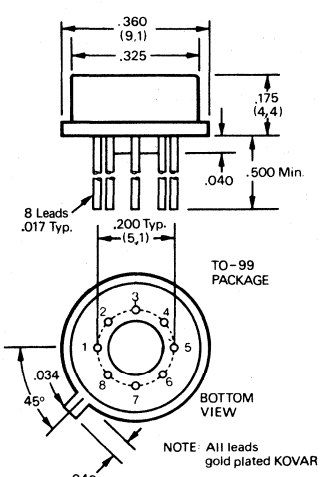
The circuit consists of a bipolar input amplifier, a low leakage electronic switch, and an FET output amplifier. The monolithic fabrication process combines P channel junction FET's with bipolar transistors to achieve a low noise, high input impedance output amplifier. Other important specifications include 10^{10} ohms input impedance and 1 MHz bandwidth. Aperture time is less than 100 nsec. and hold mode feedthrough is less than .005%. Hold mode droop is 200 μV/msec. max. with a 1000pF hold capacitor and 20 μV/msec. max. with a .01 μF capacitor. The SHM-LM-2 can operate over a power supply range of ±5V to ±18V.

Applications include sampling for A/D conversion, deglitching circuits, automatic zeroing circuits, and analog demultiplexing circuits. It is recommended that the holding capacitor (C_H) be a teflon, polystyrene, or polypropylene type for best results. Operating temperature range is 0°C to 70°C for SHM-LM-2 and -55°C to +125°C for SHM-LM-2M.





MECHANICAL DIMENSIONS
INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+ POWER SUPPLY
2	OFFSET ADJUST
3	INPUT
4	– POWER SUPPLY
5	OUTPUT
6	HOLD CAPACITOR (C_H)
7	SAMPLE CONTROL REF.
8	SAMPLE CONTROL

DATEL-INTERSIL, INC. 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 95134

SPECIFICATIONS

(Typical at 25°C, ±15V supplies and C_H = .01 μF unless otherwise stated)

MAXIMUM RATINGS	
Power Supply Voltage, pins 1 & 4	±18V
Input Voltage, pin 3	±Supply
Sample Control to Sample Reference, pin 8 to pin 7	+7, -30V
Hold Capacitor Short Circuit	10 sec.
INPUTS	
Input Voltage Range	±11.5V min.
Input Overvoltage, no damage	± Supply
Input Impedance	10^{10} ohms
Input Bias Current	10 nA typ., 50 nA max.
Sample Control	TTL or CMOS
Sample Control Input Current[1]	10 μA max.
OUTPUT	
Output Voltage Range	±11.5V min.
Output Current, S.C. protected	±5 mA
Output Impedance	0.5 ohm
PERFORMANCE	
Gain	+1.000, +0, −.01%
Output Offset Voltage, adj. to zero	±7 mV max.
Offset Voltage Drift, SHM-LM-2	20 μV/°C
Offset Voltage Drift, SHM-LM-2M	10 μV/°C[2]
Sample to Hold Offset	2.5 mV max.
Hold Mode Feedthrough	.01% max.
Power Supply Rejection Ratio	80 dB min.
Output Noise, hold mode (10Hz-100kHz)	8.5 μV RMS
Hold Mode Droop, C_H = 1000 pF	200 μV/msec. max.
C_H = .01 μF	20 μV/msec. max.
DYNAMIC RESPONSE	
Acquisition Time	
10V Change, C_H = 1000 pF	5 μsec. to 0.1%
10V Change, C_H = 1000 pF	6 μsec. to .01%
20V Change, C_H = 1000 pF	7 μsec. to 0.1%
20V Change, C_H = 1000 pF	8 μsec. to .01%
10V Change, C_H = .01 μF	20 μsec. to 0.1%
10V Change, C_H = .01 μF	25 μsec. to .01%
Aperture Delay Time	100 nsec.
Hold Mode Settling Time[3]	800 nsec.
Bandwidth, Sample Mode, −3 dB	1 MHz
POWER REQUIREMENT	
Voltage, rated performance	±15VDC
Voltage Range, operating	±5V to ±18VDC
Quiescent Current	6 mA
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range, SHM-LM-2	0°C to +70°C
SMM-LM-2M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Case	8 pin TO-99

NOTES:
1. For either Sample Control or Sample Control Reference inputs
2. 28 μV/°C max.
3. The time for the output to settle within 1 mV of final value after the logic command to switch into hold mode.

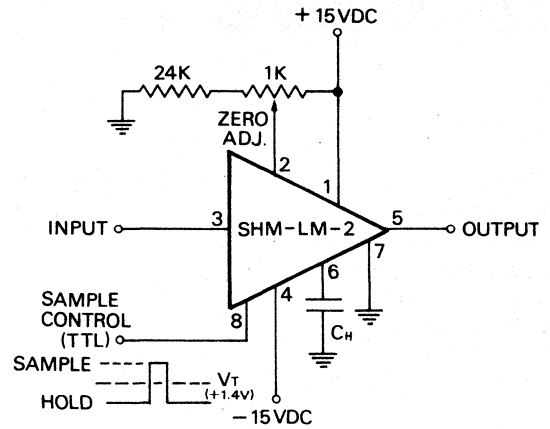
ORDERING INFORMATION

Model	Operating Temp. Range
SHM-LM-2	0°C to 70°C
SHM-LM-2M	-55°C to +125°C

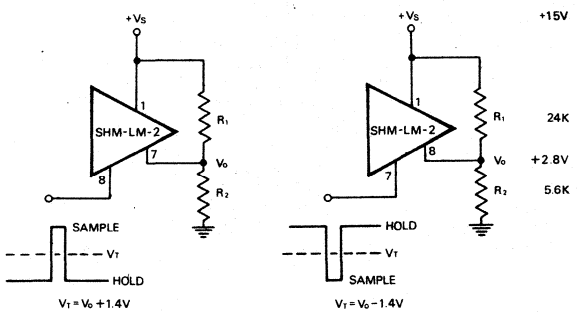
Trimming Potentiometer, TP1K

THE SHM-LM-2 IS COVERED BY GSA CONTRACT

CONNECTION DIAGRAM



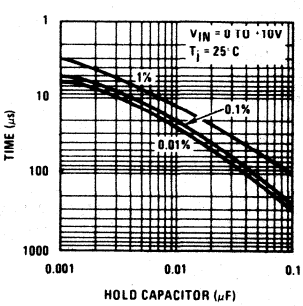
SAMPLE-CONTROL CONNECTIONS



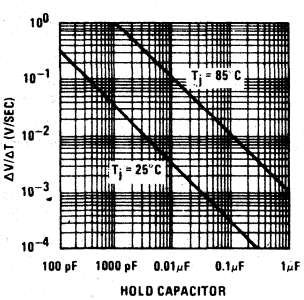
For TTL connect pin 7 to ground.

For TTL use values shown on right.

ACQUISITION TIME



HOLD MODE DROOP



TECHNICAL NOTES

1. The sample to hold offset can be adversely affected by stray capacitive coupling from input sample control signals to the hold capacitor. It is recommended that a guard ring connected to the output be put around pin 6 in a circuit board layout in order to minimize this effect.
2. For various types of logic inputs the logic threshold (V_T) is set by two biasing resistors as shown in the diagram. Inverted or non-inverted pulses may be used by using either pin 7 or pin 8 as the sample control input.

Ultra-High Speed Sample-Holds SHM-UH Series

FEATURES

- **10 MHz Sampling Rate**
- **30 nsec Acquisition Time**
- **30 psec Aperture Uncertainty**
- **Diode Bridge Switch**
- **45 MHz Bandwidth**

GENERAL DESCRIPTION

The SHM-UH series is comprised of two ultra-fast sample-holds specifically designed for use with ultra-fast 6, 8 and 10 bit A/D converters. Both models in this series use an open loop design optimized for ultra-high speed operation. This design consists of an ultra-fast input buffer amplifier, a transformer driven diode bridge switch, and a high impedance output buffer amplifier.

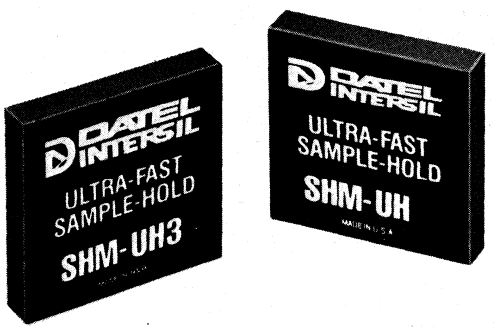
The unique pulse transformer driven diode bridge switch is a key design feature in attaining a 30 nsec. acquisition time for a 10V signal change. This switch also holds aperture uncertainty time to less than 30 picoseconds for the SHM-UH3 and less than 200 picoseconds for the SHM-UH.

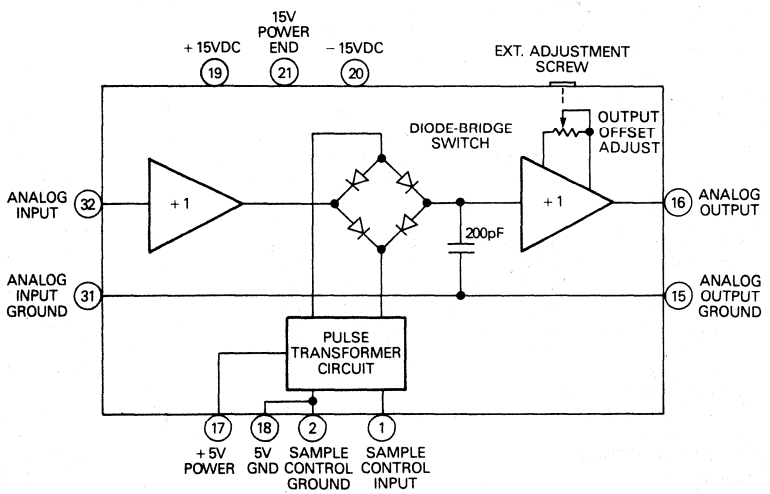
The SHM-UH3 is the newest member of this series and embodies substantial performance improvements on an already high performance design. This model is recommended for inclusion in new design applications. In addition to a 30 nsec acquisition time with only 30 picoseconds of aperture uncertainty, linearity is 0.05% of full scale and hold-mode feedthrough is −66 dB for inputs from DC to 10 MHz. The SHM-UH3 utilizes all hermetically sealed semiconductors in its design.

The SHM-UH is the lower cost version of the series. An acquisition time of 50 nsec, aperture uncertainty of less than 200 picoseconds, and linearity of 0.25% make this model well suited to use with ultra-high speed A/D converters with up to 8 bits resolution.

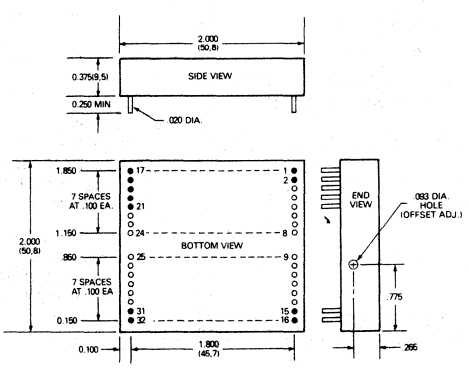
Both models have sample-mode bandwidths of 45 MHz, output slew rates of 500V/μsec and output current drive capabilities of ±30 mA. Each has an output offset adjustment accessible from the side of the module.

These sample-holds are encapsulated in 2 × 2 × 0.375 inch (51 × 51 × 5 mm) cases with dual-in-line pinning compatibility. Power requirements are ±15 VDC and +5 VDC. Standard versions operate over a temperature range of 0 to +70°C with extended temperature range versions also available.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL IN
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	+5V POWER
18	5V POWER GND
19	+15V POWER
20	−15V POWER
21	15V POWER GND
31	ANALOG INPUT GND
32	ANALOG INPUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SHM-UH SERIES
(Typical at 25°C and ±15 VDC and +5 VDC Supplies, unless otherwise noted)

	SHM-UH	SHM-UH3
MAXIMUM RATINGS[1]		
Analog Input Voltage	±15V	±5.5V
Sample Control Input Voltage	+5.5V	+5.5V
Sample Pulse Width[7]	70 nsec	100 nsec
Analog Supply Voltage	±18V	±18V
Digital Supply Voltage	+5.5V	+5.5V
INPUTS		
Input Voltage Range	±5V	±5V
Input Impedance	100 Meg	100k
Input Bias Current	50 pA[2]	±20 μA
Sample Control Pulse	+5V @ 130 mA	+3.5 @ 60 mA
Sample Control Pulse Width	40 ±10 nsec.	35 ±10 nsec.
Sample Control Input Impedance	50Ω	50Ω
Sample Pulse Rise or Fall Time	3 nsec, max.	3 nsec, max.
OUTPUTS		
Output Voltage Range, min.	±5V	±5V
Output Current, max.	±30 mA	±30 mA
Output Impedance, DC	3Ω	3Ω
Output Load[3]	500Ω	500Ω
Maximum Capacitive Load	100 pF	100 pF
PERFORMANCE		
Gain	+0.92 to +0.95	+0.95 to +0.98
Linearity Error, % of Full Scale	±0.25%, max.[9]	±0.05%, max.
Output Offset Voltage, Hold Mode	Adj. to Zero	Adj. to Zero
Output Offset Voltage Drift	±50 μV/°C	±50 μV/°C
Hold Mode Droop	50 μV/μsec	50 μV/μsec
Hold Mode Feedthrough[4]	-50 dB @ 10 MHz	-66 dB, DC to 10 MHz
Analog Supply Rejection	6 mV/V	25 mV/V
DYNAMIC RESPONSE		
Acquisition Time	50 nsec[5]	30 nsec
Acquisition to Output Time[11]	70 nsec	50 nsec
Hold Mode Settling Time	20 nsec	20 nsec
Bandwidth, Sample Mode	45 MHz	45 MHz
Output Slew Rate	500V/μsec	500V/μsec
Aperture Delay Time	12 nsec[6]	12 nsec[8]
Aperture Uncertainty Time	200 psec	30 psec
Sampling Rate, max.	10 MHz[10]	10 MHz[10]

POWER REQUIREMENT	
Analog Power Supply	±15 VDC ±0.2 VDC @ 50 mA
Digital Power Supply	+5 VDC ±0.25 VDC @ 100 mA
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	-55°C to +85°C
Relative Humidity	Up to 100% Non-condensing
Case Size	2 × 2 × 0.375 inches (50,8 × 50,8 × 9,5 mm)
Case Material	Black Diallyl Phthalate, per MIL-M-14
Pins	0.020" Dia, Gold Plated 0.25" Long, min.
Weight	3 oz. (85g)

NOTES:
1. Maximum ratings represent the limits of device operation without damage. The devices should not be operated at these limits.
2. 150 pA max @ 25°C. Doubles every 10°C (SHM-UH Only).
3. For full scale signal outputs. For small signal outputs (±1V), output load resistance must be decreased to 100Ω.
4. See Feedthrough Attenuation Graph.
5. Model SHM-UH requires three sampling pulses to acquire a full scale signal change.
6. For the SHM-UH this will vary by ±2 nsec max. with temperature.
7. See Technical Note 10.
8. This may vary between units by 3 nsec.
9. For input signal changes of ±1.25V max., larger input signal changes require additional sample pulses and settling time. See Technical Note 9.
10. 30 nsec sampling pulses with 70 nsec between pulses.
11. See Technical Note 4.

TECHNICAL NOTES

1. These devices are true sample-holds, rather than track and holds, in that they take an "instantaneous" sample of the input signal rather than continuously track it and hold on command. The extremely high speed available with this series allows a close approximation to sampling period of the ideal zero-order hold. Design considerations necessary to attain this level of performance place a limit on long-term holding ability. A/D converters used with these sample-holds should be selected for compatible speed and accuracy.

2. Aperture uncertainty time is a measurement of the time uncertainty or jitter of the actual point in time of the switch change to the off state. It is an indication of the repeatability of the switch characteristics. This time should not be confused with the aperture delay time which is a fixed delay and can be compensated for.

3. Acquisition time is the time required, after the sampling switch is closed, for the hold capacitor to charge to a full scale voltage change and remain within a specified error band around the final value.

4. Acquisition to output time is defined as the period from the receipt of the sample command until the output of the sample-hold has settled to within a specified error band of its final value. This is the operating period of the sample-hold, including all internal delays and settling time, and consequently defines the total time required for a single sample-hold operation.

5. Digital and analog grounds are not connected internally. When using these sample-holds with A/D converters, good design practice dictates the connection of analog and digital grounds from both devices at one point, preferably at the A/D converter to avoid ground loops. Use of a ground plane is recommended for best performance.

6. For Model SHM-UH only, hold mode droop is from the held value of the analog input signal toward the signal level at the input. The droop experienced is also dependent on input signal characteristics and is related to the feedthrough attenuation characteristics. The combination of these factors may cause the observed hold mode voltage droop to be significantly less than 50 μV/μsec for some applications, e.g., droop is zero for a constant input signal. In the case of Model SHM-UH3, droop is independent of feedthrough.

7. For both the SHM-UH and the SHM-UH3 input sources should be purely resistive.

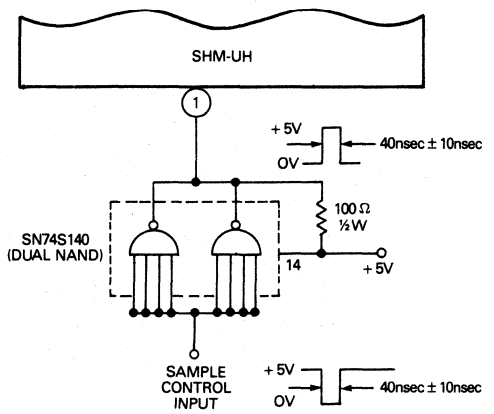
8. Input overvoltage protection may be added to the SHM-UH3 by connecting diodes from the analog input and the analog input ground to the +5V and -5V supplies, see "Input Protection" diagram.

9. To acquire full scale input signal changes, the SHM-UH requires three sampling pulses with a 100 nsec. settling time allowed between each to acquire full scale input changes to rated linearity.

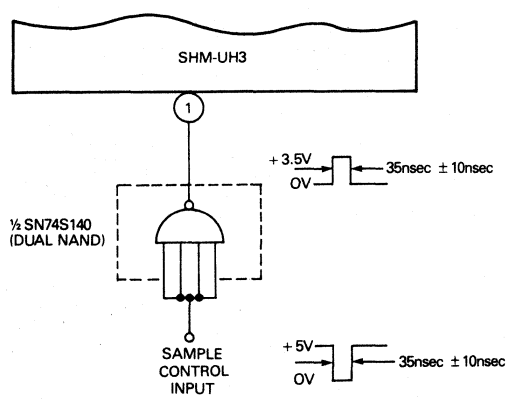
10. Sample pulse widths greater than those specified under MAXIMUM RATINGS will give unsatisfactory performance due to drive transformer saturation. For Model SHM-UH3, excessive pulse widths will result in the sample-hold returning to the hold mode before the sample control input is taken low. Model SHM-UH may be damaged by exceeding sample pulse width limits.

APPLICATION

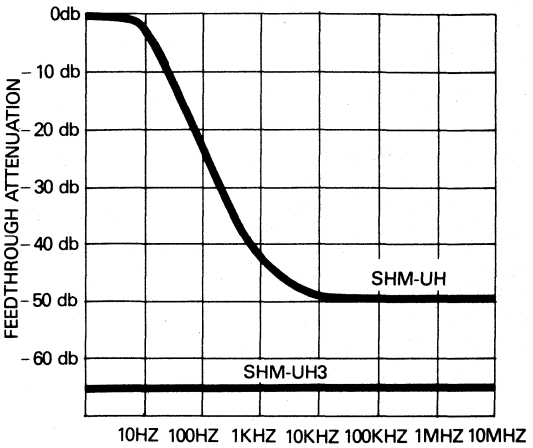
SAMPLE CONTROL INTERFACE SHM-UH



SAMPLE CONTROL INTERFACE SHM-UH3



HOLD MODE FEEDTHROUGH ATTENUATION



HOLD-MODE FEEDTHROUGH IS A PHENOMENA THAT OCCURS AFTER THE SWITCH HAS BEEN OPENED AND THE SIGNAL IS BEING HELD. A SMALL PART OF THE SIGNAL ON THE INPUT WILL BE COUPLED TO THE OUTPUT.

ORDERING INFORMATION

MODEL	DESCRIPTION
SHM-UH	50 nsec, 0.25%
SHM-UH3	30 nsec, 0.05%

Mating Socket DILS-2, 2 req'd/Module

For extended temperature range operation the following suffixes should be added to the model number. Consult Factory for Price and Delivery.

-EX	-25°C to +85°C Operation
-EXX-HS	-55°C to +85°C Operation, with all hermetically sealed semiconductor components.

THESE SAMPLE-HOLDS ARE COVERED BY GSA CONTRACT

ADJUSTMENT PROCEDURE

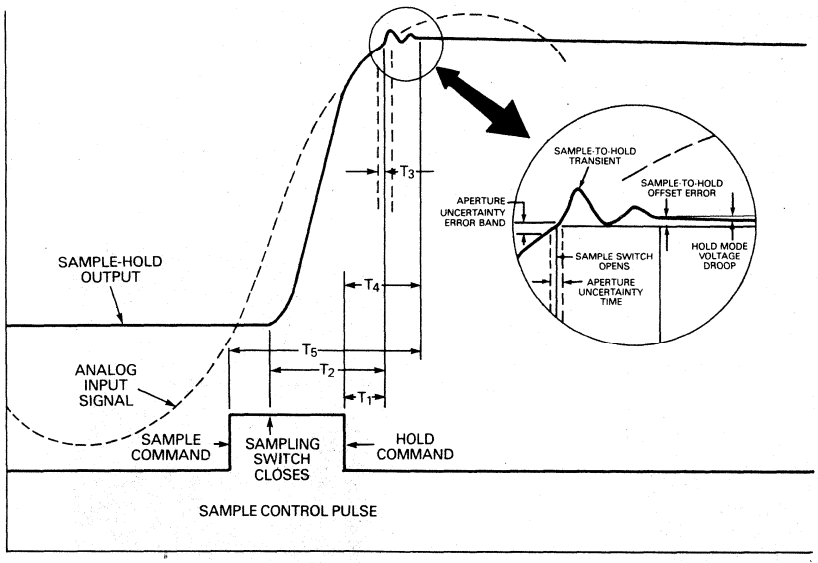
1. Connect the Analog Input (pin 32) to the Analog Input Ground (Pin 31).
2. Connect a precision pulse generator with negative going output pulses via a terminated coaxial cable to the Sample Control Input (pin 1) and the Sample Control Ground (pin 2). Use the sample control interface shown in the applicable diagram.
3.

Pulse Repetition Rate	50 KHz
Pulse Width	40 nsec
Pulse Amplitude	+5V

   Note: Sample Control Input Impedance is 50 Ohms
4. Connect a precision digital voltmeter to the Analog Output (pin 16) and the Analog Output Ground (pin 15).
5. Adjust the Offset Adjust Potentiometer (accessible through side of case) until the digital voltmeter reads 0.0000V.

APPLICATION

SAMPLE-HOLD DEFINITIONS



T_1, **APERTURE DELAY TIME**
The period between the receipt of the hold command and opening of the sampling switch. Due to sampling switch characteristics, the measurement of this period contains a small amount of uncertainty, i.e., the actual point in time of the opening of the sampling switch will vary by a small amount with each operation. This variance falls within a narrow time range which is specified as the aperture uncertainty time (see definition below).

T_2, **ACQUISITION TIME**
The time required, after the closing of the sampling switch, for the hold capacitor to charge to a full scale voltage change and then remain within a specified error band around the final value.

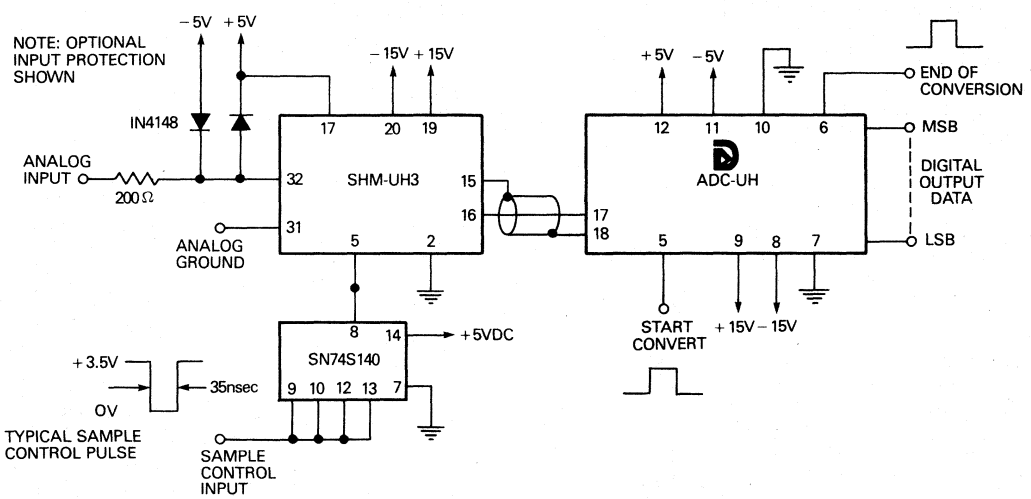
T_3, **APERTURE UNCERTAINTY TIME**
The time variation, or jitter, in the opening of the sample switch.

APERTURE UNCERTAINTY ERROR
An amplitude uncertainty in the held value due to the change in the analog input signal during the aperture uncertainty time. This error is the product of the rate of change of the input signal and the aperture uncertainty time. Therefore, small values of aperture uncertainty time yield small values of aperture uncertainty error.

T_4, **HOLD MODE SETTLING TIME**
The time from the hold command transition until the output has settled within a specified error band around the final value.

T_5, **ACQUISITION TO OUTPUT TIME**
The time from the receipt of the sample command until the output of the sample-hold has settled within a specified error band around the final value.

SHM-UH3 AND ADC-UH8B CONNECTION



Ultra-Fast, .01% Sample-Hold SHM-5

FEATURES

- **200nSec. Acquisition to 0.1%**
- **350nSec. Acquisition to .01%**
- **5MHz Bandwidth**
- **.005% Linearity**
- **250 pSec. Aperture Uncertainty**

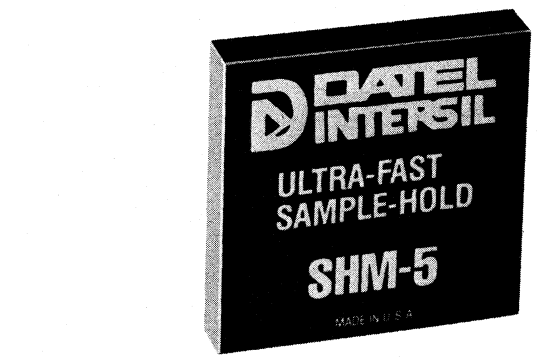
GENERAL DESCRIPTION

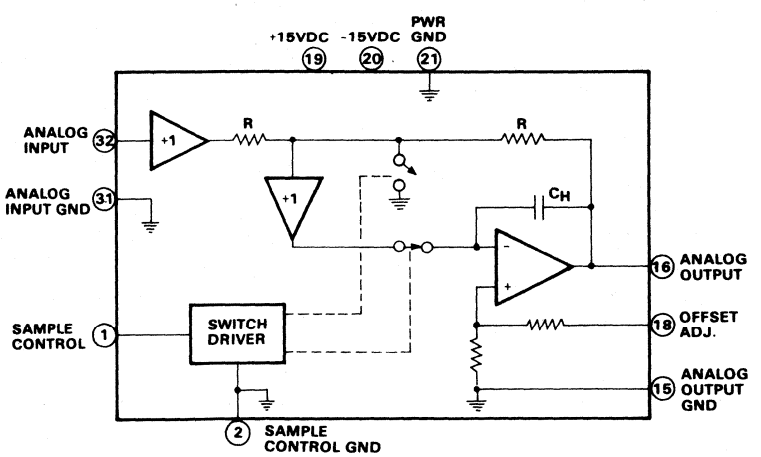
Model SHM-5 is a new, ultra-fast acquisition sample-hold module for use with high speed 10 and 12-bit A/D converters. When used with Datel-Intersil's model ADC-EH12B3, a 12-bit 2 μsec, A/D, the SHM-5 permits sampling and conversion at rates up to 425 kHz. The key circuit element in the SHM-5 is an ultra-fast settling hybrid operational amplifier manufactured in Datel's thin-film hybrid facility. This amplifier operates in the inverting mode as a hold amplifier. A fast FET sampling switch operates between two virtual ground points in order to keep switching errors small and independent of signal level. A second FET switch operates out-of-phase with the first one to minimize signal feedthrough errors.

The SHM-5 is designed primarily for fast track & hold and simultaneous sampling applications with A/D converters. From the tracking mode it realizes acquisition times of 200 nsec. to 0.1% or 350 μsec. to 0.01% for a 10V change. When the input buffer amplifier must also make a 10V change, as in multiplexer applications, the total acquisition time is 1 μsec. to 0.01%.

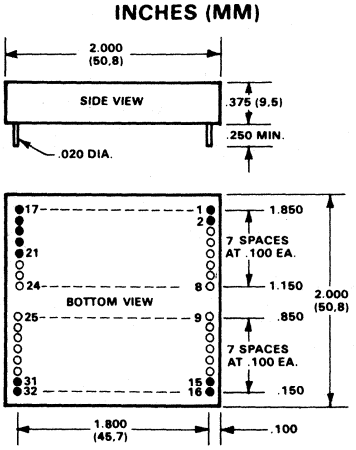
The SHM-5 operates in the inverting mode with a gain of -1 and an input impedance of 10^8 ohms. Dynamic characteristics include a 5 MHz small signal bandwidth, and 25V/μsec. slew rate in the sampling (tracking) mode. When acquiring a new sample, however, the internal slew rate across the holding capacitor is 200V/μsec. Aperture delay time is 20 nanoseconds and aperture uncertainty time is 250 picoseconds.

This device is packaged in a 2 x 2 x 0.375 inch epoxy encapsulated module. Operating temperature range is 0°C to 70°C and power requirement is ± 15VDC at 75 mA maximum. The SHM-5 is pin compatible with Datel-Intersil's model SHM-UH3.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	NO CONNECTION
18	OFFSET ADJ.
19	+15V POWER
20	-15V POWER
21	POWER GND
31	ANALOG INPUT GND
32	ANALOG INPUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SHM-5

(Typical at 25 C, ±15V supply unless otherwise noted)

INPUTS	
Input Voltage Range	±10V min.
Input Overvoltage, no damage	±15V
Input Impedance	10^8 ohms
Input Bias Current	250nA max.
Sample Control, sample mode	+2.0 to +5.5V
hold mode	0V to +0.8V
Sample Control Loading	+1mA
Offset Adjustment Range	±300mV
OUTPUT	
Output Voltage Range, min.	±10V
Output Current, S.C. protected	±40mA
Output Impedance	0.1 Ωmax.
PERFORMANCE	
Gain	-1.000±0.1%
Gain Temp. Coefficient	±15ppm/°C max.
Output Offset Voltage, sample mode	±50mV max.
Output Offset Voltage Drift	±30μV/°C max.
Sample to Hold Offset Error	±5mV max.
Tracking Nonlinearity	±.005% max.
Hold Mode Droop	20μV/μsec max.
Hold Mode Feedthrough, DC-500kHz	0.02%
Output Offset vs Supply	1mV/V
DYNAMIC RESPONSE	
Acquisition Time[1], 10V to 0.1%	200 nsec. max.
Acquisition Time[1], 10V to .01%	350 nsec. max.
Acquisition Time[2], 10V to 0.01%	1.0 μsec typ., 1.5 μsec. max.
Bandwidth, tracking, −3dB	5MHz
Slew Rate, tracking	25V/μsec.
Aperture Delay Time	20nsec.
Aperture Uncertainty Time	250 psec.
POWER REQUIREMENT	
Power Supply Voltage	±15VDC ±0.5V
Quiescent Current	75mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range	0°C to 70°C
Storage Temp. Range	−55°C to +85°C.
Relative Humidity	Up to 100% non-condensing
Case Size	2.0 X 2.0 X 0.375 in, 50,8 X 50,8 X 9,5 mm
Case Material	Black diallyl phthalate per MIL-M-14
Pins	.020" round, gold plated; .25" long min.
Weight	2 oz. (57g.)

NOTES:

1. From tracking mode.
2. From input buffer.

ORDERING INFORMATION

PRICE (1-9)

SHM-5

Mating Socket: DILS-2 (2/module)

Trimming Potentiometer, TP20K

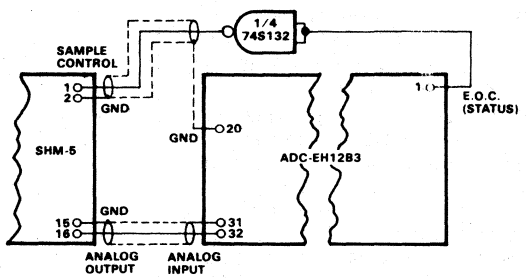
For extended temperature range operation, the following suffix is added to the model number. Consult factory for price and delivery.

−EX −25°C to +85°C operation.
−EXX-HS −55°C to +85°C with hermetically sealed semiconductor components.

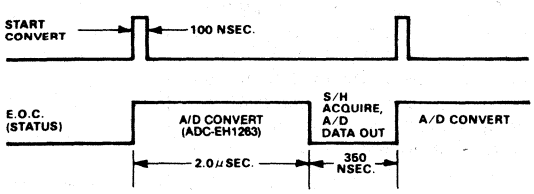
TECHNICAL NOTES

1. The SHM-5 initial gain error of ±0.1% must be adjusted out separately from the sample hold. This is most easily done by using the gain adjust of the A/D converter used with the SHM-5.
2. The maximum sample-to-hold offset error of 5mV is constant with signal level. This error can be adjusted out in the hold mode by means of the external offset adjustment shown in the diagram. It should be noted that the SHM-5 can be adjusted for zero output offset in either the sample (tracking) mode or the hold mode, but not in both at the same time.
3. The sample control input is compatible with standard TTL levels. It is recommended that this input be driven from its own active pull-up Schottky TTL circuit, such as the 74S132. This will readily supply the +1mA drive current required by the SHM-5.
4. The analog signal delay from the input of the SHM-5 to the sampling switch is approximately 32 nsec. Aperture delay is 20 nsec.
5. When the SHM-5 is switched into the hold mode, about 50 nsec. is required for the switch transient to settle. This time should be allowed for before the first A/D conversion is made.

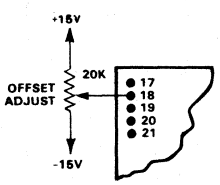
CONNECTION TO ADC-EH12B3



TIMING DIAGRAM



OFFSET ADJUSTMENT



THE SHM-5 IS COVERED BY GSA CONTRACT.

0.01%, 1.0 μ Sec. Microelectronic Sample-Hold SHM-6

FEATURES

- **0.01% Accuracy**
- **1.0 μs Acquisition Time**
- **2 nsec Aperture Uncertainty**
- **5 MHz Bandwidth**
- **25 mA Output Current**
- **Gain Programmable From ±1 to ±10**

GENERAL DESCRIPTION

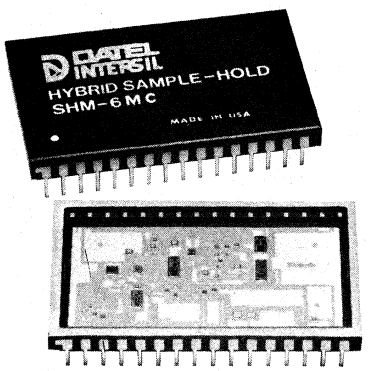
The SHM-6 is a high speed, high accuracy sample-hold circuit manufactured with thin film hybrid technology. This design offers the speed and performance of modular sample-holds with the compactness and integrity of advanced hybrid techniques. The unit's excellent high-speed characteristics include a guaranteed acquisition time of 800 nsec to 0.1% accuracy and 1.0 μsec to 0.01% for a 10 volt change.

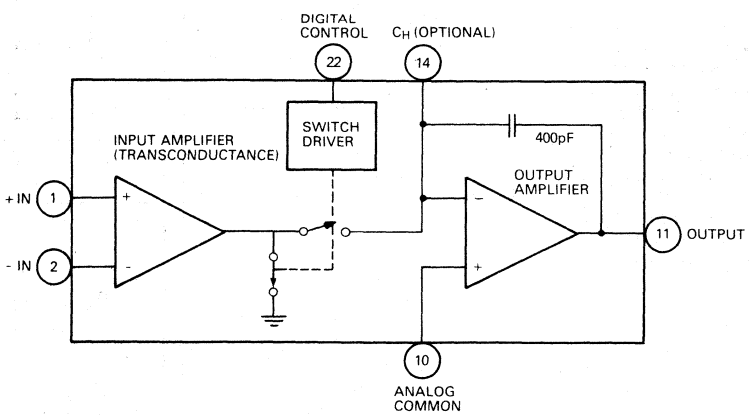
The SHM-6 is a complete sample-hold containing a precision MOS holding capacitor. The input amplifier is an open loop transductance amplifier which can be externally connected for closed loop gains from ±1 to ±10. In addition to its speed, accuracy and selectable gain, the SHM-6 has an output capability of 25 mA. These features allow this unit to offer an unusual degree of adaptability.

The most frequently utilized configuration of the SHM-6 is a unity gain, noninverting sample-hold. In this mode, the device has a ±10V input and output range with $10^8\Omega$ input resistance. Full power bandwidth is 500 KHz, and small signal tracking capability is 5 MHz. The input offset voltage and sample to hold error can be adjusted to zero with the use of two external trim pots.

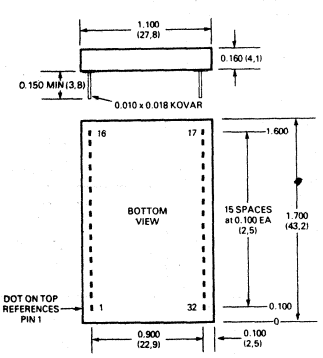
The SHM-6 is a key component in fast data acquisition systems. A 110 KHz throughput rate can be accomplished using the SHM-6 in conjunction with Datel-Intersil's ADC-HZ 12 bit A/D converter (which offers 8 μsec maximum conversion time).

The sample-hold is cased in a 32-pin ceramic package. Models are available in three operating temperature ranges: 0 to +70, −25 to +85, and −55 to +100 degrees centrigrade. High reliability versions are available processed to MIL-STD-883 level B. For further information on these, contact the factory.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STAND OFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+IN	17	S/H STEP ADJUST.
2	-IN	18	S/H STEP ADJUST.
3	NC	19	NC
4	OFFSET ADJUST.	20	NC
5	NC	21	NC
6	OFFSET ADJ. (WIPER)	22	DIGITAL CONTROL
7	NC	23	NC
8	OFFSET ADJUST.	24	+5 VDC
9	NC	25	NC
10	ANALOG COMMON	26	POWER GROUND
11	OUTPUT	27	NC
12	NC	28	+15 VDC
13	NC	29	NC
14	C.H. (OPTIONAL)	30	NC
15	NC	31	-15 VDC
16	S/H ADJ. (WIPER)	32	NC

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SHM-6

Typical at 25°C, ±15V and +5V supplies unless otherwise noted

MAXIMUM RATINGS

Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7.0V
Digital Input Voltage	+5.5V
Analog Input Voltage	±Vs
Differential Input Voltage	±30V

INPUT AMPLIFIER SPECIFICATIONS

Offset Voltage	±2 mV
Offset Voltage Tempco	±100 μV/°C
Offset Current	1 nA max.
Offset Current vs. Temp.	Doubles every 10°C
Bias Current	10 nA max.
Input Resistance	$10^8\Omega$
Common Mode Voltage Range	±10V min.
Common Mode Rejection Ratio	74 dB min.
Open Loop Gain	10^6V/V
Gain Bandwidth Product	5MHz
Power Supply Rejection Ratio	0.004%/% Supply

DIGITAL INPUT CHARACTERISTICS

Digital Control Logic	DTL, TTL
Input Logic Level, Sample Mode	0V to +0.8V @ -3.2 mA
Input Logic Level, Hold Mode	+2.0V to +5.0V @ +80μA

ANALOG OUTPUT CHARACTERISTICS

Output Voltage Range	±10V min.
Output Current	± 25 mA max.
Output Resistance	0.1Ω max.

SAMPLE HOLD CHARACTERISTICS (Noninverting unity gain)

Acquisition Time, 10V Step to 0.1%	800 nsec. max.
Acquisition Time, 10V Step to 0.01%	1 μsec. max.
Aperture Delay Time	20 nsec.
Aperture Uncertainty Time	2 nsec.
Sample to Hold Error	Adjustable to Zero
Hold Mode Voltage Droop	10 μV/μsec. max.
Hold Mode Feedthrough	0.01% max.
Offset	Adjustable to Zero
Gain	±1 to ±10
Gain Error	0.01% max.
Nonlinearity, V_{OUT} = ±10V	0.01% max.
Full Power Bandwidth, V_{OUT} = ±10V	500 KHz
Slew Rate	40V/μsec.

POWER REQUIREMENTS

Positive Supply	+15 VDC ±0.5V @ 55 mA
Negative Supply	-15 VDC ±0.5V @ 60 mA
Logic Supply	+5 VDC ±0.5V @ 30 mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Ranges	
SHM-6MC	0°C to +70°C
SHM-6MR	-25°C to +85°C
SHM-6MM	-55°C to +100°C
Storage Temperature Range	-65°C to +150°C
Package Type	32 Pin Ceramic
Pins	Kovar (.010 x .018)
Weight	0.5 Oz (14g)

TECHNICAL NOTES

1. It is essential that the +15V, -15V and +5V supplies, pins 28, 31 and 24 respectively, each be bypassed to ground with a 0.1 μF ceramic capacitor connected as close to the pins as possible.
2. Digital Common, pin 26, and Analog Common, pin 10, are not connected together internally, therefore they must be connected externally as directly as possible. It is strongly recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 10, digital ground and +5V power ground should be run to pin 26.
3. An external holding capacitor can be added to decrease hold mode voltage droop but with consequently longer acquisition time. For temperatures up to +85°C, polystyrene capacitors are recommended; for higher temperatures, polypropylene or teflon capacitors should be used.
4. In the inverting unity gain operating mode, the feedback and input resistors should be carefully matched or trimmed to yield the desired gain of one. In general, the operating parameters are the same as in the noninverting unity gain configuration, except that the sampling bandwidth is reduced by a factor of two. For applications of the SHM-6 with gain greater than one, sampling bandwidth is inversely proportional to gain.
5. Capacitive loads on the output should be limited to 100 pF to maximize acquisition time. The SHM-6 has a ± 25mA current drive capability.
6. This device dissipates approximately 2 watts of power due to the transconductance amplifier. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above +50°C, care should be taken to maintain air circulation in the vicinity of the case.
7. The adjustment procedures for the SHM-6 are as follows. Ground the input pin and connect the output to a D.V.M., operate the offset adjustment potentiometer to yield an output of zero as read on the D.V.M. The sample-hold step adjustment is performed with the input pin grounded and the output connected to an oscilloscope set to 1 mV/cm sensitivity. The digital input pin is driven with a compatible square wave at approximately 250 KHz and the sample-hold step adjustment potentiometer is operated to produce a flat-line output on the oscilloscope.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL	PRICE
SHM-6MC	0°C to +70°C	Hermetic	
SHM-6MR	-25°C to +85°C	Hermetic	
SHM-6MM	-55°C to +100°C	Hermetic	

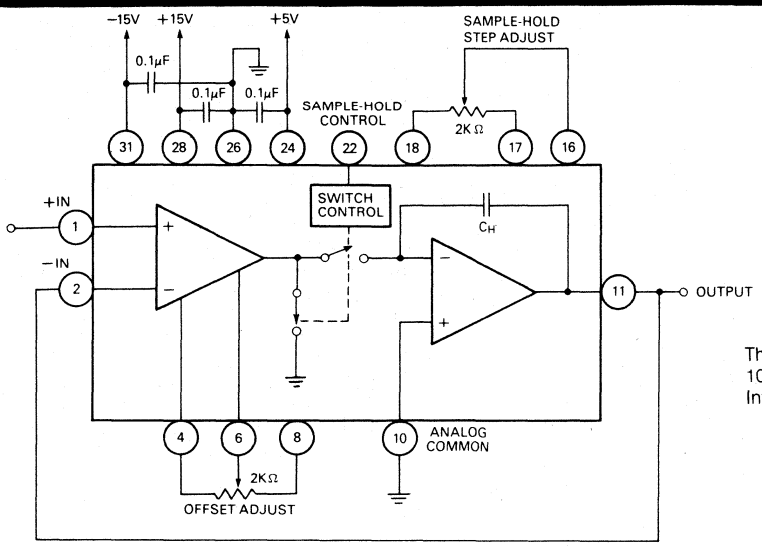
Trimming Potentiometers TP2K
(2 Required Per SHM-6)

DILS-2 Mating Socket
(2 Required Per Sample-Hold)

For High Reliability versions of the SHM-6, including units screened to MIL-STD-883, Level B, contact the factory.

THESE SAMPLE-HOLDS ARE COVERED BY GSA CONTRACT.

OPERATING MODES

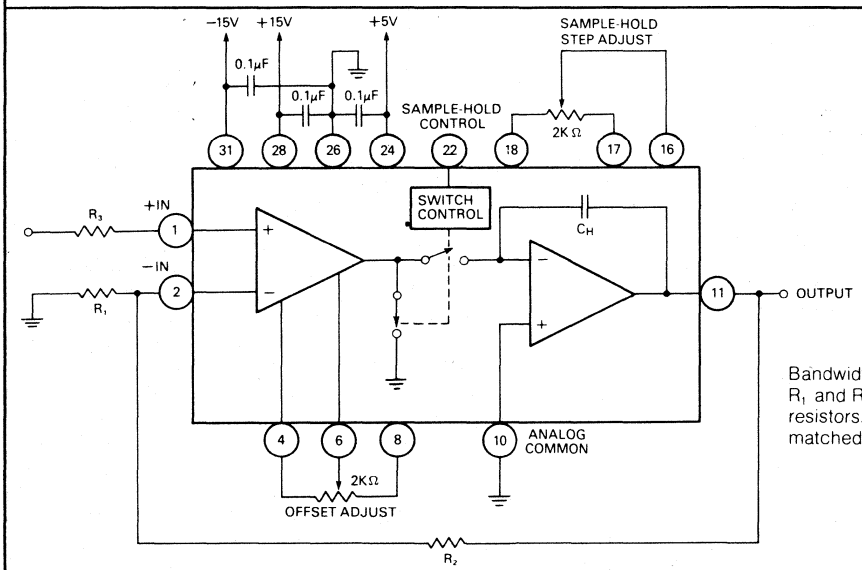


SAMPLE-HOLD

NONINVERTING

GAIN = +1

The 2KΩ offset trimming potentiometers should be of the 100PPM/°C cermet type. These are available from Datel-Intersil as model TP2K.

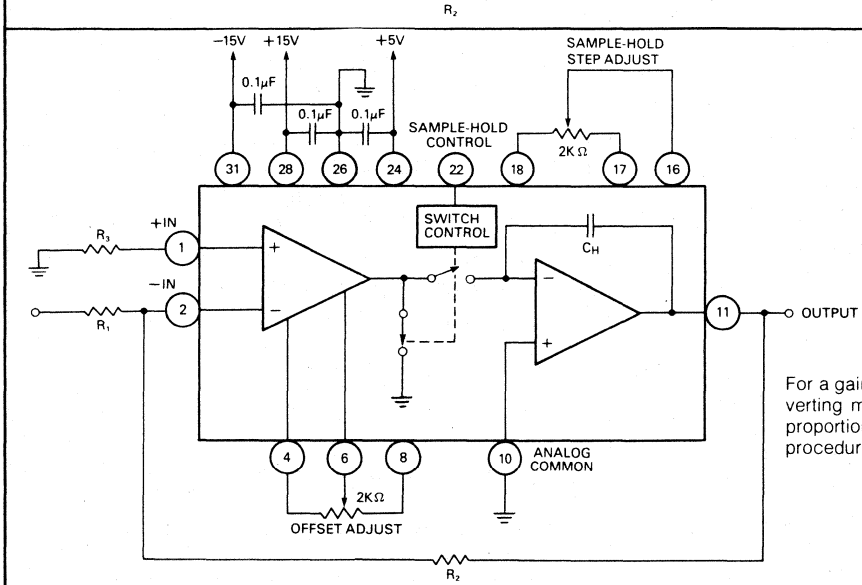


SAMPLE-HOLD

NONINVERTING

$$\textbf{GAIN} = 1 + \frac{R_2}{R_1}$$

Bandwidth decreases proportionately with gain. Resistors R_1 and R_2 should be 100PPM/°C or better, metal film type resistors. The indicated ratio between R_1 and R_2 should be matched as closely as possible and trimmed if necessary.



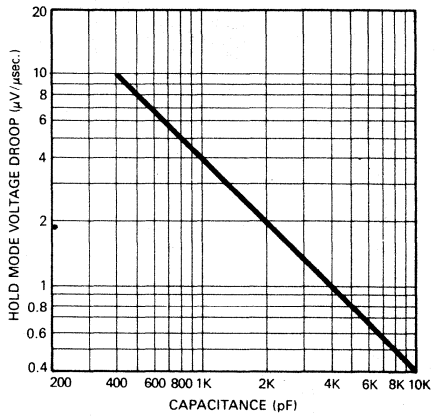
SAMPLE-HOLD

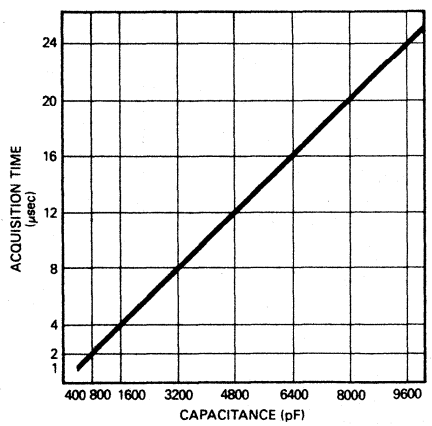
INVERTING

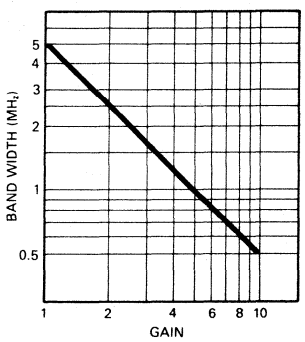
$$\textbf{GAIN} = -\frac{R_2}{R_1}$$

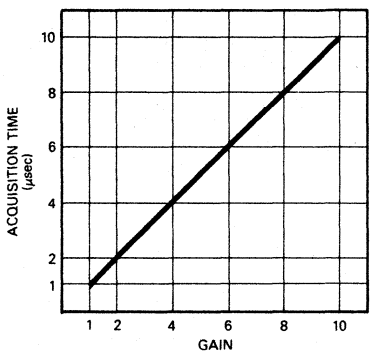
For a gain of -1 the bandwidth is one half that of the noninverting mode, for higher gains the sampling bandwidth is proportionately reduced. The above-mentioned matching procedures should be followed.

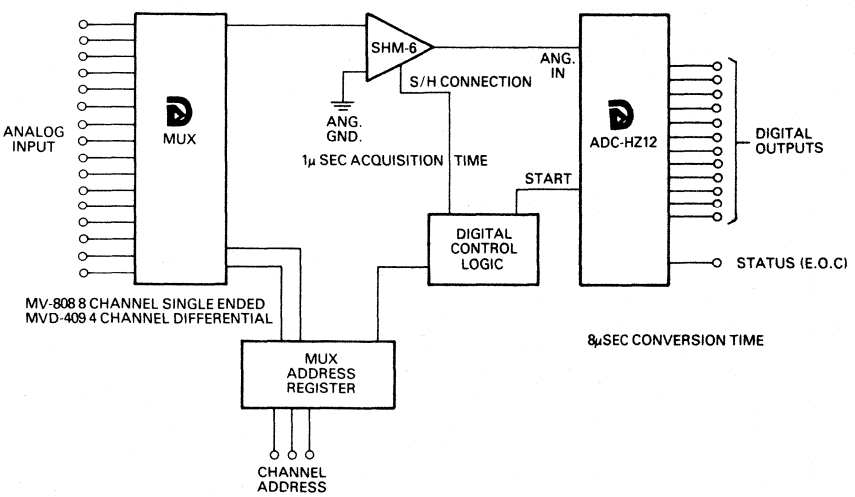
TYPICAL PERFORMANCE
(Noninverting unity gain at 25°C, ±15V and +5V supplies unless otherwise noted)











A high speed data acquisition system employing the SHM-6. This system is capable of a 110 KHz throughput rate with 12 bit resolution. In this system the SHM-6 is used with **Datel-Intersil's** ADC-HZ12, a high-speed hybrid 12 bit A/D converter, and Datel's MV-808, a low cost monolithic analog multiplexer. Use of a low on-resistance MUX is recommended, so that the time constant formed by MUX on-resistance and bus capacitance does not limit the acquisition performance of the SHM-6.

NEW DATEL

Video Speed Sample-Hold SHM-7

FEATURES

- **40 nsec Acquisition Time**
- **Dual Outputs**
- **10 psec Aperture Uncertainty**
- **40 MHz Bandwidth**
- **30 mA Output Current**

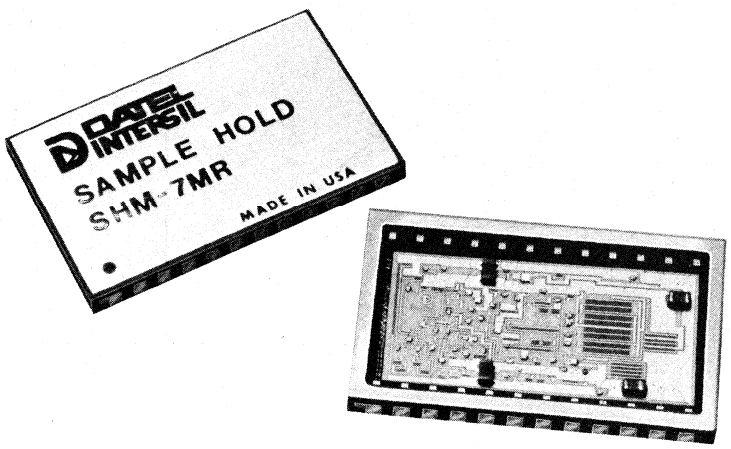
GENERAL DESCRIPTION

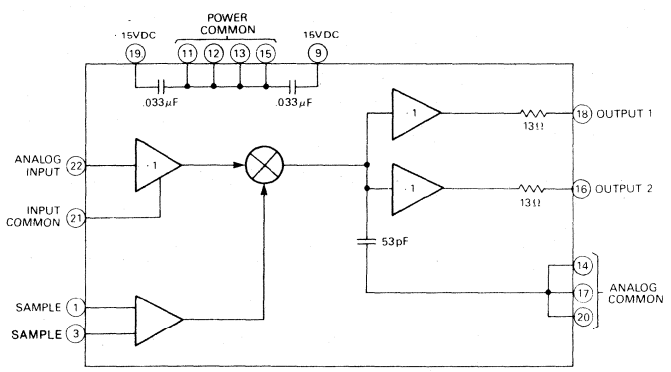
Datel-Intersil's SHM-7 is an ultra-fast sample and hold designed for high speed analog signal processing applications. The SHM-7 acquires a 2V input change to 0.1% in only 40 nsec and aperture uncertainty time is less than 10 psec. Sample-mode bandwidth is 40 MHz.

The SHM-7 is a complete Sample-Hold, containing an input buffer amplifier, a precision 53 pF MOS holding capacitor, and two output buffer amplifiers. The sampling switch is controlled by a series 10,000 complementary ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

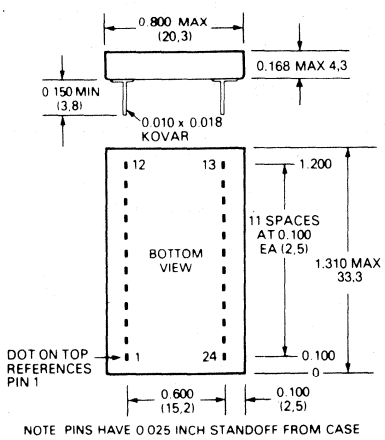
Other features of the SHM-7 include a ±5V input voltage range, a fixed gain of +0.995, and a maximum gain temperature coefficient of 33 ppm/°C. The device has two outputs, each with a ±5V output voltage swing at 30 mA and an output impedance of only 13Ω. The outputs may be tied together for decreased output impedance and increased output current. The SHM-7 is functionally laser trimmed at the factory for offset, sample to hold offset, and gain errors, and is designed to be used without external adjustment circuits.

The SHM-7 is an ideal choice for use in ultra-high speed data acquisition systems, and video processing applications, and with its dual outputs, it is especially useful in two stage flash converter systems. Power requirement is ±15 VDC at 60 mA. Two models are available for operation over the 0°C to +70°C and −25°C to +85°C operating temperature ranges. Both models are cased in a 24 pin, hermetically sealed, ceramic package.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SAMPLE	13	POWER COM.
2	N.C.	14	ANALOG COM.
3	SAMPLE	15	POWER COM.
4	N.C.	16	OUTPUT 2
5	N.C.	17	ANALOG COM.
6	N.C.	18	OUTPUT 1
7	N.C.	19	+15VDC
8	N.C.	20	ANALOG COM.
9	−15VDC	21	INPUT COM.
10	N.C.	22	ANALOG INPUT
11	POWER COM.	23	N.C.
12	POWER COM.	24	N.C.

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SPECIFICATIONS, SHM-7
(Typical at 25°C, ± 15VDC Supplies Unless Otherwise Noted)

MAXIMUM RATINGS	
Positive Supply	+ 18V
Negative Supply	− 18V
Digital Input Voltage	± 5V
Analog Input Voltage	± 5V
INPUTS	
Input Voltage Range[1], min.	± 2.5V
max.	± 5V
Input Bias Current	50μA
Input Impedance, min.	10 kΩ
Maximum Source Impedance[2]	50Ω
Sample control Inputs[3]	Differential ECL 10,000 Positive Pulse on Pin 3 and Negative Pulse on Pin 1 gives Hold Mode.
OUTPUTS	
Output Voltage Range[1], min.	± 2.5V
max.	± 5V
Output Current[4]	± 30 mA
Output Impedance[4]	13Ω
PERFORMANCE	
Linearity ± 2.5V input volt. range	0.1%
± 5V input volt. range	0.2%
Gain	+ 0.995
Gain Tempco, max.	± 33 ppm/°C
Sample-to-Hold Offset Error, max.	40 mV
Sample-Mode Offset Voltage, max.	± 20 mV
Sample-to-Hold Offset Voltage Drift	75 μV/°C
Sample-Mode Offset Voltage Drift	± 250μV/°C
Hold Mode Feedthrough, max.	− 66 dB
Hold Mode Droop	100 μV/μsec
DYNAMIC CHARACTERISTICS	
Acquisition Time, 2V to 0.1%	40 nsec
2V to 1%	25 nsec
4V to 0.1%	50 nsec
4V to 1%	35 nsec
10V to 0.1%	60 nsec
10V to 1%	45 nsec
Aperture Delay Time	3 nsec
Aperture Uncertainty Time, max.	10 psec
Hold Mode Settling Time	20 nsec
Sample-Mode Bandwidth; — 3 dB	40 MHz
Sampling Rate[5]	17 MHz
POWER REQUIREMENTS	
Positive Supply, Pin 19	+ 15V ± 0.5V @ 60 mA
Negative Supply, Pin 9	− 15V ± 0.5V @ 60 mA
PHYSICAL ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-7MC	0°C to + 70°C
SHM-7MR	− 25°C to + 85°C
Storage Temperature Range	− 65°C to + 150°C
Package Type	24 Pin, hermetically sealed, ceramic.
Pins	0.010 × 0.018 Inch Kovar

NOTES:
1. The SHM-7MR is specified for operation with a maximum input/output voltage range of ± 2.5V. The SHM-7MC has a maximum input/output voltage range of ± 5V.
2. Should be purely resistive. See technical note 3.
3. Input logic voltage levels are V_{in} "0" = − 1.5V to − 1.4V, and V_{in} "1" = − 0.7V to − 1.05V.
4. Specified for each output, both outputs may be tied together for decreased output impedance and increased output current.
5. For a ± 2V input.

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for rated performance. The power common (Pins 11, 12, 13 and 15), analog common (Pins 14, 17 and 20), and input common (Pin 21) pins are not connected internally and therefore must be connected externally as directly as possible through a low inductance, low resistance path. The extensive use of a ground plane for all common connections is highly recommended.

2. Although they are internally bypassed with .033 μF capacitors the supply pins (Pins 19, 9) should be externally bypassed with 0.1 μF ceramic chip capacitors mounted as close to the supply pins as possible.

3. The SHM-7 inputs and outputs are sensitive to unusual loading or long lines. The analog input must be nonreactive so that leads should be short and purely resistive. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.

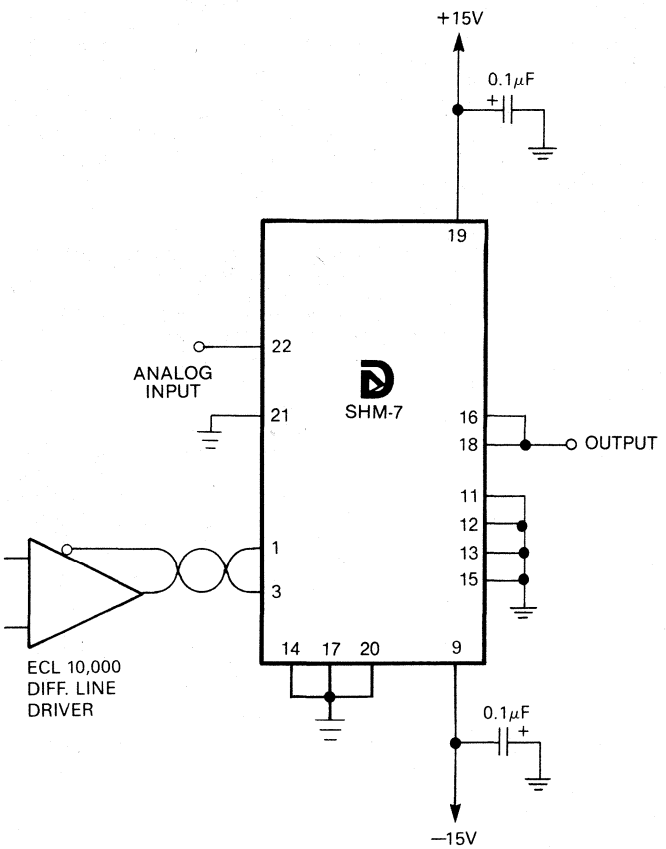
4. The maximum, differential, digital input voltage is ± 5V. For example, if pin 3 is at a potential of − 5V, pin 1 may not exceed 0V.

ORDERING INFORMATION

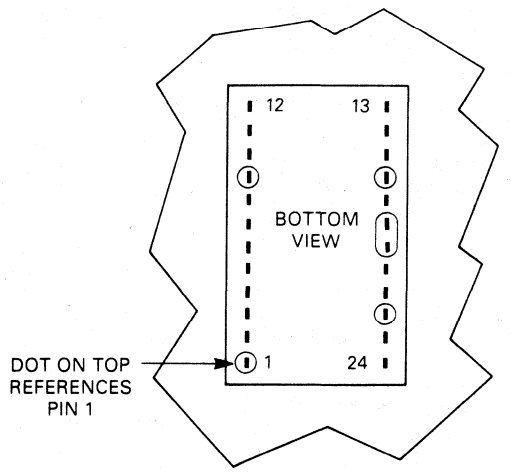
MODEL NO.	OPERATING TEMP. RANGE	PRICE (1-24)
SHM-7MC	0°C to + 70°C	
SHM-7MR	− 25°C to + 85°C	

PERFORMANCE AND CONNECTION

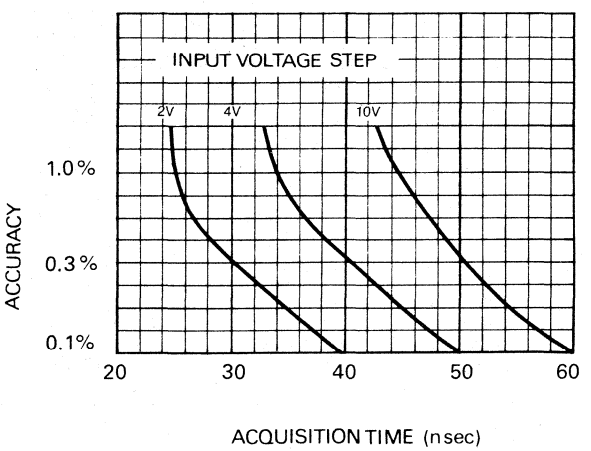
TYPICAL CONNECTION



BASIC GROUND PLANE LAYOUT



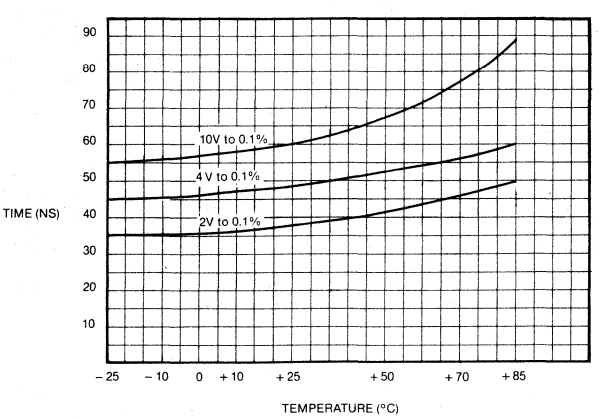
ACQUISITION TIME VS INPUT VOLTAGE



SAMPLE-HOLD DEFINITIONS

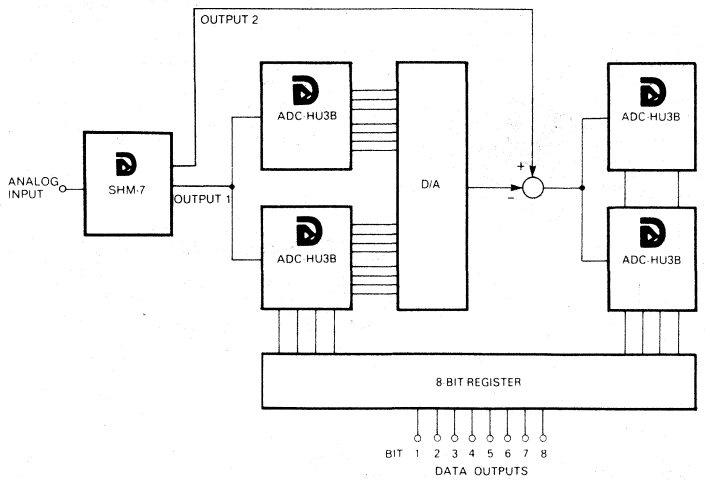
1. Acquisition Time
   Time required, after receipt of the sample command, for the hold capacitor to charge to a specified voltage change and remain within a specified error band such as 0.1%.
2. Aperture Delay Time (effective)
   The time elapsed from the hold command to the opening of the sampling switch minus the delay from the analog input to the sample switch.
3. Aperture Uncertainty Time
   Time variation, or jitter, in the opening of the sampling switch.
4. Aperture Uncertainty Error
   An amplitude uncertainty in the held value due to the change in the analog input signal during the aperture uncertainty time. This error is the product of the rate of change of the input signal and the aperture uncertainty time.
5. Hold-Mode Settling Time
   The time from the hold command transition until the output of the Sample-Hold has settled within the specified error band (0.1%). It includes aperture delay time.
6. Hold-Mode Droop
   The output voltage change per unit of time while in the hold mode.
7. Bandwidth
   The frequency at which the gain is down 3 dB from its dc value. It's measured in the sample-mode with a small-signal sine wave.

ACQUISITION TIME VS. TEMPERATURE



TYPICAL APPLICATIONS

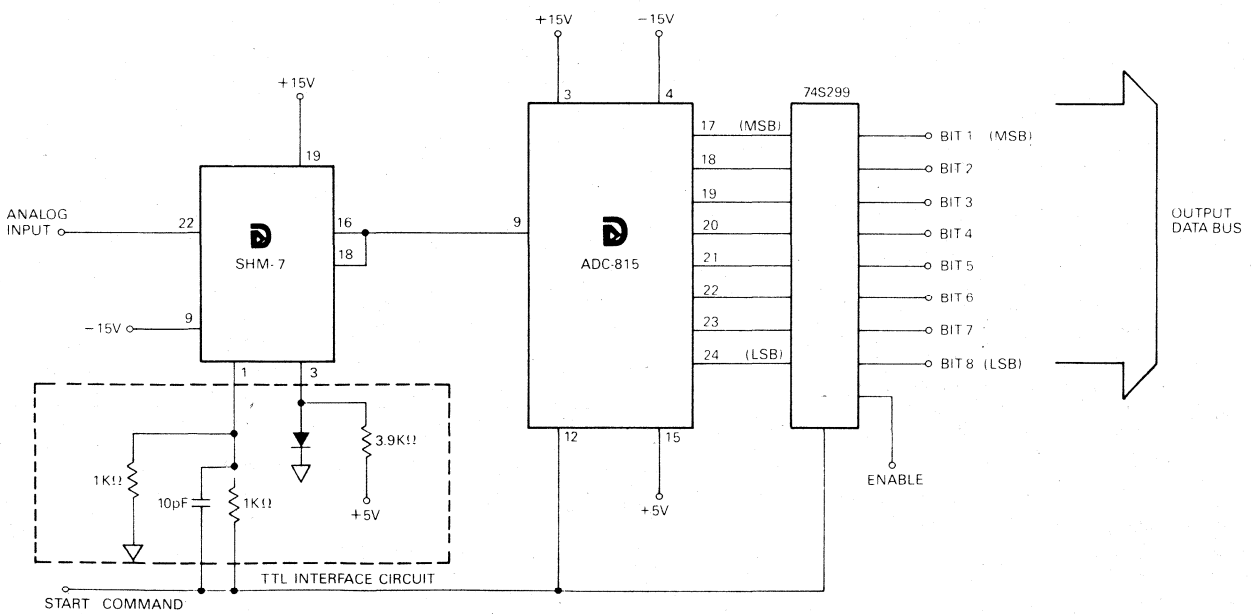
TWO STAGE CONVERSION SYSTEM



The dual outputs of the SHM-7 lend it to applications involving two stage conversion techniques. In the sample shown, using output 1 of the SHM-7; the parallel conversion of the first 4 bits is accomplished and goes to an ultra-fast D/A converter which converts the result back to analog. The resultant analog voltage is then subtracted from output 2 of the SHM-7 and the difference is converted to digital form by the second 4 bit parallel converter. Each 4 bit stage passes its output to an 8 bit output register which holds the 8 bit digital word at the end of conversion. The SHM-7 is shown here with Datel-Intersil's ADC-HU3B, a low cost, 3 bit flash converter.

The sample-hold requires two buffered outputs because of the load changes caused by the switching voltages present at the D/A summing junction. These load changes would cause errors at the sample-hold output which would in turn be passed into the A/D input.

HIGH SPEED DATA SYSTEM



A high speed data system using Datel-Intersil's SHM-7 and ADC-815, with an output register, to drive a data bus. The Start Command is a 60 nsec wide, TTL compatible, pulse with a maximum frequency of 1.5 MHz. Upon receipt of a start command, the SHM-7 will track the input voltage and the ADC-815 will reset. On the trailing edge of the start command, the SHM-7 will hold the intput and the ADC-815 will begin its conversion. On the leading edge of the next start command, the output data will be clocked out of the output three-state register. The ADC-815 is an 8 bit, 700 nsec, analog to digital converter. With this system, a ±2.5V input step can be acquired to 0.1% accuracy in 40 nsec and held to within 80 μV while the A/D conversion takes place.

NEW

DATEL

Low Cost, Fast, 0.01% Sample-Hold SHM-9

FEATURES

- Low Cost
- 0.01% Accuracy
- 6 μsec Acquisition Time
- 0.2 mV/msec Hold-Mode Droop
- No External Adjustments Needed

GENERAL DESCRIPTION

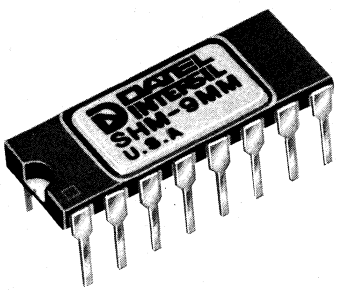
Datel-Intersil's SHM-9 is a fast, hybrid sample-hold amplifier that combines high performance versatility and low cost. Acquisition time, for a 10V change to 0.01%, is only 6 μsec, and aperture delay time is 200 nsec. The small signal bandwidth is 4 MHz.

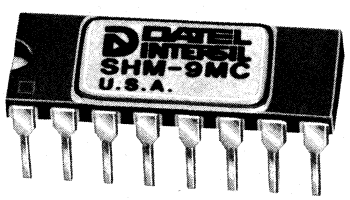
The SHM-9 is a complete, self-contained unit, including a bipolar input amplifier, a low-leakage electronic switch, a FET output amplifier, a precision 1000 pF hold capacitor and logic control circuitry. The control circuitry allows the SHM-9 to be interfaced with virtually any A/D converter using the converter's start/convert and EOC signals. This allows the user to put the SHM-9 into the hold mode using the start/convert pulse; thus when the A/D's EOC signal goes high and conversion begins, the SHM-9 will already be providing a stable analog input signal. When the EOC goes low, signaling the end of conversion, the SHM-9 is switched into the sample mode. If this is not practical, the SHM-9 can also be used with a single control signal. An external hold capacitor may be added if necessary.

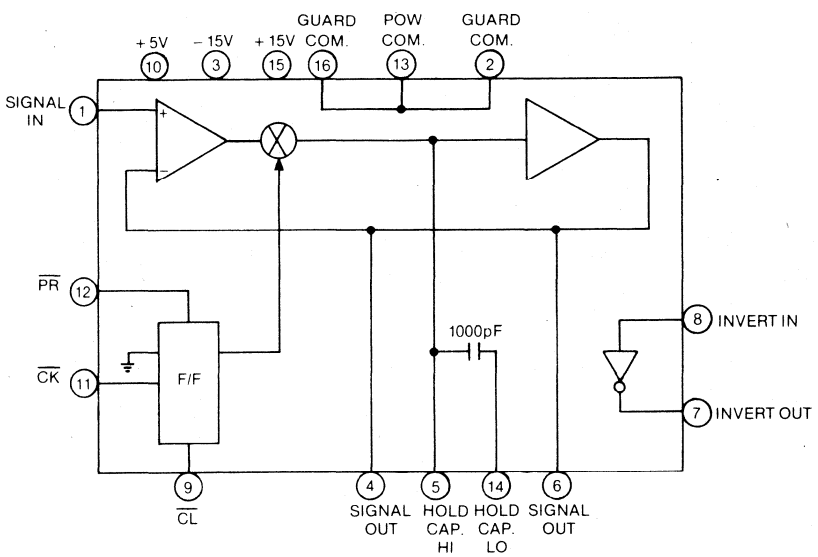
Other important features include $10^{10}\Omega$ input impedance, a hold-mode feedthrough of 0.01%, and a hold-mode droop of only 0.2 mV/msec maximum. Input/output voltage range is ±11.5V, input bias current is 50 nA maximum, and the input offset voltage drift is 20 μV/°C. The SHM-9 is functionally laser trimmed to eliminate offset, and sample to hold offset errors, and is designed to be used without external adjustment circuits.

Its low cost, high performance and input control flexibility make the SHM-9 a good choice for unnumerable applications including sampling for A/D conversion, analog demultiplexing circuits and simultaneous sampling circuits. The small size of the SHM-9 allows it to be easily used with automatic insertion equipment.

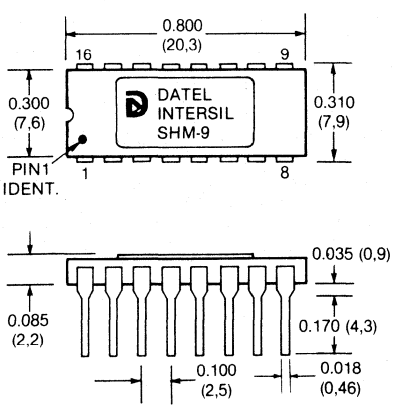
The SHM-9 is available in three models for operation over the commercial, 0°C to +70°C industrial, −25°C to +85°C and military, −55°C to +125°C, operating temperature ranges. Power requirement is ±15VDC and +5VDC. All models are packaged in a 16 pin hermetically sealed, ceramic DIP.







MECHANICAL DIMENSIONS INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT	9	$\overline{CL}$
2	GUARD COMMON	10	+5VDC
3	−15VDC (V−)	11	$\overline{CK}$
4	OUTPUT	12	$\overline{PR}$
5	EXT. HOLD CAP. HI	13	POWER COMMON
6	OUTPUT	14	EXT. HOLD CAP. LO
7	INVERT OUT	15	+15VDC (V+)
8	INVERT IN	16	GUARD COMMON

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SPECIFICATIONS, SHM-9

Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted.

MAXIMUM RATINGS	
Positive Supply, Pin 15	+18V
Negative Supply, Pin 3	−18V
Logic Supply, Pin 10	5.5V
Analog Input Voltage	$\pm V_S$
ANALOG INPUT	
Input Voltage Range	±11.5V
Input Impedance	$10^{10}\Omega$
Input Offset Voltage, max.[1]	±2 mV
Input Offset Voltage Drift	20 μV/°C
Input Bias Current, max.	50 nA
DIGITAL INPUTS	
Logic Level High, V_{in} ("1"), min.	+2V
Logic Level Low, V_{in} ("0"), max.	+0.8V
High Level Input Current	60 μA
Low Level Input Current	−0.8 mA
Inverter Input Delay, max.[2]	30 nsec
OUTPUT	
Output Voltage Range	±11.5 V
Output Current, S.C. Protected	5 mA
Output Impedance	0.5Ω
PERFORMANCE	
Accuracy	0.01%
Gain	+1 V/V
Gain Error, max.[3]	0.01%
Sample to Hold Offset, max.[4]	2.5 mV
Hold Mode Feedthrough	0.01%
Hold Mode Droop, max.	0.2 mV/msec
Output Noise, Hold Mode[5]	8.5 μV RMS
Power Supply Rejection Ratio min.	80 dB
DYNAMIC CHARACTERISTICS	
Acquisition Time, 10V to 0.1%	5 μsec
10V to 0.01%	6 μsec
20V to 0.1%	7 μsec
20V to 0.01%	8 μsec
Aperture Delay Time	200 nsec
Small Signal Bandwidth, −3 dB	4 MHz
POWER REQUIREMENT	
Analog Supply Range	±5 VDC to ±18 VDC
Supply Voltage, Rated Performance	±15 VDC @ 6.5 mA max.
Logic Supply	+5 VDC ±0.25V @ 9 mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range: MC	0°C to +70°C
MR	−25°C to +85°C
MM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package	16 pin hermetically sealed ceramic DIP

NOTES:

1. Adjustable to zero
2. This specification refers to the time delay between the invert input (Pin 8) and invert output (Pin 7).
3. R_L = 10 kΩ
4. V_{out} = OV
5. 10 Hz to 100 kHz

TECHNICAL NOTES

1. An external hold capacitor may be added from Pin 5 (EXT. CAP. HI) to Pin 14 (EXT. CAP. LO). For best results, this should be a good quality capacitor with very high insulation resistance and low dielectric absorption; such as MOS, polystyrene or polypropylene type capacitors. Hold mode droop and sample to hold offset will decrease proportionately with the size of this capacitor, and acquisition time will increase proportionately. For lowest hold mode droop, a guard ring connected to the output should be put around EXT. CAP. HI Pin (Pin 5), as shown in the circuit board layout on page 5.

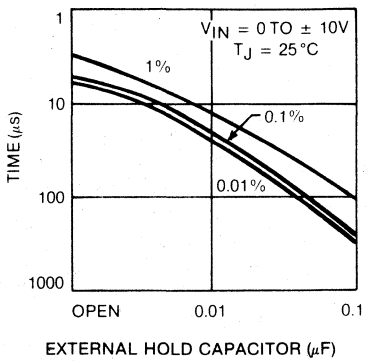
2. Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this, the circuit board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source.

ORDERING INFORMATION

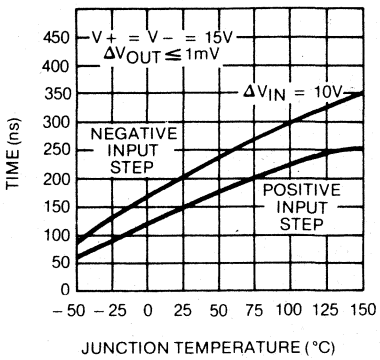
MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
SHM-9MC	0°C to +70°C	
SHM-9MR	−25°C to +85°C	
SHM-9MM	−55°C to +125°C	

PERFORMANCE CURVES

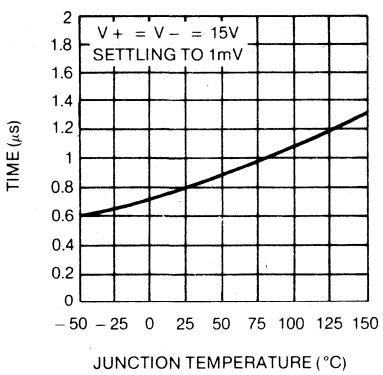
ACQUISITION TIME



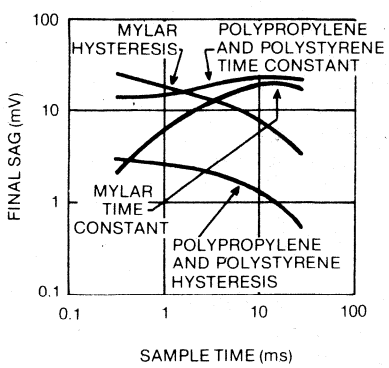
APERTURE TIME



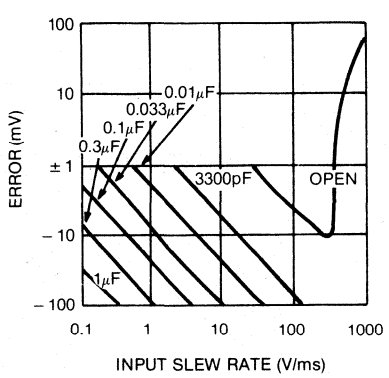
"HOLD" SETTLING TIME



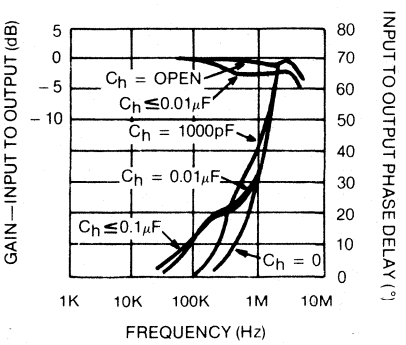
CAPACITOR HYSTERESIS



DYNAMIC SAMPLING ERROR

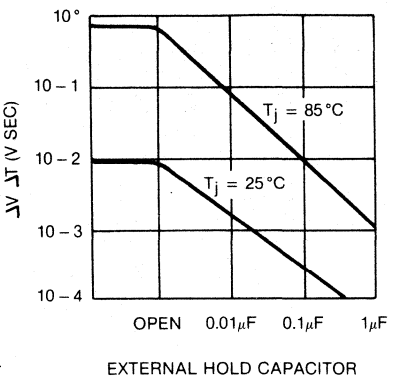


PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)

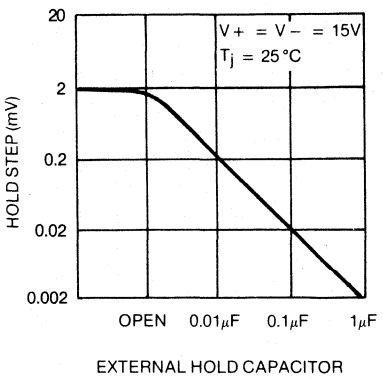


PERFORMANCE CURVES

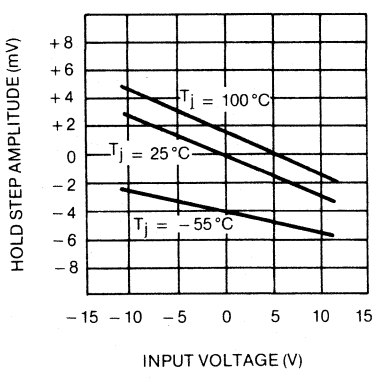
OUTPUT DROOP RATE



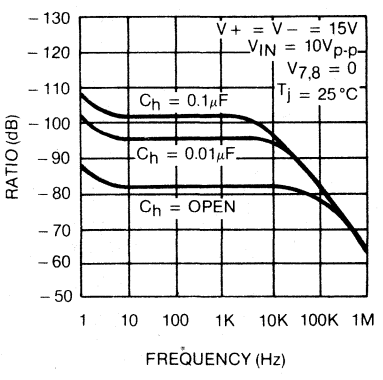
HOLD STEP



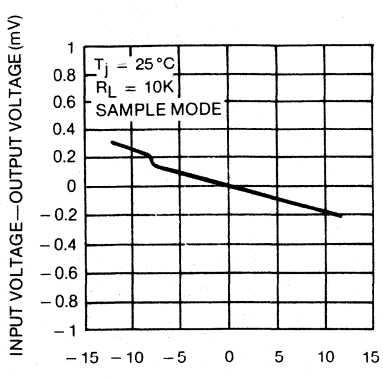
HOLD STEP INPUT VOLTAGE



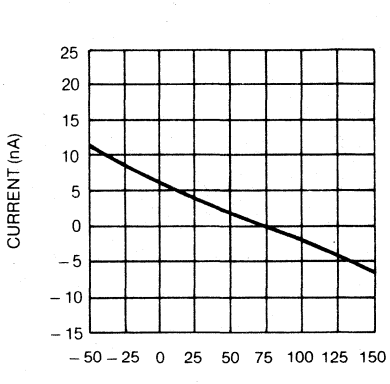
FEEDTHROUGH REJECTION RATIO (HOLD MODE)



GAIN ERROR

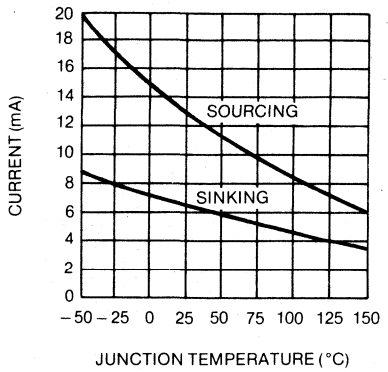


INPUT BIAS CURRENT

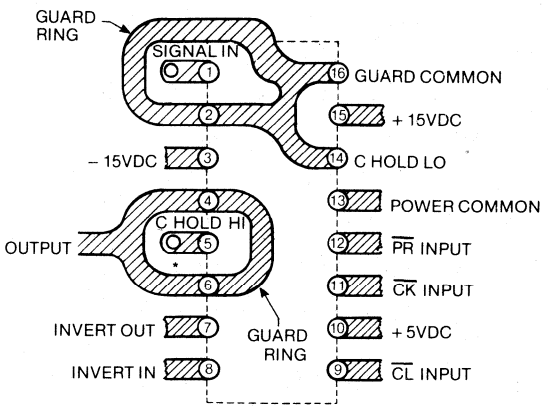


PERFORMANCE AND CONNECTION

OUTPUT SHORT CIRCUIT CURRENT

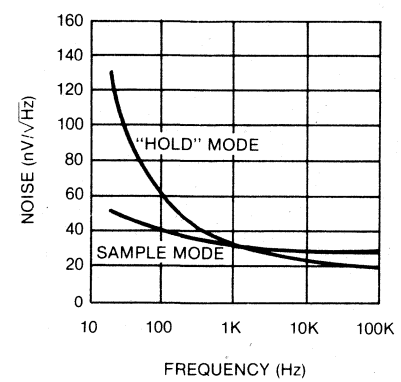


CIRCUIT BOARD LAYOUT

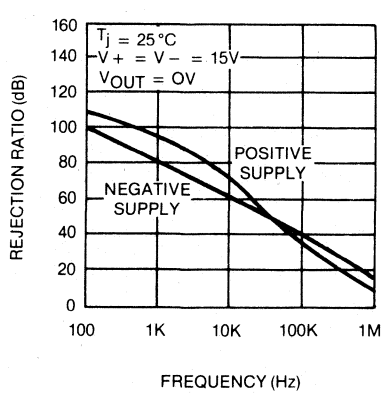


*ADDITIONAL EXTERNAL CAP, IF USED

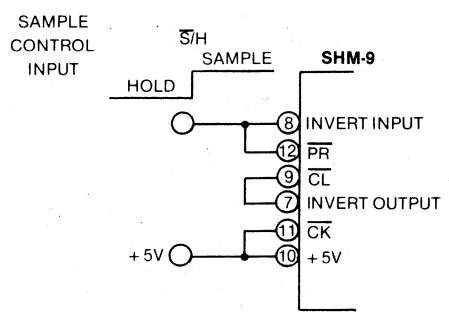
OUTPUT NOISE

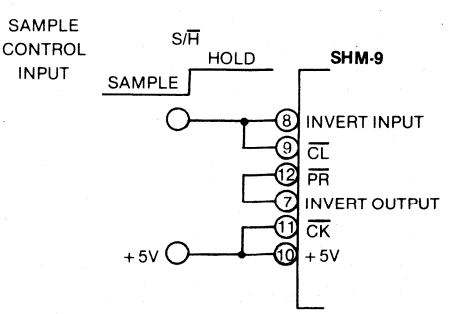


POWER SUPPLY REJECTION



SINGLE LINE CONTROL

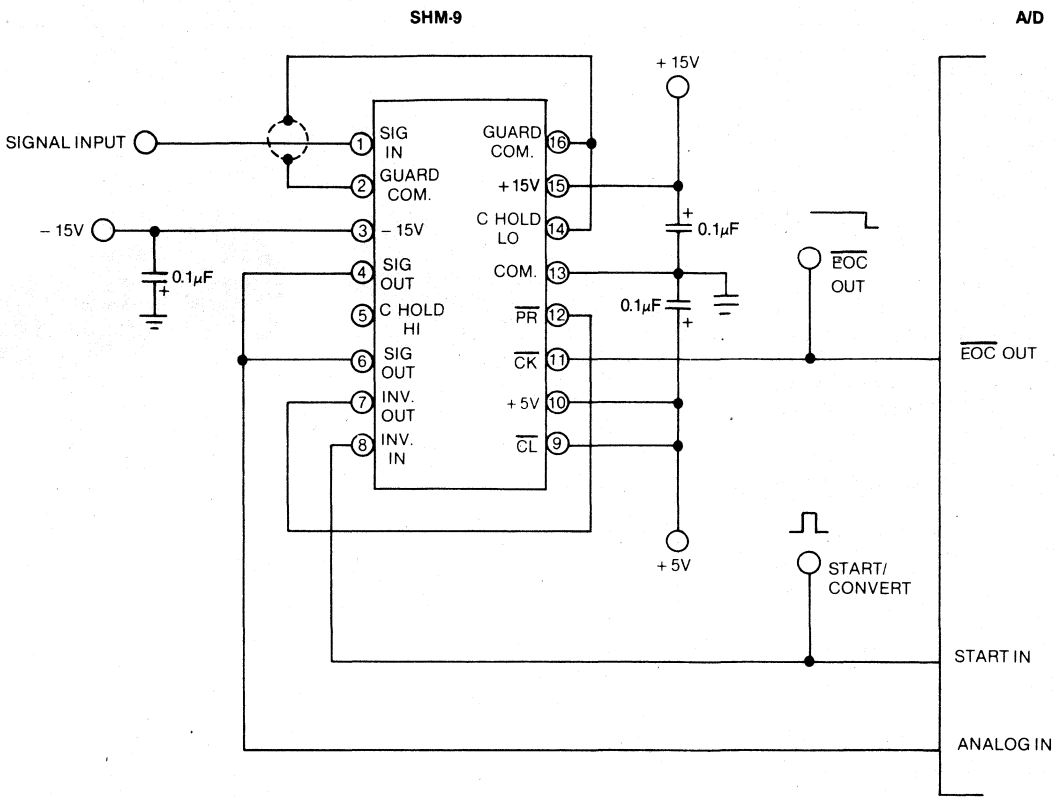




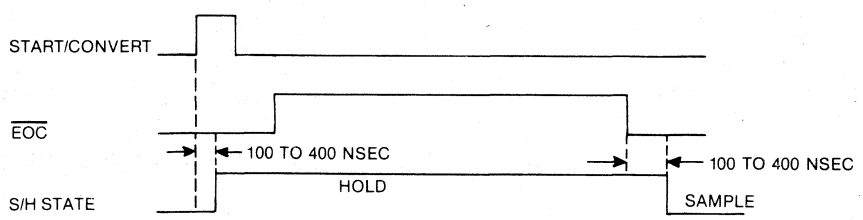
The SHM-9 sample/hold switch can be controlled with one hold command input. The above diagrams give the circuit connection for either a Sample/Hold or a Sample/Hold control input. When using the SHM-9 with an A/D converter, the converters' E.O.C. (STATUS) output can be used to control the SHM-9.

APPLICATION

A/D INTERFACE



TIMING DIAGRAM



The SHM-9 is easily interfaced with most A/D converters. The diagram shows a typical connection in which the SHM-9 is controlled by the Start/Convert and EOC (Status) signals of the A/D converter. The Start/Convert signal puts the SHM-9 into the hold mode. The internal inverter allows the designer to use either a positive or negative Start/Convert signal. When the E.O.C. signal goes high and the A/D begins its conversion cycle, the SHM-9 is already providing a stable analog input to the A/D's comparator. When the E.O.C. goes low, signaling the end of conversion, the SHM-9 is switched back to the sample mode.

NEW

DATEL

High Speed, 0.01% Monolithic Sample/Hold SHM-20

FEATURES

- **Internal Hold Capacitor**
- **1 μS Acquisition Time**
- **1 nS Aperture Uncertainty**
- **0.01% Accuracy**
- **0.08 μV/μS Droop Rate**
- **Differential Inputs**

GENERAL DESCRIPTION

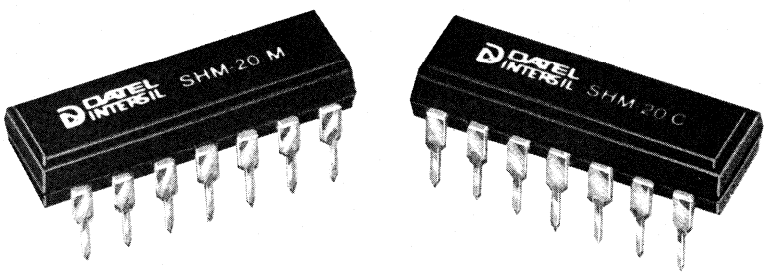
DATEL-INTERSIL's SHM-20 is a low cost, complete monolithic sample/hold amplifier which includes an internal 100 pF MOS hold capacitor. Primarily designed for high speed analog signal processing applications, the SHM-20 features a typical acquisition time of 1.0 μS for a 10V input step to 0.01%. Aperture uncertainty is typically 1 ns and droop rate is as low as 0.08 μV/μS.

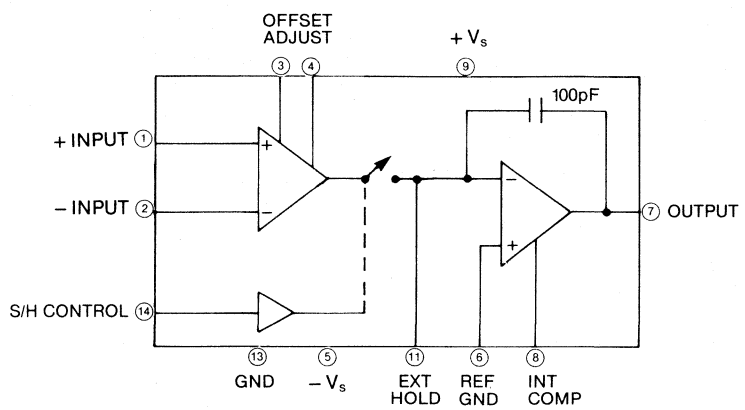
The SHM-20 consists of an input transconductance amplifier, a low leakage analog switch, an output integrating amplifier and a 100 pF MOS hold capacitor. Charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by using the offset adjust inputs. For improved droop rate, an external hold capacitor may be added at the expense of acquisition time.

Other important features of the SHM-20 include a 30 nS aperture delay time, 1 mV pedestal error, a minimum DC gain of 10^6V/V and fully differential inputs with a ± 10V input voltage range. Maximum input offset voltage is as low as 0.5 mV with a maximum input offset voltage drift as low as 15 μV/°C.

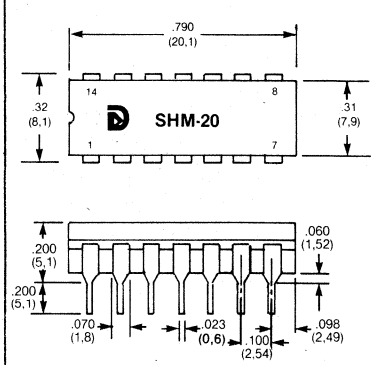
Its low cost and high performance make the SHM-20 an excellent choice for innumerable applications including, precision data acquisition systems, deglitching circuits, auto-zero circuits, data distribution systems and peak amplitude detectors. Power requirement is ± 15 VDC.

The SHM-20 is available in two models for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges. Both models are packaged in a 14 pin ceramic DIP.





MECHANICAL DIMENSIONS INCHES (mm) MAX.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+ INPUT
2	– INPUT
3	OFFSET ADJUST
4	OFFSET ADJUST
5	– V_S
6	REFERENCE GROUND
7	OUTPUT
8	INTEGRATOR COMPENSATION
9	+ V_S
10	NO CONNECTION
11	EXTERNAL HOLD CAPACITATOR
12	NO CONNECTION
13	SUPPLY VOLTAGE GROUND
14	S/H CONTROL

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, SHM-20

(Typical at +25°C, ±15VDC, using internal hold capacitor, unless otherwise noted.)

	SHM-20C	SHM-20M
MAXIMUM RATINGS		
Voltage between Supply Pins (Pins 9,5)	40V	
Differential Input Voltage	±24V	
Digital Input Voltage, Pin 14	+8V to −15V	
Output Current, Continuous[1]	±20 mA	
ANALOG INPUT		
Input Voltage Range,[2] min.	±10V	
Input Impedance, min.	1 MΩ	
Input Capacitance, max.	3 pF	
Input Offset Voltage, max.	1 mV	0.5 mV
Input Offset Voltage Drift, max.	20 μV/°C	15 μV/°C
Input Bias Current, max.	300 nA	200 nA
Input Offset Current, max.	300 nA	100 nA
DIGITAL INPUTS[2]		
Logic Level High, Vin ("1"), min.	2.0V	
Logic Level Low, Vin ("0"), max.	0.8V	
High Level Input Current, max.	0.1 μA	
Low Level Input Current, max.	4 μA	
OUTPUT		
Output Voltage Range[2], min.	±10V	
Output Current[2], min.	±10 mA	
Output Impedance, Hold Mode[2]	1 Ω	
PERFORMANCE		
Accuracy	0.01%	
DC Gain, min.	3×10^5 V/V	10^6 V/V
Gain Accuracy[4]	0.5×10^{-4}%FSR	
Gain Error Tempco	±0.6 ppm/°C	
Gain Bandwidth Product[5]	2 MHz	
Hold Mode Feedthrough, 10V P-P, 100 kHz[2]	2 mV	
Droop Rate	0.08 μV/μS	
Droop Rate[2]	1.2 μV/μS	17 μV/μS
Charge Transfer[6]	0.1 pc	
Pedestal Error	1 mV	
Total Output Noise, DC to 10 MHZ, max.	200 μVRMS	
Power Supply Rejection Ratio, min:		
+VS	80 dB	
−VS	65 dB	
Pedestal Error	1 mV	
DYNAMIC CHARACTERISTICS		
Acquisition Time, 10V to 0.1%	0.8 μS	
10V to 0.01%	1.0 μS	
Aperture Delay Time	30 nS	
Aperture Uncertainty Time	1 nS	
Aperture Time	25 nS	
Hold Mode Settling Time, 0.01%[2]	185 nS	
Rise Time	100 nS	
Overshoot	15%	
Slew Rate[7]	45 V/μS	
POWER REQUIREMENTS[8]		
Positive Supply, Pin 9	+15V ±0.5V @ 11 mA	
Negative Supply, Pin 5	−15V ±0.5V @ −11 mA	
PHYSICAL ENVIRONMENTAL		
Operating Temperature Ranges,		
SHM-20C	0°C to +70°C	
SHM-20M	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Package Type	14 Pin, Ceramic DIP	

NOTES:

1. Internal power dissipation may limit output current below +20 mA.
2. Over full operating temperature range.
3. Cannot tolerate even a momentary short circuit to ground or either supply.
4. Voltage gain = +1
5. Voltage gain = +1, load resistance = 1 kΩ, load capacitance = 50 pF, output voltage = 100 mV P-P.
6. Input voltage = 0V, digital input voltage = 3.5V
7. Output voltage = 10V step.
8. A power supply voltage as low as ±12V may be used. However, this will cause some degradation in performance.

TECHNICAL NOTES

1. A printed circuit board with ground plane is recommended for best performance. The supply pins (Pins 5,9) should be bypassed to ground with a 0.01 to 0.1 μF ceramic capacitor as close to the pins as possible.

2. If an external hold capacitor (C_H) is used, then a noise bandwidth capacitor with a value of 0.1 C_H (10% of the value of the external hold capacitor) should be connected from Pin 8 to ground. Exact value and type are not critical.

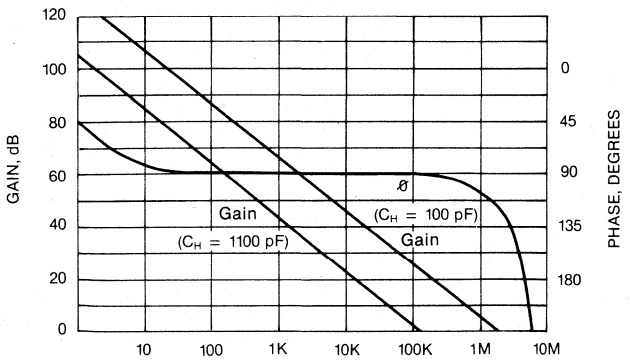
3. The Hold Capacitor (C_H) should have high insulation resistance and low dielectric absorption to minimize droop error. For operating temperatures up to +85°C, polystyrene dielectric is a good choice. For good performance to +125°C, Teflon or glass dielectrics are recommended. Any PC connections to the hold capacitor terminal (Pin 11) should be kept short and "guarded" by the ground plane to avoid errors due to drift currents from nearby signal lines or power supply voltages.

ORDERING INFORMATION

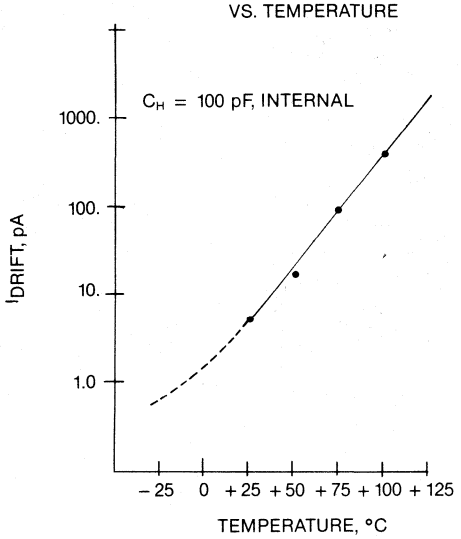
MODEL	TEMP. RANGE	PRICE (1-24)
SHM-20C	0°C to +70°C	
SHM-20M	−55°C to +125°C	

TYPICAL PERFORMANCE AND DEFINITIONS

OPEN LOOP GAIN AND PHASE RESPONSE



DRIFT CURRENT VS. TEMPERATURE



SAMPLE and HOLD DEFINITIONS:

ACQUISITION TIME: The time required, after the sample command is given, for the hold capacitor to charge to a full-scale voltage change and then remain within a specified error band around the final value.

APERTURE TIME: The time required for the Sample & Hold switch to open, independent of delays through the switch driver and input amplifier circuitry.

APERTURE DELAY TIME: The time elapsed from the hold command to the actual opening of the sampling switch.

APERTURE UNCERTAINTY TIME: The time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample.

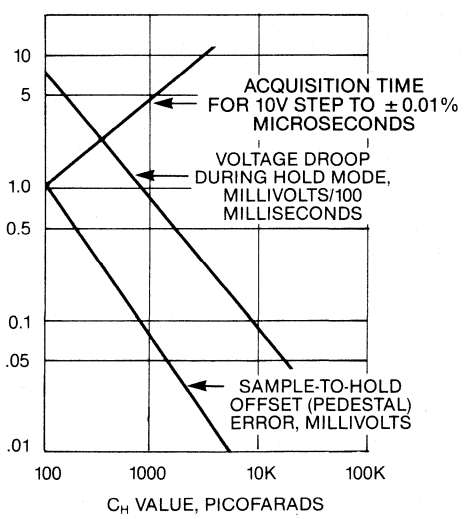
CHARGE TRANSFER: The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the hold mode. This is caused by the switch control voltage change coupling through switch capacitance to the hold capacitor. Also called charge dumping or charge injection.

DRIFT CURRENT: The net leakage current from the hold capacitor during hold mode.

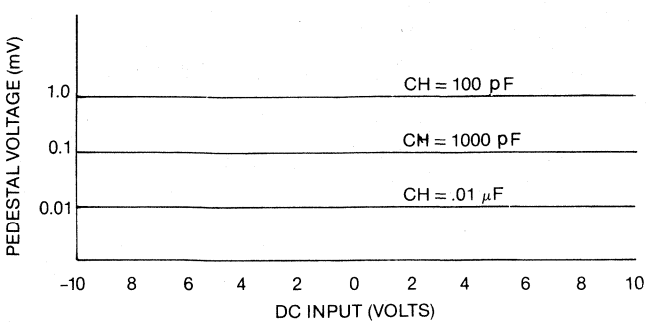
HOLD MODE DROOP: The output voltage change per unit time with the sampling switch open. Commonly expressed in V/sec or μV/μsec.

PEDESTAL ERROR: For a sample-hold, the change in output voltage from the sample-mode to the hold-mode, with constant input voltage. This error is caused by the sampling switch tranferring charge onto the hold capacitor as it opens.

TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR

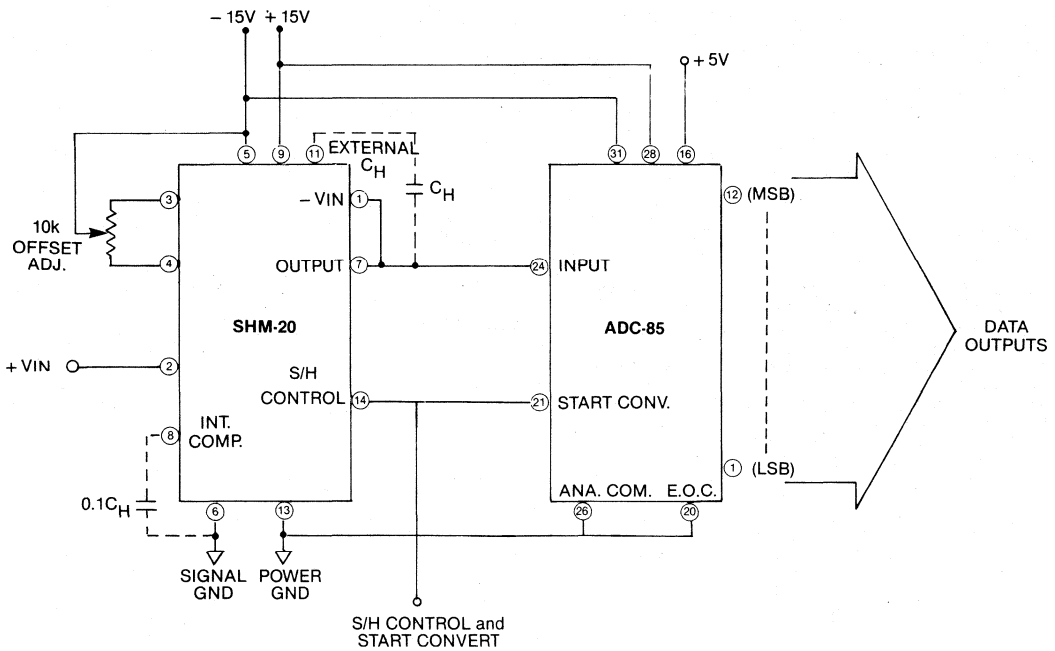


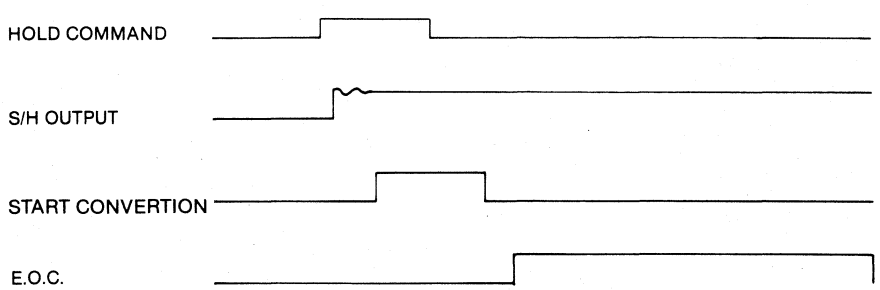
PEDESTAL VS. INPUT VOLTAGE



APPLICATIONS

UNITY GAIN NON-INVERTING S/H AMPLIFIER





The above diagram shows the SHM-20 connected as a unity gain non-inverting S/H amplifier, with Datel-Intersil's ADC-85, 12 bit successive approximation A/D converter. The SHM-20's pedestal error is adjustable to zero, by the offset adjust trim pot, allowing a 12 bit accurate output from the ADC-85.

If an external hold capacitor (C_H) is required, it may be connected as shown between Pins 11 and 7. If an external hold capacitor is used, a capacitor, 0.1 C_H (10% of the value of the external hold capacitor) is then required from Pin 8 to ground to reduce output noise in hold mode. The RC network on Pin 14 delays the S/H Control/Start Convert Pulse to allow the sample to hold transient time to settle before a conversion begins. See Timing Diagram.

NEW

DATEL

High Speed, 0.01% Hybrid Sample/Hold SHM-4860

PRELIMINARY

FEATURES

- **200 nsec Max. Acquisition Time**
- **0.01% Accuracy**
- **100 nsec Max. Sample-Hold Settling Time**
- **74 dB Feedthrough Attenuation**
- **± 50 psec Aperture Uncertainty**

GENERAL DESCRIPTION

DATEL-INTERSIL's SHM-4860 is a high speed, high accuracy sample-hold designed for precision, high-speed analog signal processing applications. Manufactured with modern, high quality hybrid technology, the SHM-4860 features excellent dynamic specifications including a maximum acquisition time of only 200 nsec for a 10V step to 0.01%. Sample to hold settling time, to 0.01% accuracy is 100 nsec maximum with an aperture uncertainty of ± 50 psec.

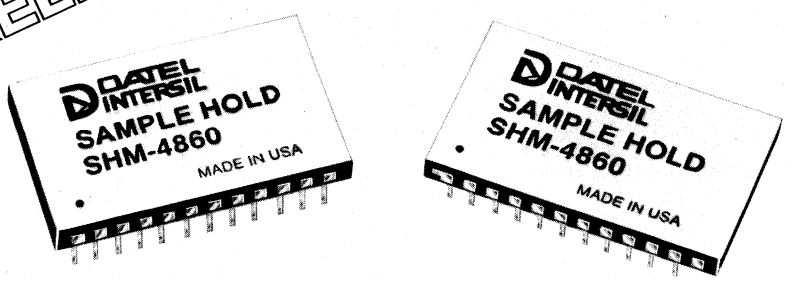
The SHM-4860 is a complete sample-hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

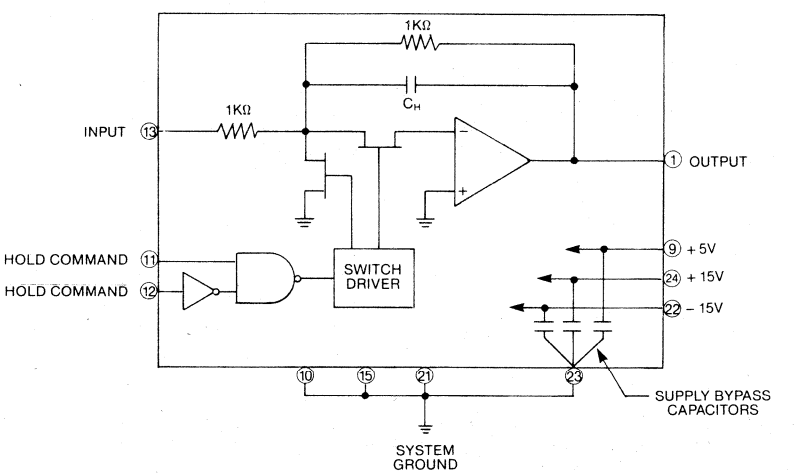
Other important features include a minimum input voltage range of ± 10.25V, an aperture delay time of 6 nsec, a typical droop rate of ± 0.4V/μsec, and a sample to hold offset error as low as ± 2.5 mV. Sample to hold offset is constant regardless of the input/output voltage level. Output slew rate is typically 300V/μsec and small signal bandwidth (– 3 dB) is 16 MHz.

Both HOLD and $\overline{\text{HOLD}}$ digital control inputs are provided for use with either positive or negative true input commands. Product performance is identical regardless of which input is used. Both digital control inputs are TTL compatible.

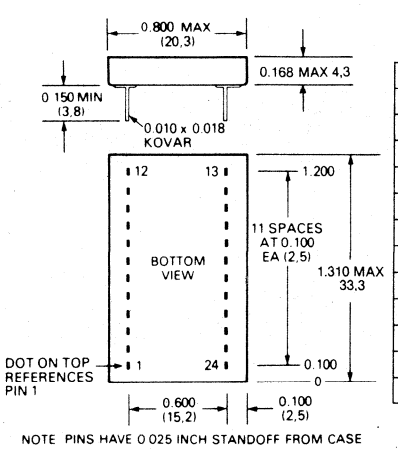
Applications for the SHM-4860 include high data acquisition and data distribution systems, peak measurement systems, fast fourier analysis, transient recorders and analog signal delay and storage.

Power requirement is ± 15 VDC and + 5 VDC with a maximum power consumption of 875 mW. The SHM-4860 is available in three models for operation over the commercial 0°C to + 70°C, industrial, – 25°C to + 85°C and military, – 55°C to + 125°C operating temperature ranges. All models are cased in a 24 pin, hermetically sealed, ceramic package. High reliability versions, screened to MIL-STD-883, level B are also available.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT	13	INPUT
2	N/C	14	N/C
3	N/C	15	GROUND
4	N/C	16	N/C
5	N/C	17	N/C
6	N/C	18	N/C
7	N/C	19	N/C
8	N/C	20	N/C
9	+ 5V SUPPLY	21	GROUND
10	GROUND	22	– 15V SUPPLY
11	HOLD COMMAND	23	GROUND
12	$\overline{\text{HOLD COMMAND}}$	24	+ 15V SUPPLY

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, SHM-4860
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted).

ABSOLUTE MAXIMUM RATINGS			
±15V Supply Voltage (Pins 24, 22)		±18V	
+5V Supply Voltage (Pin 9)		−0.5V to +7V	
Analog Input (Pin 13)[1]		±18V	
Digital Input (Pins 11, 12)		−0.5V to +5.5V	
Output Current[2]		±65 mA	
	MIN	**TYP**	**MAX**
ANALOG INPUT/OUTPUT			
Input/Output Voltage Range	±10.25V	±11.5V	
Input Impedance		1 kΩ	
Output Current[2]			±40 mA
Output Impedance		0.1Ω	
Maximum Capacitive Load		250 pF	
DIGITAL INPUT			
Input Logic Level,[3] Logic "1"	+2.0V		+5.0V
Logic "0"	0V		+0.8V
Loading[4]		1 TTL Load	
TRANSFER CHARACTERISTICS			
Gain		−1.0 V/V	
Gain Accuracy		±0.05%	±0.1%
Gain Linearity Error[5]		±0.005% FS	±0.01% FS
Sample-Mode Offset Voltage		±0.5 mV	±5 mV
Sample-to-Hold Offset Error (Pedestal)[6]		±2.5 mV	±20 mV
Gain Tempco (Drift)		±0.5 ppm/°C	±5 ppm/°C
Sample-Mode Offset Drift[5]		±3 ppm of FSR/°C	±15 ppm of FSR/°C
Sample-to-Hold Offset (Pedestal) Drift[5]		±4 ppm of FSR/°C	
DYNAMIC CHARACTERISTICS			
Acquisition Time;[7]			
10V to ±0.01% FS (±1 mV)		160 nS	200 nS
10V to ±0.1% FS (±10 mV)		100 nS	170 nS
10V to ±1% FS (±100 mV)		90 nS	
1V to ±1% FS (±100 mV)		75 nS	
Sample-to-Hold, Settling Time[8]			
10V to ±0.01% FS (±1 mV)		60 nS	100 nS
10V to ±0.1% FS (±10 mV)		40 nS	
Sample-to-Hold Transient		180 mV P-P	
Aperture Delay Time		6 nS	
Aperture Uncertainty (Jitter)		±50 ps	
Output Slew Rate		300 V/μS	
Small Signal Bandwidth (−3 dB)		16 MHz	
Droop: +25°C		±0.5 μV/μS	±5 μV/μS
+70°C		±15 μV/μS	
+125°C		±1.2 mV/μS	
POWER REQUIREMENTS			
Voltage Range: ±15V		±3%	
+5V		±5%	
Power Supply Rejection Ratio		±0.5 mV/V	
Quiescent Current Drain: +15V		+21 mA	+25 mA
−15V		−22 mA	−25 mA
+5V		+17 mA	+25 mA
Power Consumption		730 mW	875 mW
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Ranges			
SHM-4860 MC		0°C to +70°C	
SHM-4860 MR		−25°C to +85°C	
SHM-4860 MM		−55°C to +125°C	
Storage Temperature Range		−65°C to +150°C	
Package Type		32 Pin Ceramic	
Pins		Kovar (0.010 x 0.018)	

NOTES:
1. Input signal should not exceed the supply voltage.
2. The SHM-4860's output is current limited at approximately ±65 mA. The device will withstand a sustained short to ground. However, shorts to either supply will cause permanent damage. For normal operation, the load current should not exceed ±40 mA.
3. See Technical Note 3.
4. One TTL load is defined as sinking 40 μA with a logic "1" input and sourcing 1.6 mA with a logic "0" input.
5. Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.
6. Sample-to-Hold offset error (Pedestal) is constant regardless of input/output level.
7. Acquisition time is tested with no load and is relatively unaffected by capacitive loads to 50 pF and resistive loads to 250Ω.
8. Sample-to-Hold settling time is the time between the point the sample-to-hold command is given and the point at which the analog output (following a transient) settles to within a specified error band around the final value.

TECHNICAL NOTES

1. All ground pins (10, 15, 21, 23) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. Care must be taken to insure that no ground potentials can exist between Pin 10 and the other ground pins.

2. Although the power supply pins (9, 22, 24) are internally bypassed to ground with 0.01 μF ceramic capacitors. Additional external 0.1 μF to 1 μF tantalum bypass capacitors may be required in critical applications.

3. A logic "0" on the HOLD COMMAND INPUT, (Pin 11) (or a logic "1" on the HOLD COMMAND INPUT, Pin 12) will put the device in the sample mode. In this mode, the device acts as an inverting unity gain amplifier and its output will track its input. A logic "1" on Pin 11 (logic "0" on Pin 12) will put the device in the HOLD mode, and the output will be held constant at the last input level present when the hold command was given.

   If the HOLD COMMAND INPUT (Pin 11) is used to control the device, Pin 12 must be tied to digital ground. If HOLD COMMAND INPUT (Pin 12) is used to control the device, Pin 11 must be tied to +5V.

4. The maximum capacitive load to avoid oscillation is typically 250 pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitances will affect both acquisition and settling time.

ORDERING INFORMATION

MODEL	TEMP. RANGE	PRICE
SHM-4860MC	0°C to +70°C	$
SHM-4860MR	−25°C to +85°C	$
SHM-4860MM	−55°C to +125°C	$

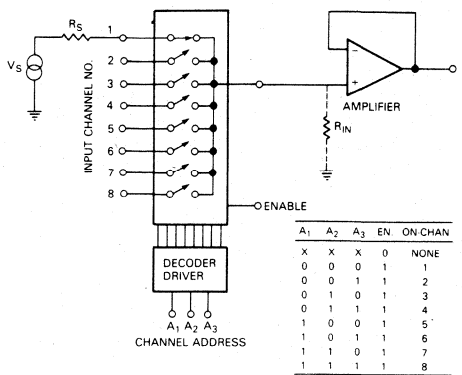
DILS-2 Mating Socket
(2 required per Sample-Hold) $

For high reliability versions of the SHM-4860, including units screened to MIL-STD-883, Level B, contact the factory.

Analog Multiplexers

Analog Multiplexer Operation

Analog multiplexers are the circuits that time-share an A/D converter among a number of different analog channels. Since the A/D converter in many cases is the most expensive component in a data acquisition system, multiplexing analog inputs to the A/D is an economical approach. Usually the analog multiplexer operates into a sample-hold circuit which holds the required analog voltage long enough for A/D conversion.



A_1	A_2	A_3	EN	ON CHAN
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Figure 1. Analog Multiplexer Circuit

As shown in Figure 1, an analog multiplexer consists of an array of parallel electronic switches connected to a common output line. Only one switch is turned on at a time. Popular switch configurations include 4, 8, and 16 channels which are connected in single (single-ended) or dual (differential) configurations.

The multiplexer also contains a decoder-driver circuit which decodes a binary input word and turns on the appropriate switch. This circuit interfaces

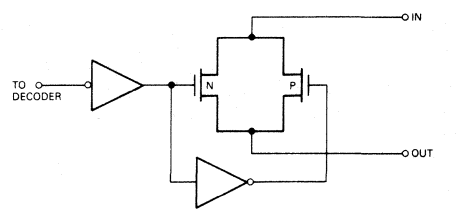


Figure 2. CMOS Analog Switch Circuit

with standard TTL inputs and drives the multiplexer switches with the proper control voltages. For the 8-channel analog multiplexer shown, a one-of-eight decoder circuit is used.

Most analog multiplexers today employ the CMOS switch circuit shown in Figure 2. A CMOS driver controls the gates of parallel-connected P-channel and N-channel MOSFET's. Both switches turn on together with the parallel connection giving relatively uniform on-resistance over the required analog input voltage range. The resulting on-resistance may vary from about 50 ohms to 2K ohms depending on the multiplexer; this resistance increases with temperature. A representative group of monolithic CMOS analog multiplexers is shown in Figure 3.

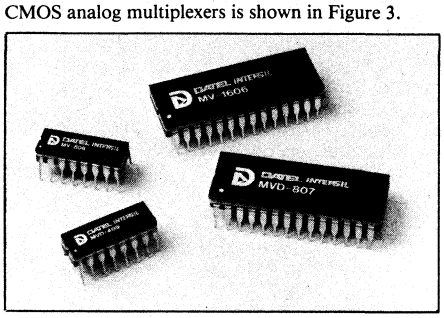


Figure 3. A Group of Monolithic CMOS Analog Multiplexers

Analog Multiplexer Characteristics

Because of the series resistance, it is common practice to operate an analog multiplexer into a very high load resistance such as the input of a unity gain buffer amplifier shown in the diagram. The load impedance must be large compared with the switch on-resistance and any series source resistance in order to maintain high transfer accuracy. *Transfer error* is the input to output error of the multiplexer with the source and load connected; error is expressed as a percent of input voltage.

Transfer errors of 0.1% to 0.01% or less are required in most data acquisition systems. This is readily achieved by using operational amplifier buffers with typical input impedances from 10^8 to 10^{12} ohms. Many sample-hold circuits also have very high input impedances.

Another important characteristic of analog multiplexers is *break-before-make* switching. There is a small time delay between disconnection from the previous channel and connection to the next channel which assures that two adjacent input channels are never instantaneously connected together.

Settling time is another important specification for analog multiplexers; it is the same definition previously given for amplifiers except that it is measured from the time the channel is switched on. *Throughput rate* is the highest rate at which a multiplexer can switch from channel to channel with the output settling to its specified accuracy. *Crosstalk* is the ratio of output voltage to input voltage with all channels connected in parallel and off; it is generally expressed as an input to output attenuation ratio in dB.

As shown in the representative equivalent circuit of Figure 4, analog multiplexer switches have a

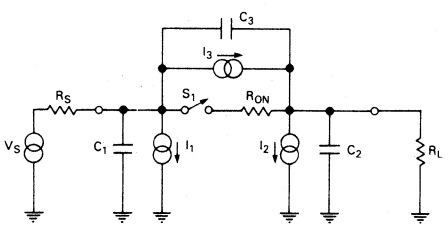


Figure 4. Equivalent Circuit of Analog Multiplexer Switch

number of leakage currents and capacitances associated with their operation. These parameters are specified on data sheets and must be considered in the operation of the devices. Leakage currents, generally in picoamperes at room temperature, become troublesome only at high temperatures. Capacitances affect crosstalk and settling time of the multiplexer.

Analog Multiplexer Applications

Analog multiplexers are employed in two basic types of operation: high-level and low-level. In *high-level multiplexing*, the most popular type, the analog signal is amplified to the 1 to 10V range ahead of the multiplexer. This has the advantage of reducing

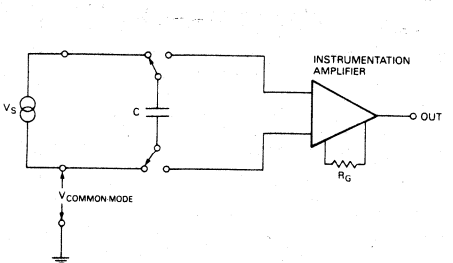


Figure 5. Flying Capacitor Multiplexer Switch

the effects of noise on the signal during the remaining analog processing. In *low-level multiplexing* the signal is amplified after multiplexing; therefore great care must be exercised in handling the low-level signal up to the multiplexer. Low-level multiplexers generally use two-wire differential switches in order to minimize noise pick-up. Reed relays, because of essentially zero series resistance and absence of switching spikes, are frequently employed in low-level multiplexing systems. They are also useful for high common-mode voltages.

A useful specialized analog multiplexer is the *flying-capacitor* type. This circuit, shown as a single channel in Figure 5 has differential inputs and is particularly useful with high common-mode voltages. The capacitor connects first to the differential analog input, charging up to the input voltage, and is then switched to the differential output which goes to a high input impedance instrumentation amplifier. The differential signal is therefore transferred to the amplifier input without the common mode voltage and is then further processed up to A/D conversion.

In order to realize large numbers of multiplexed channels, you can connect analog multiplexers in parallel using the enable input to control each device. This is called *single-level multiplexing*. You can also connect the output of several multiplexers to the inputs of another to expand the number of channels; this method is *double-level multiplexing*.

Glossary

ANALOG MULTIPLEXER: An array of switches with a common output connection for selecting one of a number of analog inputs. The output signal follows the selected input within a small error.

BREAK-BEFORE-MAKE SWITCHING: A characteristic of analog multiplexers in which there is a small time delay between disconnection from the previous channel and connection to the next channel. This assures that no two inputs are ever momentarily shorted together.

CROSSTALK: In an analog multiplexer, the ratio of output voltage to input voltage with all channels connected in parallel and off. It is generally expressed as an input to output attenuation ratio in dB.

DOUBLE-LEVEL MULTIPLEXING: A method of channel expansion in analog multiplexers whereby the outputs of a group of multiplexers connect to the inputs of another multiplexer.

FLYING-CAPACITOR MULTIPLEXER: A multiplexer switch which employs a double-pole, double-throw switch connected to a capacitor. By first connecting the capacitor to the signal source and then to a differential amplifier, a signal with a high common-mode voltage can be multiplexed to a ground-referenced circuit.

HIGH-LEVEL MULTIPLEXING: An analog multiplexing circuit in which the analog signal is first amplified to a higher level (1 to 10 volts) and then multiplexed. This is the preferred method of multiplexing to prevent noise contamination of the analog signal.

LOW-LEVEL MULTIPLEXING: An analog multiplexing system in which a low amplitude signal is first multiplexed and then amplified.

MUX: Abbreviation for multiplexer. See *Analog Multiplexer.*

SINGLE-LEVEL MULTIPLEXING: A method of channel expansion in analog multiplexers whereby several multiplexers are operated in parallel by connecting their outputs together. Each multiplexer is controlled by a digital *enable* input.

ANALOG MULTIPLEXERS

Quick selection: Analog multiplexers

	MODEL	DESCRIPTION	CHANNELS NO.	CHANNELS TYPE	SETTLING TIME, 20V to 0.01%	ACCESS TIME	CHANNEL RESISTANCE ON
	MV-808		8	Single Ended	2.8 μs	350 ns	250 Ω
	MV-808M						
	MV-1606	Low On-resistance, Dielectrically Isolated MUX's	16	Single Ended	2.4 μs	300 ns	270 Ω
	MV-1606M						170 Ω
	MVD-409		4	Diff.	2.8 μs	350 ns	250 Ω
	MVD-409M						
	MVD-807		8	Diff.	2.4 μs	300 ns	270 Ω
	MVD-807M						170 Ω
	MX-808	Overvoltage Protected	8	Single Ended	3 μs	500 ns	1.5 kΩ
	MX-808M						1.2 kΩ
NEW	MX-818C	High Speed	8	Sing. End. or Diff.	400 ns	125 ns	750 Ω
NEW	MX-818M		4				
	MX-1606	Overvoltage Protected	16	Single Ended	3 μs	500 ns	1.5 kΩ
	MX-1606M						1.2 kΩ
NEW	MX-1616C	High Speed	16	Sing. End. or Diff.	400 ns	150 ns	750 Ω
NEW	MX-1616M		8				
	MXD-409	Overvoltage Protected	4	Diff.	3 μs	500 ns	1.5 kΩ
	MXD-409M						1.2 kΩ
	MXD-807		8	Diff.	3 μs	500 ns	1.5 kΩ
	MXD-807M						1.2 kΩ

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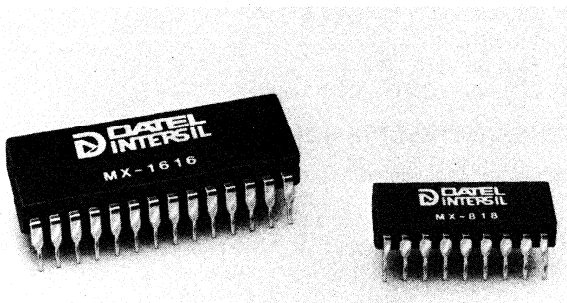
Each model of this broad line of 4, 8 and 16-channel multiplexers features break-before-make switching and an inhibit input that enables or disables the entire device permitting channel expansion by using several devices together.

Two new models, the MX-818 and MX-1616, are tailored for high-speed applications with access time specifications of 125 ns and 150 ns, respectively. A unique feature of these devices is their user programmable inputs, selectable for either single-ended or differential operation by simple pin-strapping.



TRANSFER ACCURACY	INPUT VOLTAGE RANGE OPER.	INPUT VOLTAGE RANGE ABS MAX	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
0.01%	± 15V	± 17V	16-pin DIP	Monolithic	0 to + 70	244
					– 55 to + 125	
0.01%	± 15V	± 17V	28-pin DIP	Monolithic	0 to + 70	
					– 55 to + 125	
0.01%	± 15V	± 17V	16-pin DIP	Monolithic	0 to + 70	
					– 55 to + 125	
0.01%	± 15V	± 17V	28-pin DIP	Monolithic	0 to + 70	
					– 55 to + 125	
0.01%	± 15V	± 35V	16-pin DIP	Monolithic	0 to + 70	248
					– 55 to + 125	
0.01%	± 15V	± 17V	18-pin DIP	Monolithic	0 to + 70	252
					– 55 to + 125	
0.01%	± 15V	± 35V	28-pin DIP	Monolithic	0 to + 70	248
					– 55 to + 125	
0.01%	± 15V	± 17V	28-pin DIP	Monolithic	0 to + 70	252
					– 55 to + 125	
0.01%	± 15V	± 35V	16-pin DIP	Monolithic	0 to + 70	248
					– 55 to + 125	
0.01%	± 15V	± 35V	28-pin DIP	Monolithic	0 to + 70	
					– 55 to + 125	

Low ON-Resistance CMOS Analog Multiplexers MV Series

FEATURES

- **Low ON Resistance**
- **Break-Before-Make Switching**
- **Dielectrically Isolated CMOS**
- **Single Ended or Differential**
- **Fast Settling Time**
- **DTL/TTL/CMOS Compatible**

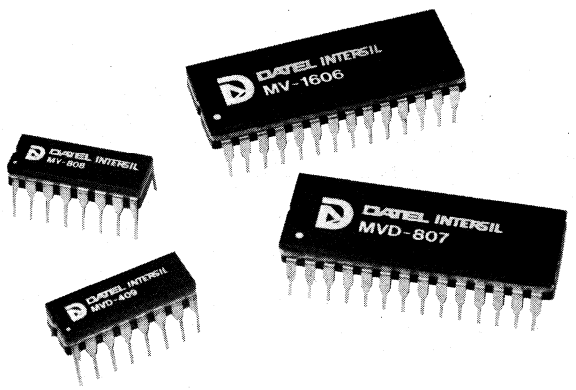
GENERAL DESCRIPTION

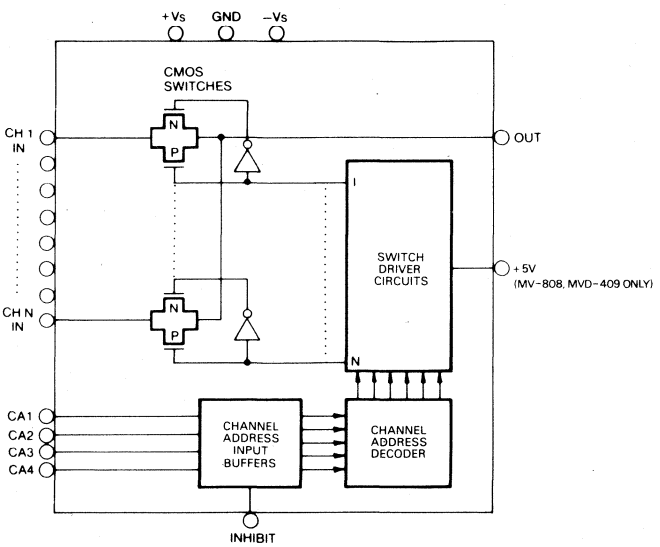
The MV series analog multiplexers are 4, 8, and 16 channel monolithic devices featuring a low ON resistance of 270 ohms. These units are manufactured with CMOS technology using a dielectric isolation process. There are 8 and 16 channel single-ended models and 4 and 8 channel differential models in this series. Channel addressing is done by a 2, 3, or 4 bit binary code; an inhibit input enables or disables the entire device to permit expansion of the number of channels by using several devices together. Another important feature is break-before-make switching, which insures that no two channels are ever momentarily shorted together.

With a high impedance load, transfer accuracies of 0.01% can be achieved at channel sampling rates up to 350 KHz. These multiplexers are ideal for multi-channel data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. The channel ON resistance is less than 500 ohms over full operating temperature range.

These multiplexers are packaged in 16 pin and 28 pin ceramic DIP's. Standard versions operate over 0 to 70°C while military versions operate from -55°C to +125°C. The MV series is similar in specification to Datel's MX series multiplexers. The MX series is recommended where input overvoltage protection to 20 volts above supply voltage is required and where higher channel ON resistance can be tolerated.

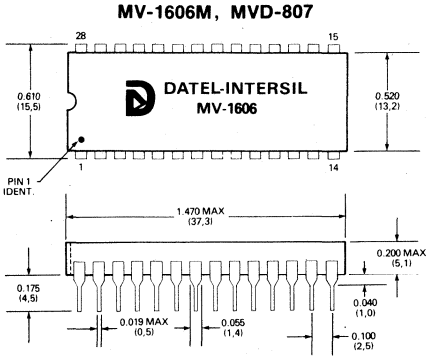
CAUTION:
These multiplexers are CMOS devices and should be handled with anti-static precautions until installed in a circuit with leakage return paths.



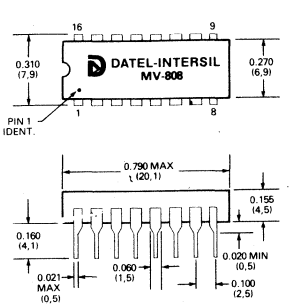


MECHANICAL DIMENSIONS - INCHES (MM)

MV-1606M, MVD-807



MV-808, MVD-409



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SPECIFICATIONS

Typical at ±15V supplies (and +5V supply for MV-808 & MVD-409), unless otherwise noted.

	MV-808 MV-808M	MV-1606 MV-1606M	MVD-409 MVD-409M	MVD-807 MVD-807M
MAXIMUM RATINGS				
Power Supply, analog	±20V	±20V	±20V	±20V
Power Supply, digital	+30V	—	+30V	—
Analog Input Voltage	±|Vs+2V|	±|Vs+2V|	±|Vs+2V|	±|Vs+2V|
Digital Input Voltage	±Vs	±|Vs+4V|	±Vs	±|Vs+4V|
Package Dissipation, max.	780mW	1200mW	780mW	1200mW
ANALOG INPUTS				
Number of Channels	8	16	4	8
Type	Single Ended	Single Ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance[1]	250Ω	270Ω	250Ω	270Ω
Channel ON Resistance[2], max. over temp.	500Ω	500Ω	500Ω	500Ω
Channel OFF Input Leakage	20pA	30pA	20pA	30pA
Channel OFF Output Leakage	100pA	1.0nA	50pA	1.0nA
Channel ON Leakage	100pA	1.0nA	50pA	1.0nA
Channel OFF Input Capacitance	4pF	4pF	4pF	4pF
Channel OFF Output Capacitance	20pF	44pF	10pF	22pF
DIGITAL INPUTS[3]				
Logic "0" Threshold, max.	+0.4V	+0.8V	+0.4V	+0.8V
Logic "1" Threshold,[4] min.	+4.0V	+2.4V	+4.0V	+2.4V
Input Current, max., HI or LO	1μA	5μA	1μA	5μA
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, all channels OFF	Logic "1"	Logic "0"	Logic "1"	Logic "0"
PERFORMANCE				
Transfer Error, max.	0.01%	0.01%	0.01%	0.01%
Crosstalk, 10KHz	-86dB	-86dB	-86dB	-86dB
Common Mode Rejection	—	—	120dB	120dB
Settling Time, 20V to 0.1%	1.1 μsec.	1.2 μsec.	1.1 μsec.	1.2 μsec.
Settling Time, 20V to 0.01%	2.8 μsec.	2.4 μsec.	2.8 μsec.	2.4 μsec.
Turn ON Time	350 nsec.	300 nsec.	350 nsec.	300 nsec.
Turn OFF Time	250 nsec.	220 nsec.	250 nsec.	220 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break-Before-Make Delay	100 nsec.	80 nsec.	100 nsec.	80 nsec.
POWER REQUIREMENT				
Power Supply Voltage	±15VDC	±15VDC	±15VDC	±15VDC
Power Supply Current,[5] max.	+1, -2mA	+5, -2mA	+1, -2mA	+5, -2mA
Digital Supply Voltage	+5VDC	—	+5VDC	—
Digital Supply Current, max.	2mA	—	2mA	—
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range, standard version	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
Operating Temp. Range, military, version	-55° to +125°C	-55° to +125°C	-55° to +125°C	-55° to +125°C
Storage Temperature Range	-65° to +150°C	-65° to +150°C	-65° to +150°C	-65° to +150°C
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP

NOTES:
1. For MV-1606M & MVD-807M typical value is 170 ohms.
2. For MV-1606M & MVD-807M max. value is 400 ohms.
3. Channel address and inhibit inputs.
4. For MV-808 and MVD-409; to drive from DTL/TTL logic 1K pull-up resistors to +5V should be used.
5. For MV-1606M & MVD-807M max. current is +3, -1 mA. For MV-808M & MVD-409M max. current is +0.5, -1 mA for analog supply, 1mA for digital supply.

CONNECTION AND APPLICATION

CHANNEL ADDRESSING

MV-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MV-808, MVD-807

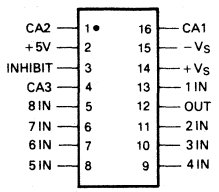
4	2	1	MVD-807 INHIB.	MV-808 INHIB.	ON CHANNEL
X	X	X	0	1	NONE
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8

MVD-409

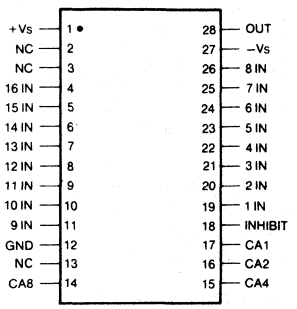
2	1	INHIB.	ON CHANNEL
X	X	1	NONE
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

PIN CONNECTIONS

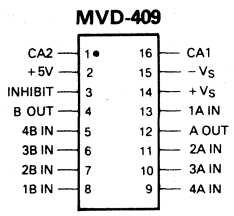
MV-808



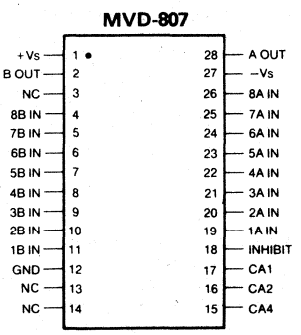
MV-1606



MVD-409



MVD-807



NOTES:

CA = CHANNEL ADDRESS
VS = SUPPLY VOLTAGE
NC = NO CONNECTIONS

TOP VIEW SHOWN

TECHNICAL NOTES

1. The transfer accuracy of the MV series multiplexers depends on both the source resistance and load resistance. For example, with zero source resistance and assuming 500 ohms max. channel ON resistance, the load impedance must be at least 5 megohms to achieve 0.01% accuracy. In practice it is recommended that a load impedance of 10^8 ohms or more be used. This is a typical input impedance value for most IC operational amplifiers connected in the follower mode (see Datel's AM-400 series) or for IC sample-holds (see Datel's SHM-1C-1, SHM-LM-2, or SLM-20). Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 250 ohms is recommended.

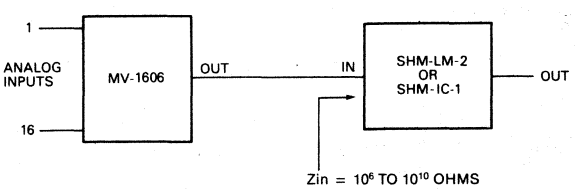
2. For differential operation either two unity gain buffers or an instrumentation amplifier (such as Datel's AM-551 is recommended as the output load. To maintain high CMR, source impedance unbalance must be kept to a minimum, and amplifiers with high CMR should be used.

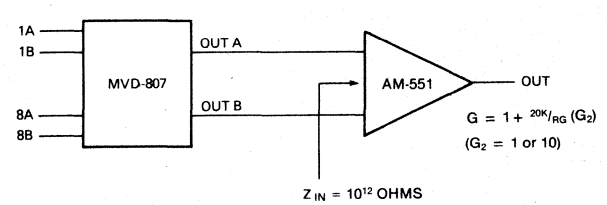
3. The maximum analog input overvoltage for the MV series is ±|Vs+2V|. The maximum digital input voltage is ±Vs. It should be noted that the logic (channel address) inputs are protected with resistors and clamp diodes but the analog inputs are not. Because the analog inputs are not protected, the low ON resistance is achieved.

4. Channel expansion is accomplished by use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

5. For the MV-808 and MVD-409 it is recommended that 1K pull-up resistors to the +5V logic supply be used when the logic inputs are driven from DTL or TTL circuits. Only these two models require a +5V logic supply.

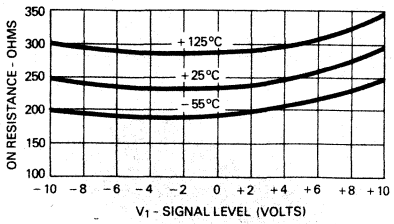
CIRCUIT CONNECTIONS



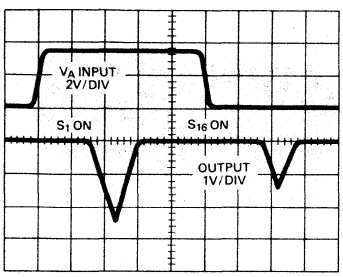


PERFORMANCE GRAPHS

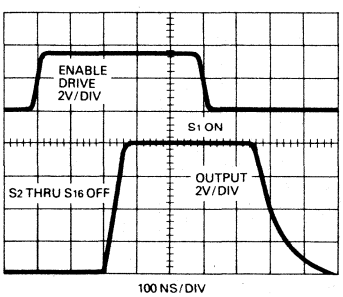
ON RESISTANCE VS. TEMPERATURE



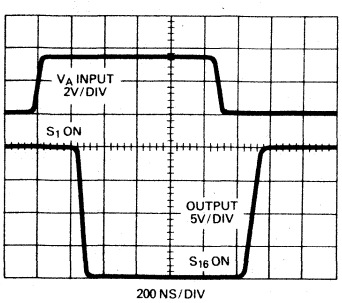
BREAK-BEFORE-MAKE DELAY
(t_{OPEN})



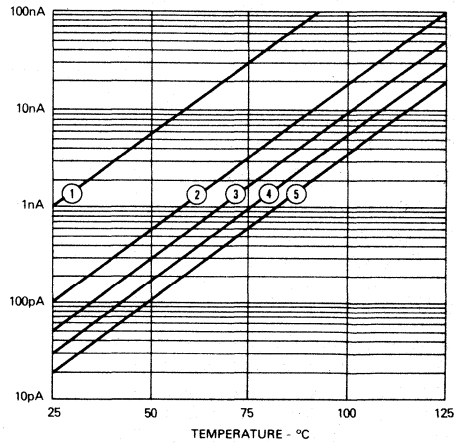
ENABLE DELAY
($t_{ON(EN)}$, $t_{OFF(EN)}$)



ACCESS TIME

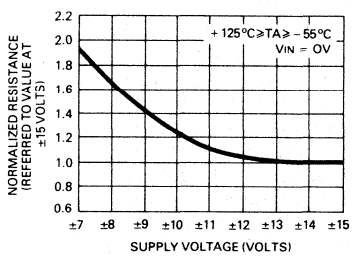


LEAKAGE CURRENT VS. TEMPERATURE



1. MV-1606, MVD-807 CHANNEL OFF OUTPUT LEAKAGE
2. MV-808 CHANNEL OFF OUTPUT LEAKAGE
3. MVD-409 CHANNEL OFF INPUT LEAKAGE
4. MV-1606, MVD-807 CHANNEL OFF INPUT LEAKAGE
5. MV-808, MVD-409 CHANNEL OFF INPUT LEAKAGE

NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE	PRICE (1-24)
MV-808	8 S.E.	0 to 70C	
MV-808M	8 S.E.	-55 to +125C	
MV-1606	16 S.E.	0 to 70C	
MV-1606M	16 S.E.	-55 to +125C	
MVD-409	4 Diff.	0 to 70C	
MVD-409M	4 Diff.	-55 to +125C	
MVD-807	8 Diff.	0 to 70C	
MVD-807M	8 Diff.	-55 to +125C	

THESE MULTIPLEXERS ARE COVERED BY GSA CONTRACT

4, 8, and 16 Channel CMOS Multiplexers MX Series

FEATURES

- **Dielectrically Isolated CMOS**
- **Break-Before-Make Switching**
- **Single-Ended and Differential**
- **Overvoltage Protection**
- **DTL/TTL/CMOS Compatible**
- **7.5 mW Standby Power**

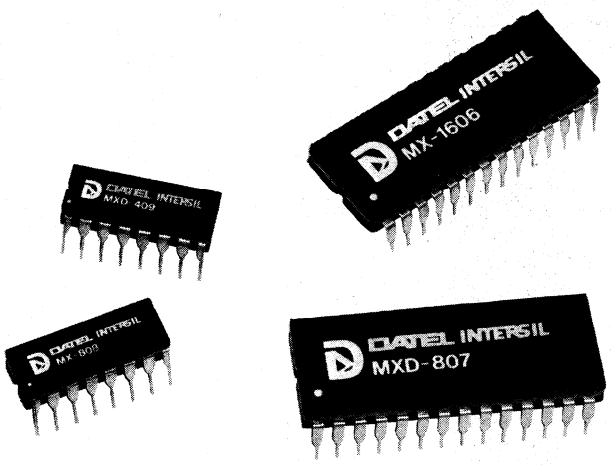
GENERAL DESCRIPTION

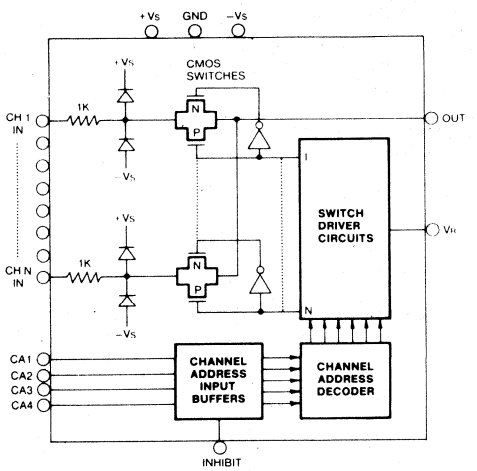
The MX series analog multiplexers are 4, 8, and 16 channel monolithic devices manufactured with a dielectrically isolated complementary MOS process. The circuits incorporate analog and digital input protection which protects the units from both overvoltage and loss of power. The digital inputs are DTL/TTL/CMOS compatible and address the proper channel by means of a 2, 3, or 4 bit binary code. An inhibit input enables or disables the entire device and thus permits expansion of the number of channels by using several devices together. Another important feature of these multiplexers is the use of break-before-make switching to insure that no two channels are ever momentarily shorted together.

Transfer accuracies of .01% can be achieved at channel sampling rates up to 200 kHz and over ±10V signal ranges. These multiplexers are ideal for multi-channel data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. Channel ON resistance is typically 1.5K at 25°C and is less than 2K over the operating temperature range.

Power consumption is only 7.5 mW at standby and 15 mW at 100 kHz switching rate. Power supply range is ±5V to ±20V. The devices are packaged in 16 pin or 28 pin DIP's and operate over the 0°C to 70°C temperature range.

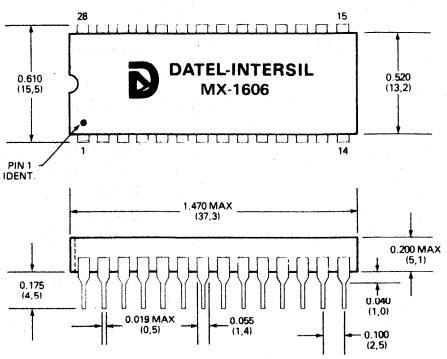
CAUTION: These are CMOS devices and may be damaged by static discharge. Standard anti-static precautions should be taken to prevent possible damage.



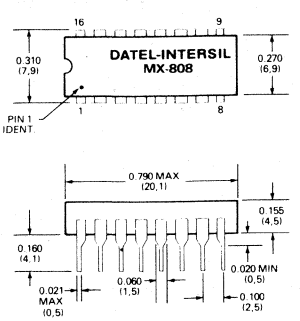


MECHANICAL DIMENSIONS — INCHES (MM)

MX-1606M, MXD-807



MX-808, MXD-409



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS MX-808 & MXD-409

Typical at 25°C, ±15V supplies, R source <1K, unless otherwise noted

	MX-808 MX-808M	MX-1606 MX-1606M	MXD-409 MXD-409M	MXD-807 MXD-807M
MAXIMUM RATINGS				
Voltage Between Supply Pins	40V	40V	40V	40V
V_{REF} to Ground, V+ to Ground	+20V	+20V	+20V	+20V
Digital Input Overvoltage	±|Vs +4V|	±|Vs +4V|	±|Vs +4V|	±|Vs +4V|
Analog Input Overvoltage	±|Vs +20V|	±|Vs +20V|	±|Vs +20V|	±|Vs +20V|
Package Dissipation, max.	725 mW	1200 mW	725 mW	1200 mW
ANALOG INPUTS				
Number/Type of Channels	8 Single-end	16 Single-end	4 Differential	8 Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance	1.5 KΩ	1.5 KΩ	1.5 KΩ	1.5 KΩ
Channel ON Resistance, Over Temp	2.0 KΩ, max.	2.0 KΩ, max.	2.0 KΩ, max.	2.0 KΩ, max.
Channel OFF Input Leakage	30 pA	30 pA	30 pA	30 pA
Channel OFF Output Leakage	1.0 nA	1.0 nA	1.0 nA	1.0 nA
Channel ON Leakage	100 pA	100 pA	100 pA	100 pA
Channel OFF Input Capacitance	5 pF	5 pF	5 pF	5 pF
Channel OFF Output Capacitance	25 pF	50 pF	12 pF	25 pF
DIGITAL INPUTS[1]				
Logic "0" Threshold	+0.8V, max.	+0.8V, max.	+0.8V, max.	+0.8V, max.
Logic "1" Threshold, (TTL)[2]	+4.0V, min.	+4.0V, min.	+4.0V, min.	+4.0V, min.
Logic "1" Threshold, (CMOS)[3]	+6.0V, min.	+6.0V, min.	—	—
Input Current, High or Low	5 μA, max.	5 μA, max.	5 μA, max.	5 μA, max.
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, All Channels OFF	Logic "0"	Logic "0"	Logic "0"	Logic "0"
PERFORMANCE				
Transfer Error, max.	.01%	.01%	.01%	.01%
Crosstalk, 1 KHz	.005%	.005%	.005%	.005%
Common Mode Rejection	—	—	120 dB	120 dB
Settling Time[4], 20V step to 0.1%	2 μsec	2 μsec	2 μsec	2 μsec
Settling Time[4], 20V Step to 0.01%	3 μsec	3 μsec	3 μsec	3 μsec
Turn ON Time	500 nsec.	500 nsec.	500 nsec.	500 nsec.
Turn OFF Time	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break Before Make Delay	80 nsec.	80 nsec.	80 nsec.	80 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
POWER REQUIREMENT				
Rated Power Supply Voltage	±15 VDC	±15 VDC	±15 VDC	±15 VDC
Power Supply Voltage Range	±5V to ±20V	±5V to ±20V	±5V to ±20V	±5V to ±20V
Quiescent Current, max.	+5, −2 mA	+5, −2 mA	+5, −2 mA	+5, −2 mA
Power Consumption, 10 KHz Sampling	7.5 mW	7.5 mW	7.5 mW	7.5 mW
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range, Standard Models	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
Operating Temp. Range, M Suffix Models	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP

NOTES:

1. The digital inputs are the channel address inputs and the inhibit input.
2. To drive from DTL/TTL circuits, 1K pull-up resistors to +5V are recommended. With models MX-1606 and MXD-807, pin 13 should be left open.
3. For a +6.0V threshold with models MX-1606 and MXD-807, pin 13 is connected to +10V.
4. With a load impedance of >100 megohms in parallel with 2 pF.

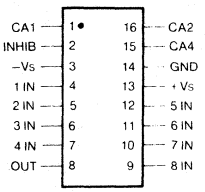
ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE	PRICE (1-24)
MX-808	8 S.E.	0°C to 70°C	
MX-808M	8 S.E.	−55°C to +125°C	
MX-1606	16 S.E.	0°C to 70°C	
MX-1606M	16 S.E.	−55°C to +125°C	
MXD-409	4 Diff.	0°C to 70°C	
MXD-409M	4 Diff.	−55°C to +125°C	
MXD-807	8 Diff.	0°C to 70°C	
MXD-807M	8 Diff.	−55°C to +125°C	

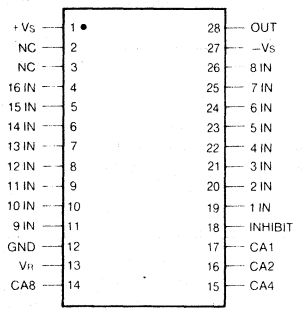
CONNECTION & APPLICATION

PIN CONNECTIONS

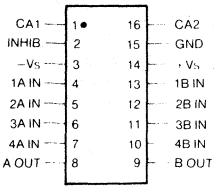
MX-808



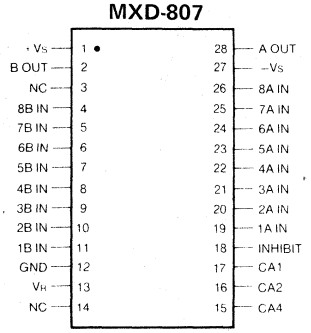
MX-1606



MXD-409



MXD-807



NOTES:

CA CHANNEL ADDRESS
V_S SUPPLY VOLTAGE
V_R REFERENCE VOLTAGE
NC NO CONNECTIONS

CHANNEL ADDRESSING

MX-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MX-808, MXD-807

4	2	1	INHIB.	ON CHANNEL
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

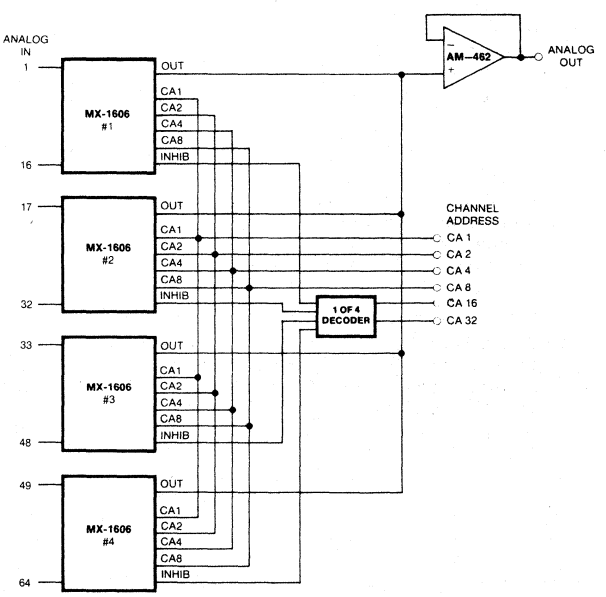
MXD-409

2	1	INHIB.	ON CHANNEL
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TECHNICAL NOTES

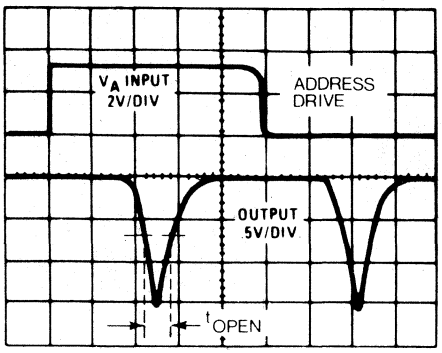
1. The transfer accuracy of these multiplexers depends on both the source resistance and the load resistance. With zero source resistance, and assuming 2K ohms max. channel ON resistance, the load impedance should be at least 20 megohms to achieve .01% accuracy. In practice it is recommended that a load impedance of at least 100 megohms be used to minimize errors. This can be done by using a good high gain, high CMR operational amplifier as a buffer (such as Datel's AM-462). Source resistance should be kept as low as possible so that accuracy is not affected; less than 1K ohms is recommended. Higher source resistance, in addition to affecting accuracy, will degrade the settling time of the multiplexer.
2. For differential operation two buffer amplifiers or a good quality instrumentation amplifier (such as Datel's AM-201) should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used, and an amplifier with high CMR should be chosen.
3. The maximum analog input overvoltage for these models is $\pm$ | Vs +20V | . Maximum logic input overvoltage is $\pm$ | Vs +4V | .
4. Channel expansion is accomplished by use of the inhibit input of the multiplexer. A logic "0" on this input disables the multiplexer. The expansion technique shown in the diagram to the right applies to all of the multiplexer models.
5. The reference terminal (V_R) sets the noise immunity level of the input logic for models MX-1606 and MXD-807. In most cases this terminal is left open (TTL inputs). For higher level inputs (+6V min.) this terminal should be connected to +10V. When addressing from DTL/TTL logic it is recommended that 1K ohm pull-up resistors to the +5V supply be used.

EXPANSION TO 64 CHANNELS

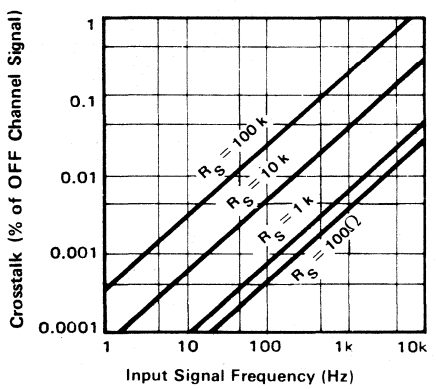


PERFORMANCE GRAPHS

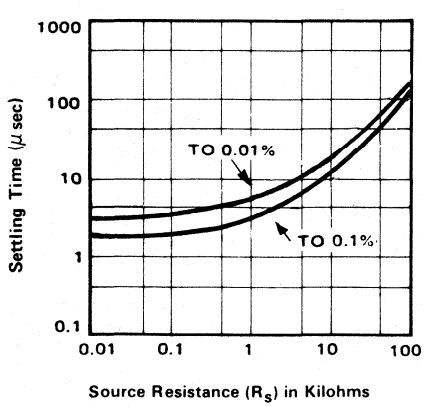
BREAK-BEFORE-MAKE DELAY (t OPEN)



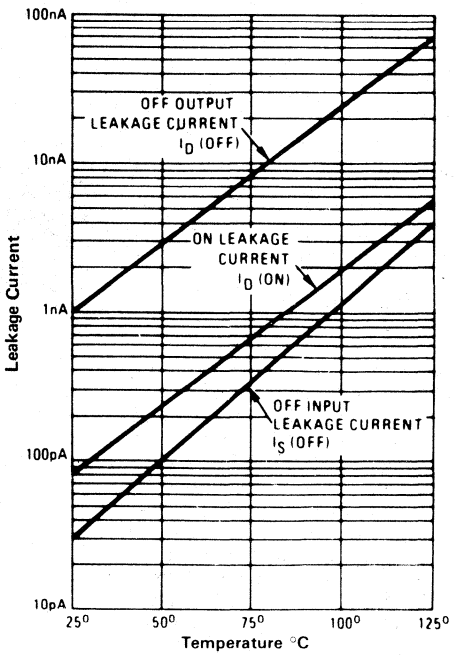
CROSSTALK VS. FREQUENCY OF INPUT SIGNAL



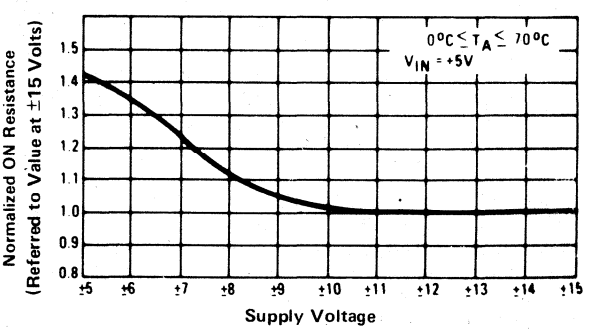
SETTLING TIME VS. SOURCE RESISTANCE (20V STEP)



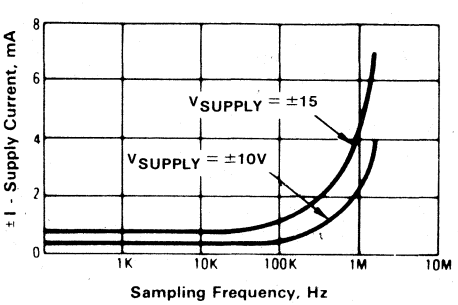
LEAKAGE CURRENT VS. TEMP.



NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. SAMPLING FREQUENCY



NEW

DATEL

High Speed CMOS Analog Multiplexers MX-1616, MX-818

FEATURES

- 400 nsec Settling Time
- Programmable Input Mode
- Break-Before-Make Switching
- Dielectrically Isolated CMOS
- TTL/CMOS Compatible

GENERAL DESCRIPTION

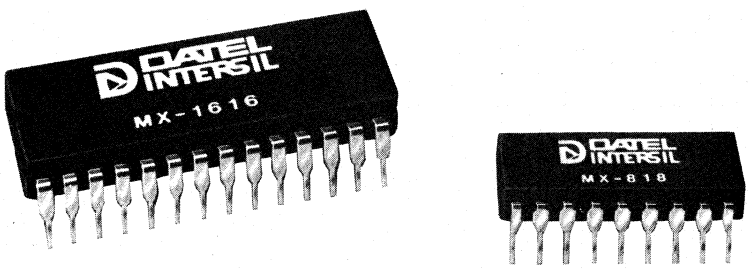
The MX-1616 and MX-818 are high speed, high performance analog multiplexers manufactured with a dielectrically isolated CMOS process. Both devices achieve transfer accuracies of 0.01% at channel sampling rates of up to 2.50 MHz over ±10V signal ranges. These multiplexers are ideal for high speed, multi-channel, data-acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier or instrumentation amplifier. Channel ON resistance is 750Ω maximum at +25°C and only 1KΩ maximum over the full operating temperature range. The channel OFF Output Leakage current is typically only 35pA for the MX-1616 and 100pA for the MX-818.

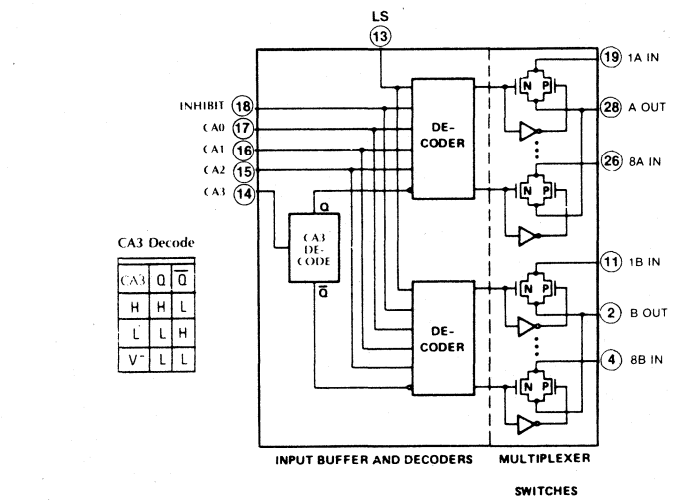
A unique feature of these circuits is the ability of the user to program their inputs for either single-ended or differential operation. The MX-1616 is user programmable either as a single ended 16-channel or as a differential 8-channel multiplexer while the MX-818 is user programmable either as a single-ended 8-channel or as a differential 4-channel multiplexer.

Digital inputs are user selectable for either TTL or CMOS compatibility. The proper channel is addressed by means of a 3 or 4 bit binary word. An inhibit function enables or disables the entire device, permitting expansion of the number of channels by using several devices together. Another important feature of these devices is the use of break-before-make switching to insure that no two channels are ever momentarily shorted together.

These multiplexers are packaged in 18 pin and 28 pin ceramic DIPS. Commercial versions operate over the 0°C to +70°C operating temperature range while military versions are specified over the −55 to +125°C operating temperature range.

CAUTION: These multiplexers are CMOS devices and should be handled with anti-static precautions until installed in a circuit with anti-static return paths.

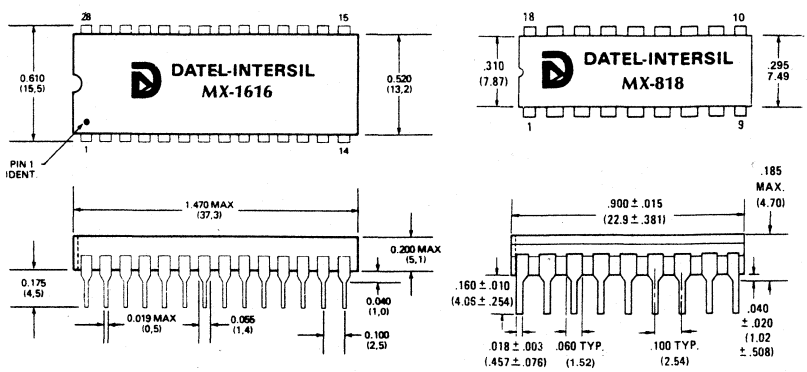




CA3 Decode

CA3	Q	$\overline{Q}$
H	H	L
L	L	H
V⁻	L	L

MECHANICAL DIMENSIONS — INCHES (MM)



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, MX-1616, MX-818
(Typical at +25°C, ±15 VDC supplies, unless otherwise noted)

	MX-1616	MX-818
MAXIMUM RATINGS		
Voltage Between Supply Pins	33V	*
Analog Input Voltage	$\pm(V_S+2V)$	*
Digital Input Voltage:		
TTL[1]	CA3 = $(-V_S-2V)$ −6V < Logic "1" < +6V	CA2 = $(-V_S-2V)$ *
CMOS[2]	$+V_S+2V$ GRND −2V	* *
Package Dissipation, max.	1200 mW	725 mW
ANALOG INPUTS		
No. of Channels	16 Single Ended 8 Differential	8 Single Ended 4 Differential
Input Voltage Range	±15V	*
Channel ON Resistance, max.[3]	750Ω	*
Channel ON Res. over Temp., max[3]	1 KΩ	*
Channel OFF Input Leakage	10 pA	50 pA
Channel OFF Output Leakage	35 pA	100 pA
Channel ON Leakage	40 pA	100 pA
Channel OFF Input Capacitance	2.5 pF	1.9 pF
Channel OFF Output Capacitance	18 pF	10 pF
DIGITAL INPUTS		
Logic "0" Threshold, max: TTL	+0.8V	*
CMOS	+0.3V	*
Logic "1" Threshold, min: TTL	+2.4V	*
CMOS	0.7 (Logic sup.)	*
Input Leakage Current, max: High	1 μA	*
Low	25 μA	20 μA
Channel Address Coding	4 Bits	3 Bits
Channel Inhibit, All Channels OFF	Logic "0"	*
PERFORMANCE		
Transfer Error, max.	0.01%	*
Settling Time, 20V step to 0.1%	200 nsec	*
20V step to 0.01%	400 nsec	*
Access Time, max.	150 nsec[4]	125 nsec[5]
Enable Delay "ON", max.	150 nsec	*
Enable Delay "OFF", max.	125 nsec	*
Break Before Make Delay	20 nsec	*
POWER REQUIREMENT		
Rated Power Supply Voltage	±15V	*
Quiescent Current max.[6]	±30 mA	±18 mA
Power Dissipation, max.	900 mW	540 mW
PHYSICAL — ENVIRONMENTAL		
Operating Temp. Range:		
C Suffix	0°C to +70°C	*
M Suffix	−55°C to +125°C	*
Storage Temperature Range	−65°C to +155°C	*
Package	28 Pin DIP	18 Pin DIP

* Same specification as column 1

NOTES

1. For TTL compatibility, the Logic Select pin (MX-1616 Pin 13, MX-818 Pin 8) is grounded or left open.
2. For CMOS compatibility, the Logic Select Pin (MX-1616 Pin 13, MX-818 Pin 8) is tied to the system Logic Supply.
3. Vin = ±10V, Iout = −100μA.
4. 200 nsec maximum at full rated operating temperature.
5. 150 nsec maximum at full rated operating temperature.
6. Specifications are given for commercial versions. Maximum quiescent current for MX-1616M is ±25mA and MX-818M is ±15mA.

TECHNICAL NOTES

1. The transfer accuracy of the MX-1616 and MX-818 depends upon both the source and the load resistance. With zero source resistance and assuming 1KΩ max. channel on resistance the load impedance must be at least 10MΩ to achieve 0.01% accuracy. This can be done by using a good high gain, high CMR operational amplifier as a buffer (such as Datel's AM-410). Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 500Ω is recommended.
2. For differential operation, two buffer amplifiers or a good instrumentation amplifier (such as Datel's AM-201) should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used and an amplifier with high CMR should be chosen.
3. These devices have the added feature of being programmable for single-ended or differential operation. The MX-1616 is user programmed for single-ended 16 channel operation by connecting A out (Pin 28) to B out (Pin 2) and using CA3 (Pin 14) as a digital address input. To program the MX-1616 for differential 8 channel operation, CA3 (Pin 14) is simply connected to $-V_S$ (Pin 27). The MX-818 may be programmed as a single ended 8 channel multiplexer by connecting A out (Pin 18) to B out (Pin 2) and using CA2 (Pin 9) as a digital input address, or as a differential 4 channel multiplexer by connecting CA2 (Pin 9) to $-V_S$ (Pin 17). Refer to the truth tables for channel addressing information.
4. Both devices are selectable for either TTL or CMOS compatibility. For TTL compatibility, the Logic Select Pin (MX-1616 Pin 13, MX-818 Pin 8) is left open or grounded. For CMOS compatibility, the Logic Select Pin should be connected to the system Logic Supply.
5. Channel expansion is accomplished by the use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE	PRICE
MX-818C	8 S.E. or 4 Diff.	0 to +70°C	
MX-818M	8 S.E. or 4 Diff.	−55 to +125°C	
MX-1616C	16 S.E. or 8 Diff.	0 to +70°C	
MX-1616M	16 S.E. or 8 Diff.	−55 to +125°C	

CONNECTION & APPLICATION

MX-1616 - USED AS 16 CHANNEL MULTIPLEXER

USE CA3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
3	2	1	0	INHIB.	OUPUT A	OUTPUT B
X	X	X	X	0	NONE	NONE
0	0	0	0	1	1A	———
0	0	0	1	1	2A	———
0	0	1	0	1	3A	———
0	0	1	1	1	4A	———
0	1	0	0	1	5A	———
0	1	0	1	1	6A	———
0	1	1	0	1	7A	———
0	1	1	1	1	8A	———
1	0	0	0	1	———	1B
1	0	0	1	1	———	2B
1	0	1	0	1	———	3B
1	0	1	1	1	———	4B
1	1	0	0	1	———	5B
1	1	0	1	1	———	6B
1	1	1	0	1	———	7B
1	1	1	1	1	———	8B

MX-1616 - USED AS DUAL 8 CHANNEL MULTIPLEXER

CONNECT CA3 TO −V SUPPLY				ON CHANNEL TO	
2	1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	X	0	NONE	NONE
0	0	0	1	1A	1B
0	0	1	1	2A	2B
0	1	0	1	3A	3B
0	1	1	1	4A	4B
1	0	0	1	5A	5B
1	0	1	1	6A	6B
1	1	0	1	7A	7B
1	1	1	1	8A	8B

MX-818 - USED AS 8 CHANNEL MULTIPLEXER

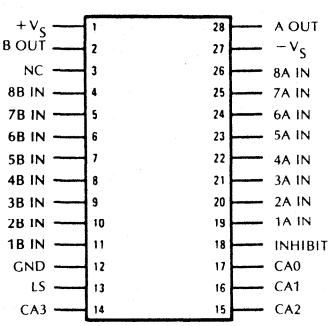
USE CA2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
2	1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	X	0	NONE	NONE
0	0	0	1	1A	———
0	0	1	1	2A	———
0	1	0	1	3A	———
0	1	1	1	4A	———
1	0	0	1	———	1 B
1	0	1	1	———	2 B
1	1	0	1	———	3 B
1	1	1	1	———	4 B

MX-818 - USED AS DUAL 4 CHANNEL MULTIPLEXER

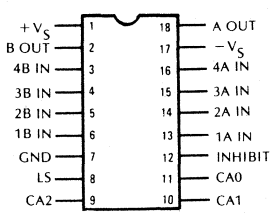
CONNECT CA2 TO −V SUPPLY			ON CHANNEL TO	
1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	0	NONE	NONE
0	0	1	1	1B
0	1	1	2	2B
1	0	1	3	3B
1	1	1	4	4B

PIN CONNECTIONS

MX-1616



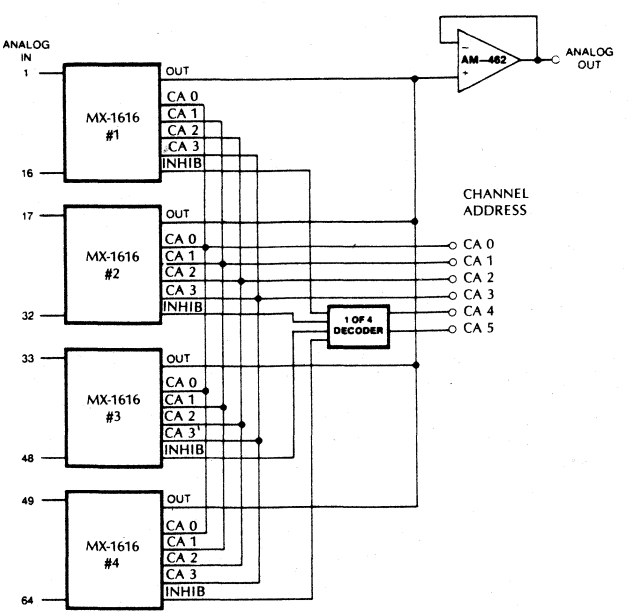
MX-818



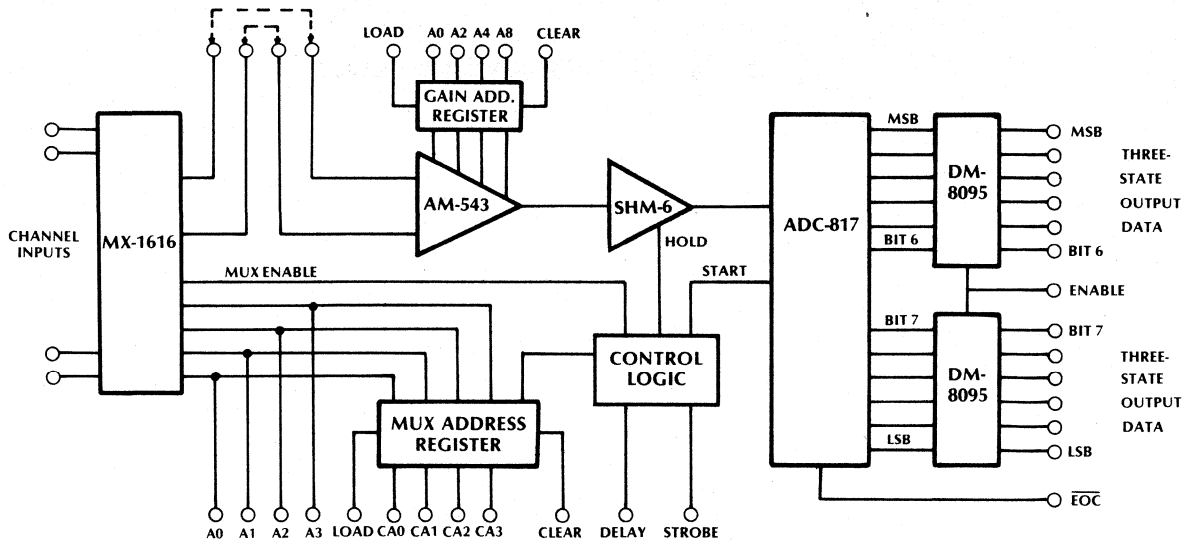
NOTES:

CA	CHANNEL ADDRESS
V_S	SUPPLY VOLTAGE
LS	LOGIC SELECT
NC	NO CONNECTION

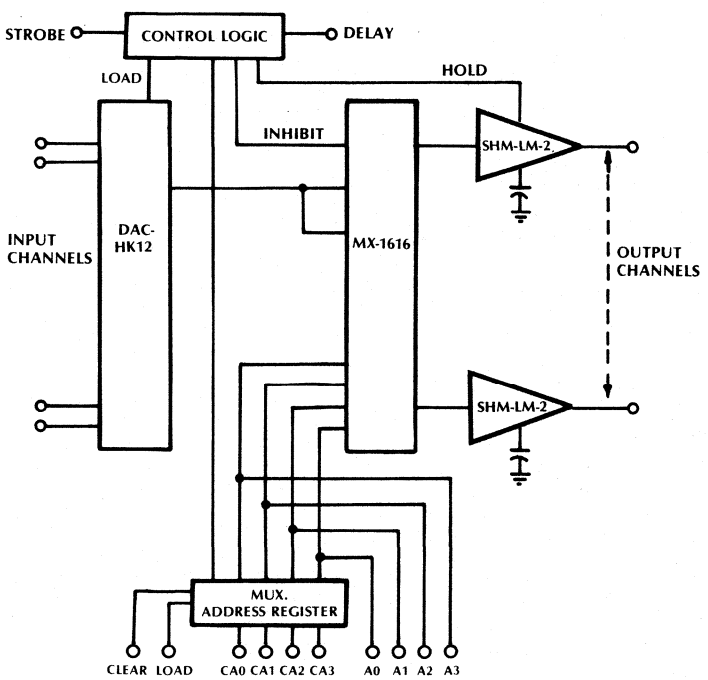
EXPANSION TO 64 CHANNELS



APPLICATION



NOTE: A high speed data acquisition system with 8 differential inputs and 12 bit resolution that utilizes the MX-1616. If the control logic is timed so that the Sample-Hold-A/D section is converting one analog value while the MUX-Amplifier section is allowed to settle to the next input value, throughput rates greater than 156 KHz can be achieved. The MX-1616 is used with Datel-Intersils' AM-543, a high speed digitally programmable gain amplifier, the ADC-817, a 12 bit hybrid A/D with a 2 μsec conversion rate, and the SHM-6, a 0.01%, 1 μsec hybrid sample-hold.



NOTE: The switches in a CMOS multiplexer will conduct equally well in either direction, making it feasible to use them as single input-selected multiple output switches. The circuit shown is capable of sample rates of 78 KHz for inputs of ±10V. The MX-1616 is used with Datel-Intersil's DAC-HK12, a 12 bit hybrid D/A with input registers and the SHM-LM-2, a low cost monolithic sample-hold.

Data Acquisition Systems

DATA ACQUISITION SYSTEM: A system consisting of analog multiplexers, sample-holds, A/D converters, and other circuits which process one or more analog signals and conver them into digital form for use by a computer.

Data Acquisition Systems

Introduction

Data acquisition and conversion systems interface between the real world of physical parameters, which are analog, and the artificial world of digital computation and control. With current emphasis on digital systems, the intefacing function has become an important one; digital systems are used widely because complex circuits are low cost, accurate, and relatively simple to implement. In addition, there is rapid growth in use of mini-computers and microcomputers to perform difficult digital control and measurement functions.

Computerized feeback control systems are used in many different industries today in order to achieve greater productivity in our modern industrial society. Industries which presently employ such automatic systems include steel making, food processing, paper production, oil refining, chemical manufacturing, textile production, and cement manufacturing.

The devices which perform the interfacing function between analog and digital worlds are analog-to-digital (A/D) and digital-to-analog (D/A) converters, which together are known as data converters. Some of the specific applications in which data converters are used include data telemetry systems, pulse code modulated communications, automatic test systems, computer display systems, video signal processing systems, data logging systems, and sampled-data control systems. In addition, every laboratory digital multimeter or digital panel meter contains an A/D converter.

Besides A/D and D/A converters, data acquisition and distribution systems may employ one or more of the following circuit functions:

Basic Data Distribution Systems

Transducers
Amplifiers
Filters
Nonlinear Analog Functions
Analog Multiplexers
Sample-Holds

The interconnection of these components is shown in the diagram of the data acquisition portion of a computerized feedback control system in Figure 1.

The input to the system is a *physical parameter* such as temperatue, pressure, flow, acceleration, and position, which are analog quantities. The parameter is first converted into an electrical signal by means of a *transducer;* once in electrical form, all further processing is done by electronic circuits.

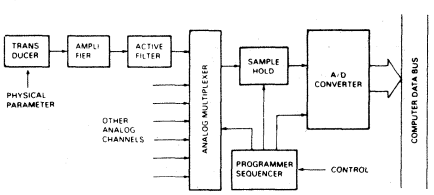


Figure 1. Data Acquisition System

Next, an *amplifier* boosts the amplitude of the transucer output signal to a useful level for further processing. Transducer outputs may be microvolt or millivolt level signals which are then amplified to 1 to 10 volt levels. Furthermore, the transducer output may be a high impedance signal, a differential signal with common-mode noise, a current output, a signal superimposed on a high voltage, or a combination of these. The amplifier, in order to convert such signals into a high level voltage, may be one of several specialized types.

The amplifier is frequently followed by a low pass *active filter* which reduces high frequency signal components, unwanted electrical interference noise, or electronic noise from the signal. The amplifier is sometimes also followed by a special *nonlinear analog function* circuit which performs a nonlinear operation on the high level signal. Such operations include squaring, multiplication, division, RMS conversion, log conversion, or linearization.

The processed analog signal next goes to an *analog multiplexer* which sequentially switches between a number of different analog input channels. Each input is in turn connected to the output of the multiplexer for a specified period of time by the multiplexer switch. During this connection time a *sample-hold* circuit acquires the signal voltage and then holds its value while an *analog-to-digital converter* converts the value into digital form. The resultant digital word goes to a computer data bus or to the input of a digital circuit.

Thus the analog multiplexer, together with the sample-hold, time shares the A/D converter with a number of analog input channels. The timing and control of the complete data acquisition system is done by a digital circuit called a *programmer-sequence,* which in turn is under control of the computer. In some cases the computer itself may control the entire data acquisition system.

While this is perhaps the most commonly used data acquisition system configuration, there are alternative ones. Instead of multiplexing high-leve signals, low-level multiplexing is sometimes used with the amplifier following the multiplexer. In such cases just one amplifier is required, but its gain may have to be changed from one channel to the next during multiplexing. Another method is to amplify and convert the signal into digital form at the transducer location and send the digital information in serial form to the computer. Here the digital data must be converted to parallel form and then multiplexed onto the computer data bus.

DATA ACQUISITION SUBSYSTEMS

Quick selection: Data acquisition subsystems

	MODEL	DESCRIPTION	RESOLUTION	CHANNELS NO.	CHANNELS TYPE	THROUGH-PUT RATE	LINEARITY ERROR MAX	GAIN RANGE
	DAS-250A DAS-250B	High Speed Complete DAS	12 Bits	16	Single Ended	250 kHz	± ½ LSB	——
	DAS-952R	CMOS, Monolithic DAS	8 Bits	16	Single Ended	17 kHz	± ½ LSB	——
	HDAS-8MC HDAS-8MR HDAS-8MM	Complete Hybrid DAS	12 Bits	8	Diff.	50 kHz	± ½ LSB	1 to 1000
	HDAS-16MC HDAS-16MR HDAS-16MM	Complete Hybrid DAS	12 Bits	16	Single Ended	50 kHz	± ½ LSB	1 to 1000
	MDAS-8D	Low Cost Modular DAS	12 Bits	8	Diff.	50 kHz	± ½ LSB	——
	MDAS-16	Low Cost Modular DAS	12 Bits	16	Single Ended	50 kHz	± ½ LSB	——
NEW	MDAS-940D	Digitally Controlled P.G.A.	12 Bits	8	Diff.	33 kHz	± ½ LSB	1, 2, 4, 8
NEW	MDAS-940S	Digitally Controlled P.G.A.	12 Bits	16	Single Ended	33 kHz	± ½ LSB	1, 2, 4, 8

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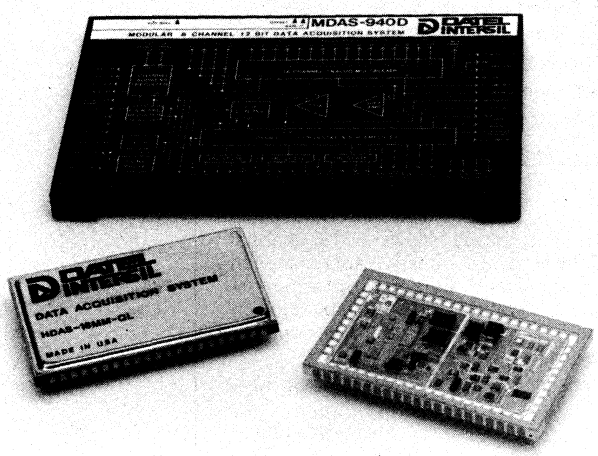
These compact, complete data-acquisition subsystems feature 8 or 16-channel multiplexed inputs, 8 or 12-bit resolution and three-state outputs. Most models include an internal sample-hold amplifier and programmable gain instrumentation amplifier. Two new models, the MDAS-940D and MDAS-940S include an internal, digitally-controlled, programmable gain instrumentation amplifier. Gain ranges of 1, 2, 4, and 8 are selected through the input of a two-bit word.

These high performance subsystems are ideal for applications ranging from microprocessor and mini-computer based data acquisition and process control to scientific instrumentation.



INPUT VOLTAGE RANGE	OUTPUT LOGIC	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
0 to −10V ±5V	3-state TTL	5.0 x 4.5 x 1.5 in (127 x 114 x 38 mm)	Module	0 to +70	—
0 to +5V	3-state TTL	40-pin DIP	Monolithic	−25 to +85	260
0 to +10 mV 0 to +10V ±10 mV to ±10V	3-state TTL	62-pin	Hybrid	0 to +70	266
				−25 to +85	
				−55 to +125	
0 to +10 mV 0 to +10V ±10 mV to ±10V	3-state TTL	62-pin	Hybrid	0 to +70	
				−25 to +85	
				−55 to +125	
0 to +5V 0 to +10V ±2.5V, ±5V, ±10V	3-state TTL	4.6 x 2.5 x 0.375 in (117 x 64 x 10 mm)	Module	0 to +70	274
0 to +5V 0 to +10V ±2.5V, ±5V, ±10V	3-state TTL	4.6 x 2.5 x 0.375 in (117 x 64 x 10 mm)	Module	0 to +70	
0 to +5V 0 to +10V ±5V, ±10V	3-state TTL	4.6 x 3.0 x 0.38 in (117 x 76 x 10 mm)	Module	0 to +70	280
0 to +5V 0 to +10V ±5V, ±10V	3-state TTL	4.6 x 3.0 x 0.38 in (117 x 76 x 10 mm)	Module	0 to +70	

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

16 Channel, 8 Bit Monolithic Data Acquisition System DAS-952R

FEATURES

- **16 Single Ended Channels**
- **8 Bits Resolution**
- **Monolithic CMOS Construction**
- **Three-State Outputs**
- **Ratiometric Operation**
- **Low Cost**

GENERAL DESCRIPTION

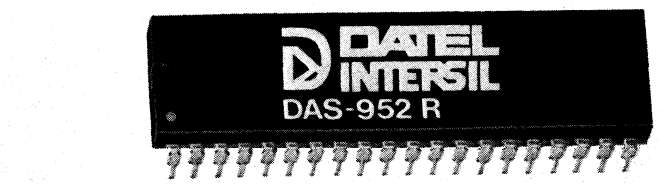
The DAS-952R is a single-chip, 16 channel, 8 bit data acquisition system. Monolithic CMOS technology allows a 16 channel multiplexer, 8 bit successive approximation A/D converter, and microprocessor-compatible control logic to be fabricated on a single chip and contained in a compact Dual-In-Line package.

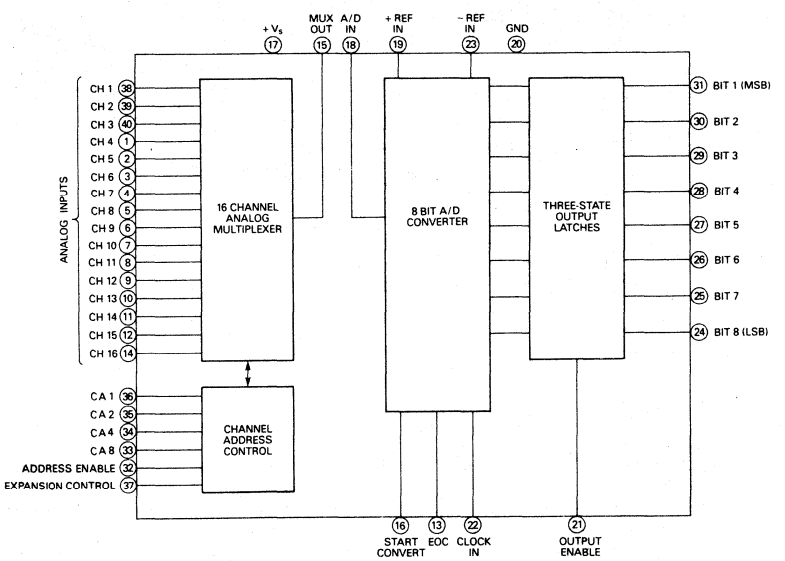
The design of this system emphasizes high accuracy, excellent repeatability, low power consumption, and a minimum of adjustments (no full scale or zero adjustment required). Latched and decoded address inputs and latched TTL three-state outputs allow easy interfacing to microprocessors.

The input multiplexer allows random access to any one of 16 single ended analog input channels and provides necessary logic for additional channel expansion. Connection of the multiplexer output to the converter input is by external pin connection, thus permitting easy signal conditioning such as amplification, linearization, or the use of a sample and hold.

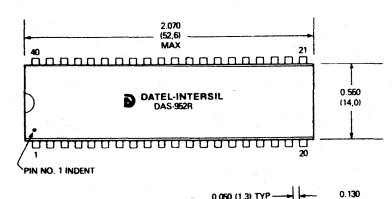
The 8 bit A/D converter uses a 256R ladder network, successive approximation register, and a chopper-stabilized comparator to implement the successive approximation conversion technique with a switching tree. Use of 256R ladder network ensures monotonicity while the chopper-stabilizer comparator makes the converter highly resistant to thermal effects and long term drift. In ratiometric conversion, the converter expresses the analog value being measured as a percentage of reference input. Full scale range may be selected within limits, to adjust the sensitivity of the converter to the desired application or to refer the output to a secondary standard.

Accuracy, speed, flexibility, excellent performance over a wide temperature range (−25°C to +85°C) and low cost make the DAS-952R an easy and practical answer to many data acquisition needs.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH. 4 IN	21	OUTPUT ENABLE
2	CH. 5 IN	22	CLOCK INPUT
3	CH. 6 IN	23	−REF. IN
4	CH. 7 IN	24	BIT 8 OUT (LSB)
5	CH. 8 IN	25	BIT 7 OUT
6	CH. 9 IN	26	BIT 6 OUT
7	CH. 10 IN	27	BIT 5 OUT
8	CH. 11 IN	28	BIT 4 OUT
9	CH. 12 IN	29	BIT 3 OUT
10	CH. 13 IN	30	BIT 2 OUT
11	CH. 14 IN	31	BIT 1 OUT (MSB)
12	CH. 15 IN	32	ADDRESS ENABLE
13	E.O.C.	33	CA 8 INPUT
14	CH. 16 IN	34	CA 4 INPUT
15	MULTIPLEXER OUTPUT	35	CA 2 INPUT
16	START CONVERT	36	CA 1 INPUT
17	+Vs	37	EXPANSION CONTROL
18	A/D IN	38	CH. 1 INPUT
19	+REF. IN	39	CH. 2 INPUT
20	GROUND	40	CH. 3 INPUT

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SPECIFICATIONS, DAS-952R

(Typical at 25° C, $+V_{SUPPLY} = +V_{REF}$, $-V_{REF} = G_{ND}$, clock = 640 KHz unless otherwise noted)

MAXIMUM RATINGS	
Voltage at Any Pin (Except Digital and REF inputs)	−0.3V to V_S +0.3V
Voltage at Digital Inputs	−0.3V to +15V
$+V_S$	+6.5V
+REF	V_S +0.1V
ANALOG INPUTS	
Number of Channels	16 Single Ended[1]
Input Voltage Range	0 to +5.25V max.
Channel ON-Resistance	1.5KΩ typ, 3KΩ max.[2]
Channel ON-Resistance, 85° C	6KΩ max.
Channel OFF Leakage Current, V_{IN} = +5V	10 nA typ., 200 nA max.
Channel OFF Leakage Current, V_{IN} = 0V	−10 nA typ., −200 nA min.
Channel Input Capacitance	5pF type., 7.5 pF max.
REF Input Resistance	1 KΩ min, 4.5 KΩ typ.[3]
REF Input Voltage	+0.512V to +5.25V[3]
A/D Converter Input Current[4]	±0.5 μA
DIGITAL INPUTS	
Logic HI ("1") Threshold, min,	V_S −1.5V
Logic LO ("0") Threshold, max	+1.5V
Input Current, Max. HI or LO	1.0 μA
Input Capacitance	7.5 pF max.
Clock Frequency	10KHz min., 1.2MHz max.
DIGITAL OUTPUTS	
Logic HI ("1") OUT, I_{OUT} = +360 μA	V_S −0.4V min.
Logic LO ("0") OUT, I_{OUT} = −1.6 mA	+0.45V max.
EOC Logic LO OUT, I_{OUT} = −1.2 mA	+0.45V max.
3-State Output Current, V_{OUT} = +5V	+3 μA max.
3-State Output Current V_{OUT} = 0V	−3 μA max.
3-State Output Capacitance	10 pF
Output Coding	Straight Binary, Positive True
CONVERTER PERFORMANCE	
Resoltuion	8 Bits
Linearity Error	±½ LSB, max.
Zero Error	±½ LSB, max.
Full Scale Error	±½ LSB, max.
Total Unadjusted Error	±½ LSB, max.[5]
Power Supply Rejection	±0.15%/V max.[6]
DYNAMIC PERFORMANCE	
Conversion Time	100 μsec typ., 116 μsec max.[7]
MUX Delay, from ADDRESS ENABLE	1 μsec typ., 2.5 μsec max.
3-State Turn-ON Delay	250 nsec max.
POWER REQUIREMENT	
Supply Voltage, rated performance	+5V ±.25V
Supply Voltage, operating range	+4.5V to +6V
Supply Current	300 μA typ., 3.0 mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	−25° C to +85° C
Storage Temperature Range	−65° C to +150° C
Package	40 Pin Plastic DIP

NOTES:

1. Logic is provided for expanding the number of channels externally.
2. Channel ON-resistances matched to within 75Ω maximum difference between any two channels.
3. Measured from +REF input to −REF input.
4. This is the comparator input current, a bias current into or out of the chopper stabilized comparator. It varies directly with clock frequency and is relatively independent of temperature.
5. Total unadjusted error is the sum of linearity, zero, and full-scale errors at any point on the transfer function.
6. V_S = +REF = +5V ±.25V
7. For clock frequency of 640 KHz. See technical note 4.

TECHNICAL NOTES

1. The DAS-952R is a ratiometric data acquisition system. The analog input voltage is expressed as a percentage of full scale voltage range. Full scale voltage range may be varied from +0.512V to +5.25V. The system uses an 8 bit converter with the full scale range divided into 256 steps (one step = 1 LSB). The ability to select the full scale range by means of the reference voltage allows selection of the size of the LSB, thereby allowing selection of the converter's sensitivity. The center of the full scale voltage range must be held within ±0.1V of the center of the supply range because the analog switch tree changes from N-channel switches to P-channel switches at this point. Failure to maintain the symmetry of these ranges may result in erratic switch operation. This condition is automatically satisfied in configurations where +REF = $+V_S$ and −REF = GND. For configurations where +REF $< +V_S$, −REF must be greater than GND by an equal amount. +REF can never exceed $+V_S$ and −REF can never be less than GND.
2. The system requires less than 1 mA of supply current. For applications where full scale range is selected between +4.75V and +5.25V, the reference can be used to generate the supply.
3. To preserve the accuracy of the system over its full operating temperature range, the reference source should have a temperature coefficient of 20 ppm/° C or less. For ambient temperature changes less than 75° C, a reference temperature coefficient of 30 ppm/° C is sufficient to maintain accuracy.
4. Conversion time and throughput rate for the DAS-952R is dependent on external clock frequency. The clock may be varied from 10 KHz to 1.2 MHz (see comparator input current graph).

ORDERING INFORMATION

MODEL	PRICE (1-24)
DAS-952R	

All external devices designated with Ⓓ in the Applications Diagrams are available from Datel/Intersil.

THIS DATA ACQUISITION SYSTEM IS COVERED BY GSA CONTRACT

DESCRIPTION OF OPERATION

Any one of 16 single-ended analog inputs may be selected by using the address decoder. The multiplexer input selection table shows the channel address input states required to select each channel. Channel address input states are latched into the address decoder on the low-to-high transition of the ADDRESS ENABLE input. Channel address inputs are required to be stable for 50 nsec. before and after the ADDRESS ENABLE low-to-high transition. Additional channel expansion is accomplished by disabling the internal multiplexer (all channels are off when EXPANSION CONTROL input is low) and connecting the additional signals directly to the converter input.

The converter input may also be used to introduce various signal conditioning devices into the analog signal path. The analog signal at the multiplexer input selected is available to the comparator after a maximum delay time of 2.5 usec. The converter's successive approximation register is reset on the positive going edge of 200 nsec. start conversion pulse, and conversion is initiated on the falling edge of the pulse.

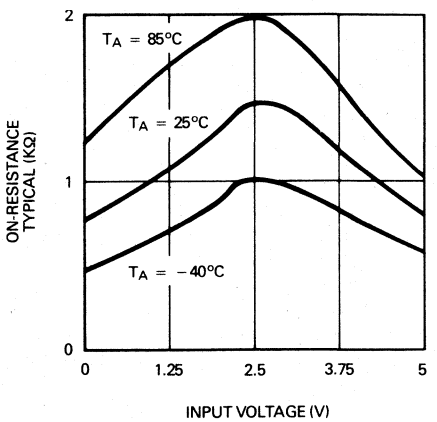
A conversion in progress may be interrupted by a new start conversion pulse. The EOC output goes LO in 1 to 8 clock periods after the rising edge of the start conversion pulse. For continuous conversions the EOC output can be tied to the start conversion input and an initial external start conversion pulse applied after power up.

The 8 bit A/D converter requires 64 clock periods to resolve the analog signal voltage level. The converter employs a chopper stabilized comparator for extreme resistance to input offset drift errors. The 256R ladder network ensures monotonicity and does not cause load variations on the reference voltage. The values of the top and bottom resistors are different from the rest of the ladder so that the first output transition occurs when the analog voltage level reaches +½ LSB and each succeeding output transition occurs at intervals of 1 LSB up to full scale.

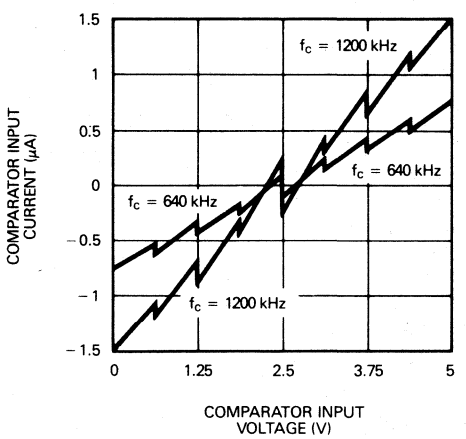
The 8 bit, straight binary, positive true result appears at the three-state output latches, which are enabled when the OUTPUT ENABLE control is HI.

TYPICAL PERFORMANCE

MULTIPLEXER ON RESISTANCE



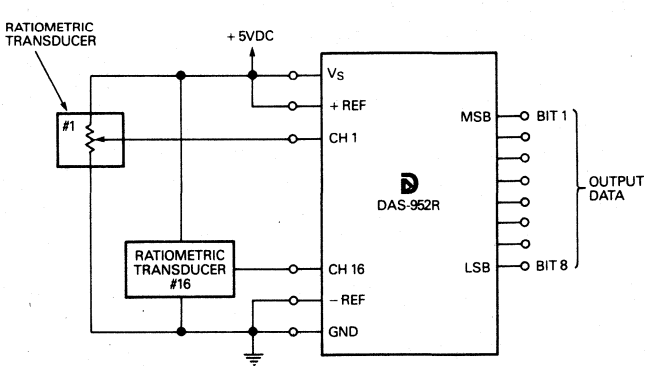
COMPARATOR INPUT CURRENT



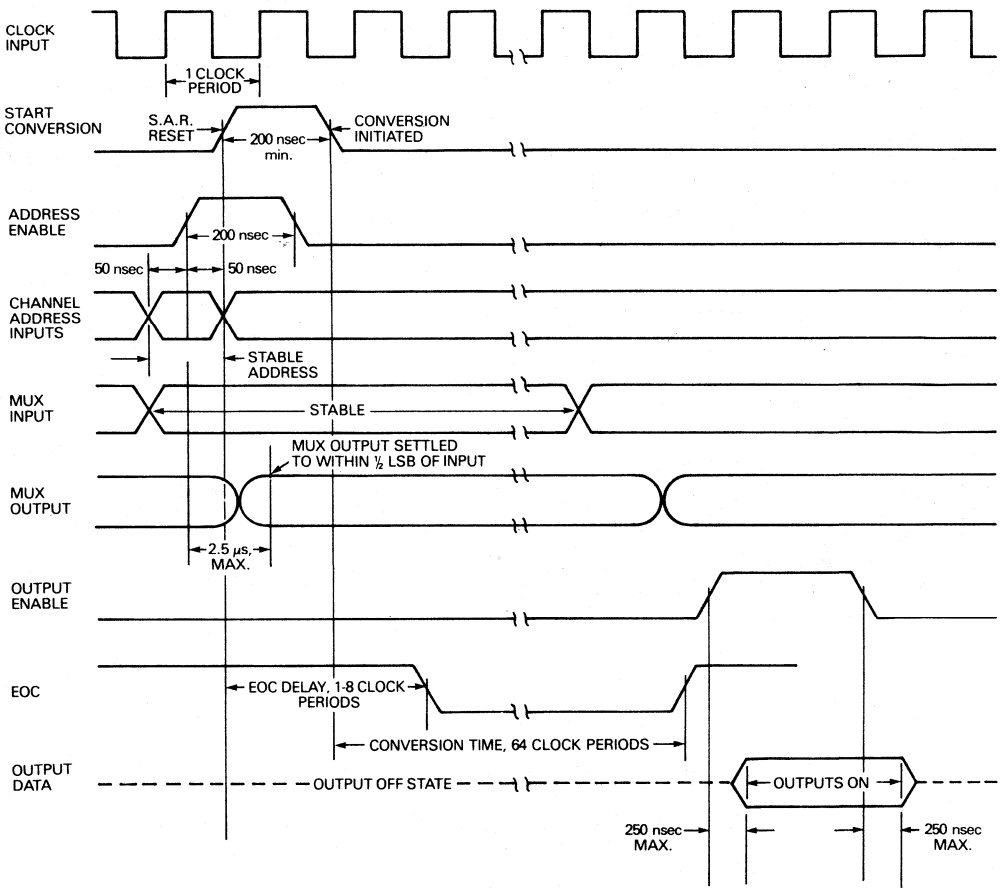
CHANNEL ADDRESS TABLE

CHANNEL ADDRESS INPUT 8	4	2	1	INHIBIT CONTROL	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

RATIOMETRIC CONVERSION SYSTEM

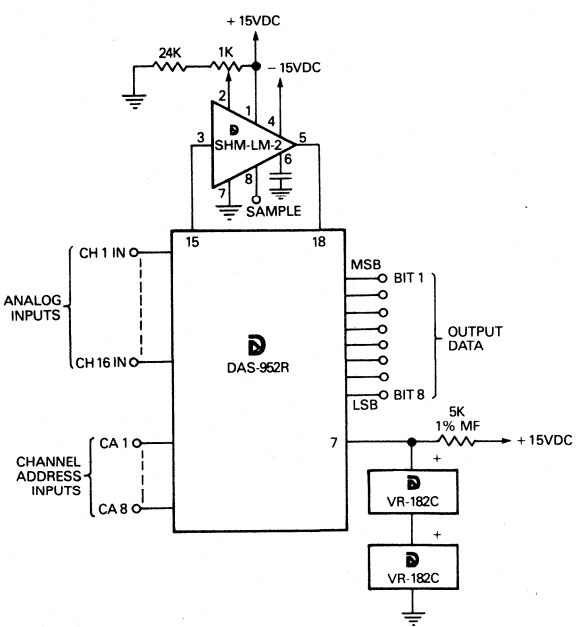


TIMING DIAGRAM



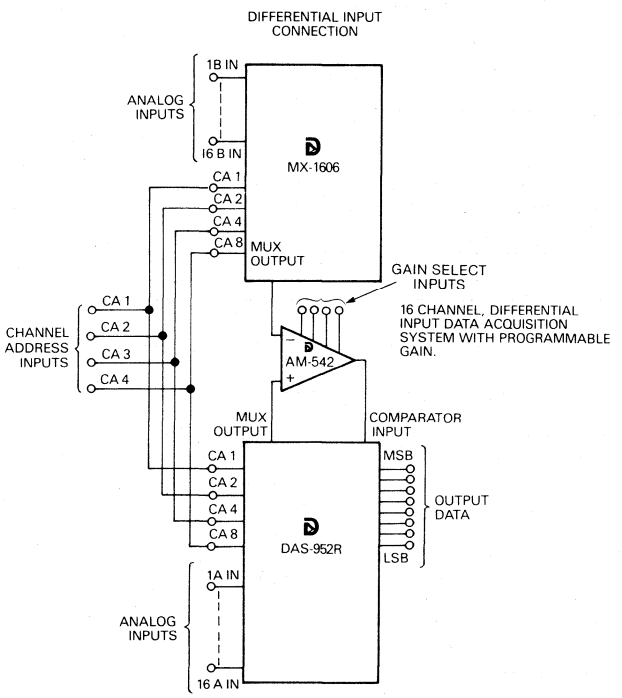
DATA ACQUISITION SYSTEM WITH SAMPLE-HOLD

For applications where a sample-hold is required, connections are made as shown in the accompanying diagram. The sample-hold may be put in the sample mode after the multiplexer output settles (see timing diagram). The start conversion input can be taken high as shown in the timing diagram but should not be taken low until the sample-hold has acquired the input voltage. The acquisition time of the sample-hold is dependent on the value of the hold capacitance. This value must be selected for the acquisition time and hold-mode voltage droop required by the converter speed and accuracy, respectively. Optimal values of hold capacitance may be selected after throughput rate is determined. See SHM-LM-2 data sheet.

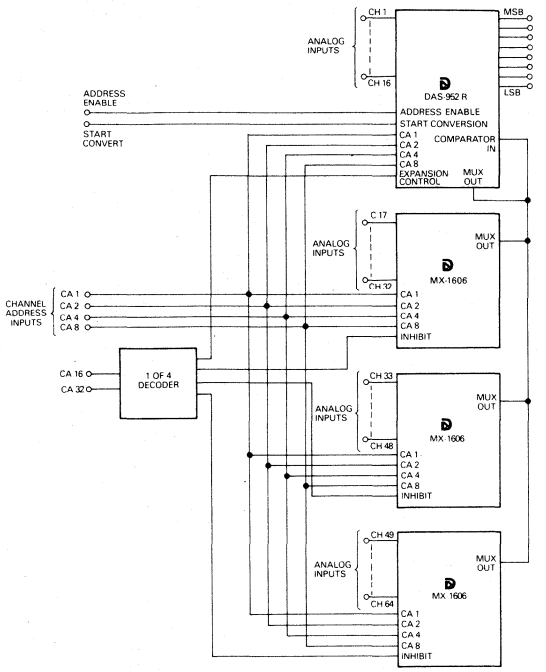


APPLICATIONS

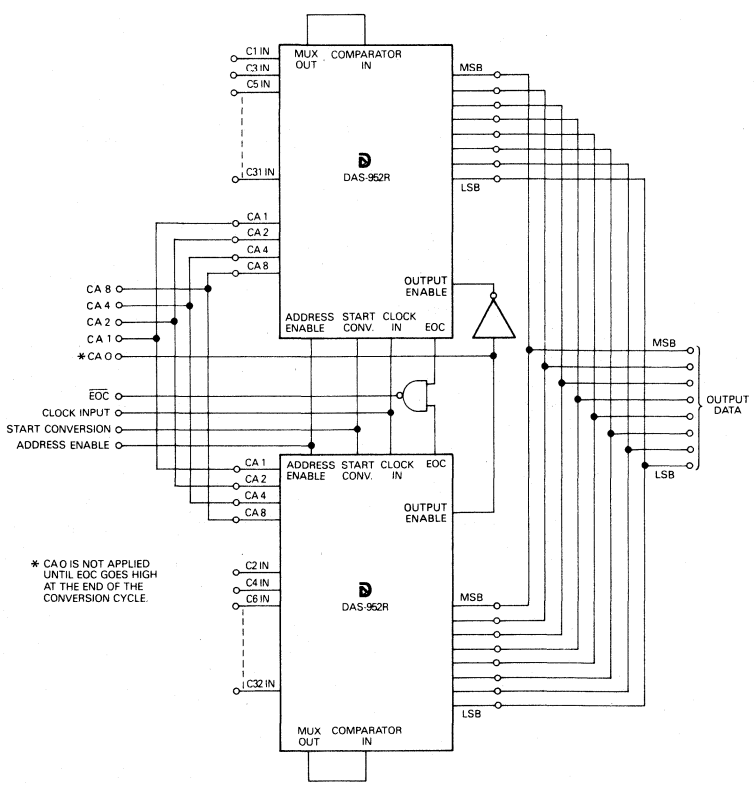
DIFFERENTIAL INPUT CONNECTION



EXPANSION TO 64 CHANNELS

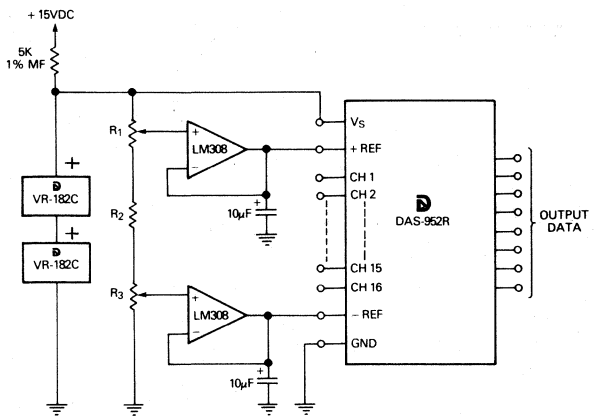


32 CHANNEL, 35KHz DATA ACQUISITION SYSTEM



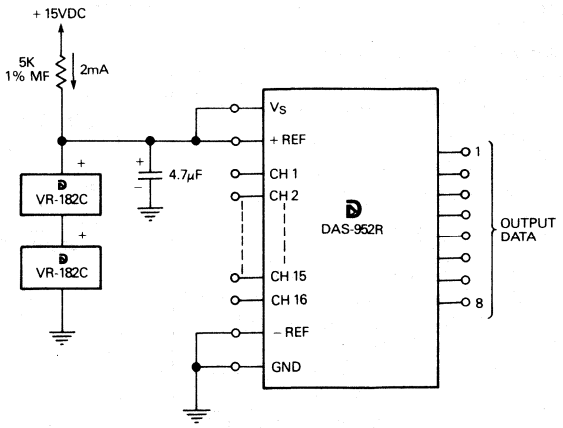
REFERENCE AND SUPPLY CIRCUITS

DUAL ADJUSTABLE REFERENCE

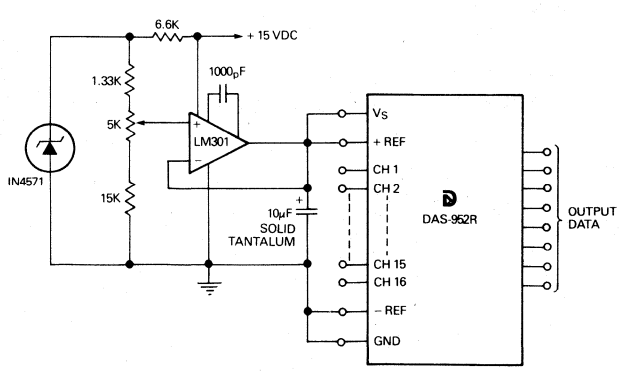


NOTE: VALUES OF R_1, R_2 and R_3 ARE SELECTED TO YIELD THE DESIRED FULL SCALE CONVERSION RANGE. SEE TECHNICAL NOTE 1.

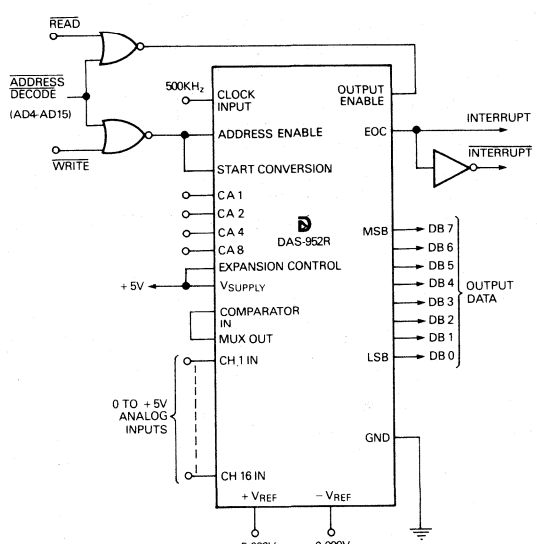
30 PPM/° C REFERENCE AND SUPPLY



ADJUSTABLE REFERENCE AND SUPPLY



TYPICAL MICROPROCESSOR INTERFACE



12 Bit Microelectronic Data Acquisition System HDAS-16, HDAS-8

FEATURES

- **Miniature 62 Pin Package**
- **12 Bit Resolution**
- **10mV to 10V Full Scale Range**
- **Three-State Outputs**
- **16 Channels Single Ended or 8 Channels Differential**

GENERAL DESCRIPTION

Utilizing hybrid technology, Datel-Intersil offers a data acquisition system with superior performance and reliability, combined with low cost.

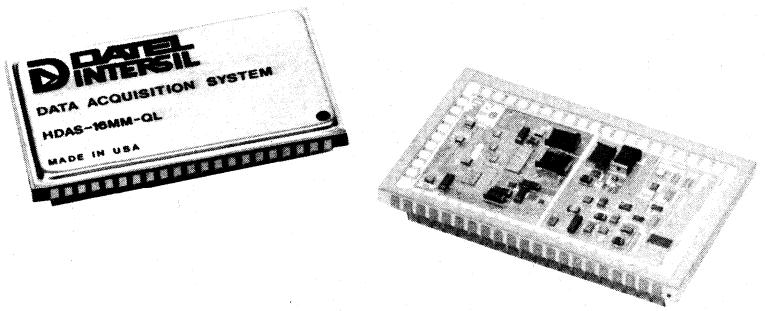
The HDAS-8 with 8 differential input channels and HDAS-16 with 16 single ended input channels are complete high performance 12 bit data acquisition systems in a 62 pin package. Acquisition and conversion time combined is 20μsec. max., giving a minimum throughput rate of 50 kHz. The twelve bit binary data can be transferred out in three four bit bytes, by means of the three-state data bus drivers. Output coding is straight binary in unipolar operation and offset binary in bipolar operation.

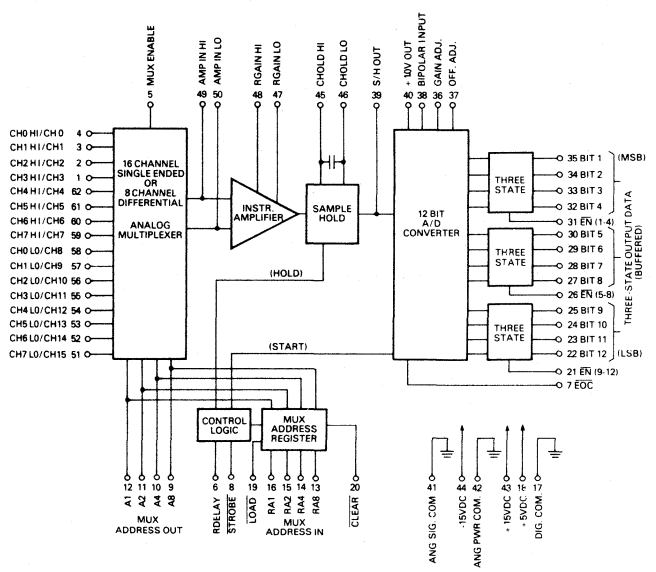
The HDAS circuit includes a multiplexer, programmable gain instrumentation amplifier, sample and hold circuit complete with MOS hold capacitor, 10 volt buffered reference, a twelve bit A/D converter with three-state outputs and digital logic.

The internal instrumentation amplifier is programmed with a single resistor for gains of 1 to 1000. This key feature is useful in low level signal applications involving bridge amplifiers, transducers, strain gauge and thermocouple interface.

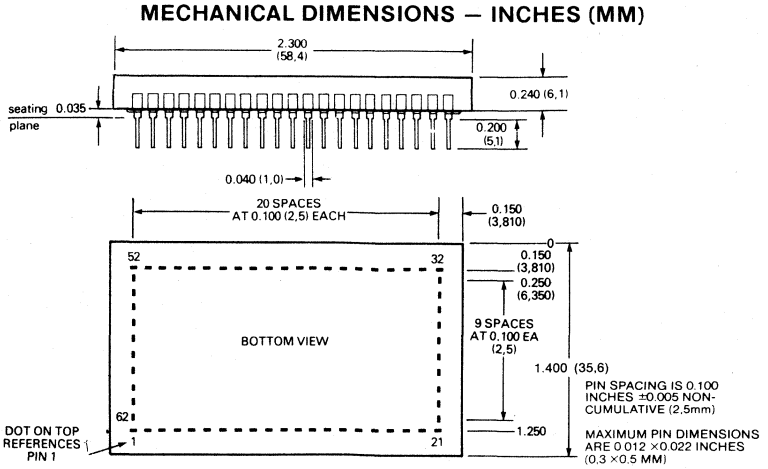
The HDAS is cased in a small hermetic 62 pin package. Models are available in three different temperature ranges: 0 to +70, −25 to +85, and −55 to +125 degrees centigrade.

High reliability versions of each model are also available. Power requirements are ±15VDC and +5VDC.





MECHANICAL DIMENSIONS — INCHES (MM)



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SPECIFICATIONS, HDAS-16 & HDAS-8 (Typical at 25°C, ±15V and +5V supplies unless otherwise indicated)

MAXIMUM RATINGS

+5V Supply	−0.5V to +7.0V
+15V Supply	−0.5V to +18.0V
−15V Supply	+0.5 to −18.0V
Analog Input Channels[1]	±35V
Digital Input Pins	−0.5V to +7.0V

ANALOG INPUTS

Number of Channels	16 Single Ended (HDAS-16) 8 Differential (HDAS-8)
Voltage Ranges[2]**, unipolar**	0 to +10mV to 0 to +10V
bipolar	±10mV to ±10V
Input Gain Equation	$G=1+\frac{20K}{RG}$
Common Mode Range	±11V min.
Input Resistance	100 megohms
Gain Equation Error[7]	0.1% max.
Input Bias Current	200pA max.
Bias Current Tempco	Doubles every 10°C
Input Offset Current	50pA max.
Offset Current Tempco	Doubles every 10°C
Input Offset Voltage	8mV typ., 27 mV max.
Offset Voltage Tempco	20μV/°C + (10μV/°C×G)
Voltage Noise (RMS)	
G=1	150μV RTI[3]
G=1000	1.62μV RTI[3]
Input Capacitance, OFF channel	10pF
ON channel	100pF (HDAS-16) 50pF (HDAS-8)

ACCURACY

Resolution	12 Bits
System Error[5]	±0.025% of FSR[4] max. (±1 LSB)
Gain Error	Adj. to zero
Offset Error	Adj. to zero
Temp. Coeff. of Gain	±10ppm/°C typ., ±30ppm/°C max.
Temp. Coeff. of Offset	±7ppm/°C of FSR max.
Diff. Linearity Tempco	±3ppm/°C of FSR max.
CMRR(Gain=1)	82 db @ 10 KHz
CMRR(Gain=1000)	110 db @ 60 Hz
Monotonicity	Guaranteed over operating temp range
Power Supply Rejection	.01%/%
+10V Ref (Pin 40)	±0.1%[8]

DYNAMIC CHARACTERISTICS

Throughput Rate	50 kHz min.
Acquisition Time	9μsec. typ. 10μsec. max.
Conversion Time	9μsec. typ. 10μsec. max.
Aperture Delay Time	100nsec.
Sample-Hold Droop	1 μV/μsec.
Feedthrough (1 KHz)	.01% max.
Channel Crosstalk (MUX)	−80 dB at 1 kHz

DIGITAL OUTPUTS[6]

Parallel Data Out	12 parallel lines of buffered three-state output data. Drives 5 TTL loads.
Coding	Straight binary, Offset binary
Mux Address Out	Buffered output of address register. Drives 5 TTL loads.
$\overline{\text{EOC}}$ (Status)	Drives 5 TTL loads.

DIGITAL INPUTS[7]

$\overline{\text{Enable}}$	Three separate inputs which enable three-state outputs in 4 bit bytes. 1 LS TTL load.
Mux Address In	3 Bit (HDAS-8) or 4 bit (HDAS-16) binary address 1 LS TTL load.
$\overline{\text{Strobe}}$	1 LS TTL load Pulse Width: 40 nsec. ≤ t_W ≤ EOC
MuxEnable	1 LS TTL load
$\overline{\text{Load}}$	1 LS TTL load
$\overline{\text{Clear}}$	1 LS TTL load
POWER REQUIREMENT	+15VDC ±0.5V @ 67 mA max. −15VDC ±0.5V @ 71 mA max. +5VDC ±0.25V @ 155 mA max.

PHYSICAL ENVIRONMENTAL

Operating Temperature Range	0°C to +70°C (MC) −25°C to +85°C (MR) −55°C to +125°C (MM)
Storage Temperature Range	−65°C to +150°C
Package Size, max.	2.33 × 1.42 × .3 inches (36,07 × 59,18 × 8,89 mm)
Package Type	62 pin, hermetically sealed
Pins	Kovar
Weight	1.4 oz. (40 g)

NOTES:

1. ±20V in power off condition
2. Selectable with proper gain range
3. RTI - Referred to Input
4. FSR - Full Scale Range 10V for 0 to +10V input, 5V for ±2.5V input.
5. The internal A/D converter is specified at ± ½ LSB max. for nonlinearity and ± ½ LSB max. for diff. linearity. These errors are contained within the system error.
6. All outputs are LSTTL (low power Schottky)
   Vout ("O") ≤0.4V Vout ("1")≥2.7V
7. All inputs are LSTTL
   Vin ("O")<0.8V Vin ("1")≥2.0V

ORDERING INFORMATION

MODEL	OP. TEMP. RANGE	PRICE (1-9)
HDAS-16MC	0°C to 70°C	
HDAS-16MR	−25°C to +85°C	
HDAS-16MM	−55°C to +125°C	
HDAS-8MC	0°C to 70°C	
HDAS-8MR	−25°C to +85°C	
HDAS-8MM	−55°C to +125°C	

Receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-4 (component lead spring socket) 62 required.
Evaluation socket, Datel P/N 58-6322-1 Includes PC board with offset and gain potentiometers, bifurcated terminals for electrical connections.
Trimming Potentiometer: TP20K (20 K ohms)
For high reliability versions of the HDAS, contact factory.
THESE MODELS ARE COVERED BY GSA CONTRACT

PIN CONNECTIONS

PIN NO.	HDAS-16	HDAS-8
1	CH3 IN	CH3 HI IN
2	CH2 IN	CH2 HI IN
3	CH1 IN	CH1 HI IN
4	CH0 IN	CH0 HI IN
5	MUX ENABLE	*
6	R DELAY	*
7	E.O.C.	*
8	STROBE	*
9	A8 ┐ MUX	*
10	A4 ├ ADDRESS	*
11	A2 ├ OUT	*
12	A1 ┘	*
13	RA8 ┐ MUX	*
14	RA4 ├ ADDRESS	*
15	RA2 ├ IN	*
16	RA1 ┘	*
17	DIGITAL COM.	*
18	+5VDC	*
19	LOAD ENABLE	*
20	CLEAR ENABLE	*
21	ENABLE (Bits 9-12)	*
22	BIT 12 OUT (LSB)	*
23	BIT 11 OUT	*
24	BIT 10 OUT	*
25	BIT 9 OUT	*
26	ENABLE (Bits 5-8)	*
27	BIT 8 OUT	*
28	BIT 7 OUT	*
29	BIT 6 OUT	*
30	BIT 5 OUT	*
31	ENABLE (Bits 1-4)	*
32	BIT 4 OUT	*
33	BIT 3 OUT	*
34	BIT 2 OUT	*
35	BIT 1 OUT (MSB)	*
36	GAIN ADJ.	*
37	OFFSET ADJ.	*
38	BIPOLAR INPUT	*
39	SAMPLE/HOLD OUT	*
40	+10V OUT	*
41	ANALOG SIGNAL COM	*
42	ANALOG POWER COM.	*
43	+15 VDC	*
44	−15 VDC	*
45	C HOLD HI	*
46	C HOLD LO	*
47	R GAIN LO	*
48	R GAIN HI	*
49	AMP. IN HI	*
50	AMP. IN LO	*
51	CH15 IN	CH7 LO IN
52	CH14 IN	CH6 LO IN
53	CH13 IN	CH5 LO IN
54	CH12 IN	CH4 LO IN
55	CH11 IN	CH3 LO IN
56	CH10 IN	CH2 LO IN
57	CH9 IN	CH1 LO IN
58	CH8 IN	CH0 LO IN
59	CH7 IN	CH7 HI IN
60	CH6 IN	CH6 HI IN
61	CH5 IN	CH5 HI IN
62	CH4 IN	CH4 HI IN

*Same as HDAS-16

TABLE 1 DESCRIPTION OF PIN FUNCTIONS

FUNCTION	LOGIC STATE	DESCRIPTION
DIGITAL INPUTS		
STROBE	"1" to "0"	Initiates acquisition and conversion of analog signal
LOAD	"0"	Random Address Mode Initiated on falling edge of STROBE
	"1"	Sequential Address Mode
CLEAR	"0"	Allows next STROBE pulse to reset MUX ADDRESS to CH0 overriding LOAD command.
MUX ENABLE	"0"	Disables internal MUX
	"1"	Enables internal MUX
MUX ADDRESS IN		Selects channel for Random Address Mode 8,4,2,1 natural binary coding
DIGITAL OUTPUTS		
E.O.C.		End of Conversion (STATUS)
	"0"	Conversion complete
	"1"	Conversion in process
ENABLE (1-4)	"0"	Enables three-state outputs Bits 1-4
	"1"	Disables three-state outputs Bits 1-4
ENABLE (5-8)	"0"	Enables three-state outputs Bits 5-8
	"1"	Disables three-state outputs Bits 5-8
ENABLE (9-12)	"0"	Enables three-state outputs Bits 9-12
	"1"	Disables three-state outputs Bits 9-12
MUX ADDRESS OUT		Output of MUX Address Register 8,4,2,1 natural binary coding
ANALOG INPUTS		
Channel Inputs		Limit voltage to ±20 V beyond power supplies. Ex.-if power supplies ON (±15V), maximum input voltage is ±35 V. If power supplies OFF (0 V), maximum input voltage is ±20 V.
Bipolar Input		For unipolar operation, connect to PIN 39 (S/H OUT) For bipolar operation, connect to PIN 40 (+10 V OUT)
ANALOG OUTPUTS		
S/H OUT		Sample Hold Output
+10 V OUT		Buffered +10 V reference output
ADJUSTMENT PINS		
ANG SIG COM		Low level analog signal return.
GAIN ADJ		External gain adjustment, see calibration instructions.
OFFSET ADJ		External offset adjustment, see calibration instructions.
R GAIN		Optional gain selection point. Factory adjusted for G=1 when left open.
C HOLD		Optional hold capacitor connection.
R DELAY		Optional acquisition time adjustment when connected to +5V factory adjusted for 9 μS.

TECHNICAL NOTES

1. Input channels are protected to 20 V beyond power supplies. All digital output pins have one second short circuit protection and CHOLD has a ten second short circuit protection.
2. To increase acquisition time allotment, (time for the multiplexer, instrumentation amplifier and sample-hold to settle out) connect a resistor from RDELAY (Pin 6) to +5 V (Pin 18). Refer to Table 2 for delay times and resistor values.
3. An external hold capacitor can be connected between CHOLD HI and CHOLD LO. The addition of this capacitor will improve the sample-hold droop rate especially at high operating temperature ranges. It is recommended that polypropylene or teflon capacitors be used for best results.
4. The HDAS has a self starting circuit for free running sequential operation. If, however, in a power up condition the supply voltage slew rate is less than .3V/usec., the free running state may not be initialized. By applying a negative pulse to the STROBE, this condition will be eliminated.
5. All digital inputs must be stable 50nsec before and 50nsec after high to low transition of STROBE.
6. For UNIPOLAR operation connect BIPOLAR IN (Pin 38) to S/H out (Pin 39). For BIPOLAR operation connect BIPOLAR IN (Pin 38) to +10V OUT (Pin 40).
7. If HDAS reference (+10V OUT) is used for external circuitry, source current should be limited to 1mA.

TABLE 2 INPUT RANGE PARAMETERS (Typical)

INPUT RANGE	GAIN	RGAIN (Ω)	AMPLIFIER SETTLING TIME	RDELAY (Ω)	THROUGHPUT	SYSTEM ACCURACY
±10V	1	NONE	9μsec.	NONE	55.5 KHz	0.009%
±5V	2	20.0K	9μsec.	NONE	55.5 KHz	0.009%
±2.5V	4	6.667K	9μsec.	NONE	55.5 KHz	0.009%
±1V	10	2.222K	9μsec.	NONE	55.5 KHz	0.009%
±200mV	50	408.2	16μsec.	7K	40.0 KHz	0.010%
±100mV	100	202.0	30μsec.	21K	25.6 KHz	0.011%
±50mV	200	100.5	60μsec.	51K	14.5 KHz	0.016%
±20mV	500	40.08	144μsec.	135K	6.5 KHz	0.035%
±10mV	1000	20.02	288μsec.	279K*	3.3 KHz	0.069%

*This value exceeds the maximum recommended for use over military temperature ranges.

NOTES:

$$RGAIN\ (\Omega) = \frac{20{,}000}{(GAIN-1)} \qquad RDELAY\ (\Omega) = \frac{\text{Amp Setting time}}{10^{-9}} - 9K$$

1. Throughput time = Amplifier Setting time and A/D Conversion Time
   A/D Conversion time = 9 μsec
2. Full Scale can be accommodated for analog signal ranges of ±10mV to ±10V.
3. The analog input range to the A/D Converter is 0 to +10.0V for unipolar and −10.0V to +10.0V for bipolar operation.

TABLE 3 CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

CALIBRATION PROCEDURES

A) Offset and gain adjustments may be made by connecting two 20K trim potentiometers as shown in Figure 1.

B) Connect a precision voltage source to pin 4 (CH0). If the HDAS-8 is used, connect pin 58 (CH.0 LO) to analog ground. Ground pin 20 ($\overline{CLEAR}$) and momentarily short pin 8 ($\overline{STROBE}$). Trigger the A/D by connecting pin 7 ($\overline{EOC}$) to pin 8 ($\overline{STROBE}$). Select proper value for RGAIN and RDELAY by referring to Table 2.

C) Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (ZERO + ½ LSB) or the bipolar offset adjustment (−FS + ½ LSB). Adjust the offset trim potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

D) Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½LSB). Adjust the gain trim potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

FIG 1 EXTERNAL ADJ.

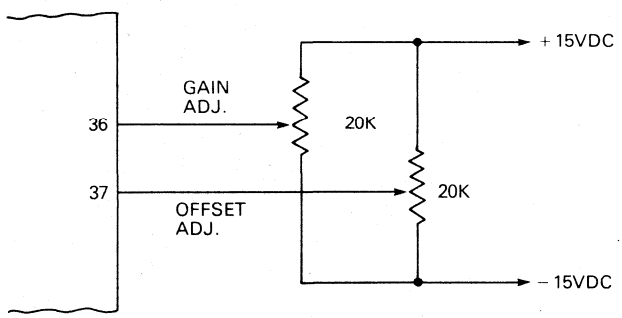


TABLE 4 OUTPUT CODING

	UNIPOLAR		STRAIGHT BINARY
	0 to +10 V	0 to +5V	
+FS-1 LSB	+9.9976	+4.9988	1111 1111 1111
+½FS	+5.0000	+2.5000	1000 0000 0000
+1 LSB	+0.0024	+0.0012	0000 0000 0001
ZERO	0.0000	0.0000	0000 0000 0000

	BIPOLAR		OFFSET BINARY*
	±10 V	±5V	
+FS-1 LSB	+9.9951	+4.9976	1111 1111 1111
+½FS	+5.0000	+2.5000	1100 0000 0000
+1 LSB	+0.0049	+0.0024	1000 0000 0001
ZERO	0.0000	0.0000	1000 0000 0000
−FS+1 LSB	−9.9951	−4.9976	0000 0000 0001
−FS	−10.000	−5.0000	0000 0000 0000

*For 2's complement - add inverter to MSB line.

TABLE 5 MUX CHANNEL ADDRESSING

← MUX ADDRESS → PIN 9 RA8	10 RA4	11 RA2	12 RA1	5 MUX ENAB.	ON CHANNEL	
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	HDAS-8 (3 BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	HDAS-16 (4 BIT ADDRESS)
1	1	1	1	1	15	

MULTIPLEXER ADDRESSING

Channel Selection

The HDAS is capable of two modes of addressing the multiplexer.

RANDOM ADDRESS

Set Pin 19 ($\overline{LOAD}$) to logic "0". The next falling edge of $\overline{STROBE}$ will load the MUX CHANNEL ADDRESS present on Pin 13 to Pin 16. Address inputs must be stable 50 nsec before and after falling edge of $\overline{STROBE}$ pulse.

FREE RUNNING SEQUENTIAL ADDRESS

Set Pin 19 ($\overline{LOAD}$) and Pin 20 ($\overline{CLEAR}$) to logic "1" or leave open. Connect Pin 7 ($\overline{EOC}$) to Pin 8 ($\overline{STROBE}$). The falling edge of $\overline{EOC}$ will increment channel address. This means that when the $\overline{EOC}$ is low, the digital output data is valid for the previous channel (CHn - 1) than that channel indicated on MUX ADDRESS OUTPUT. The HDAS will continually scan all 16 channels.

example

CH 4 has been addressed and a conversion takes place. The $\overline{EOC}$ goes low and that Channels data becomes valid but MUX ADDRESS CODE is now CH5.

TRIGGERED SEQUENTIAL ADDRESS

Set Pin 19 ($\overline{LOAD}$) and Pin 20 ($\overline{CLEAR}$) to logic "1" or leave open. Apply a falling edge trigger pulse to Pin 8 ($\overline{STROBE}$). This negative transition causes the contents of the address counter to be incremented by one followed by an A/D conversion in 9 μsec.

FIG. 2 HDAS TIMING DIAGRAM

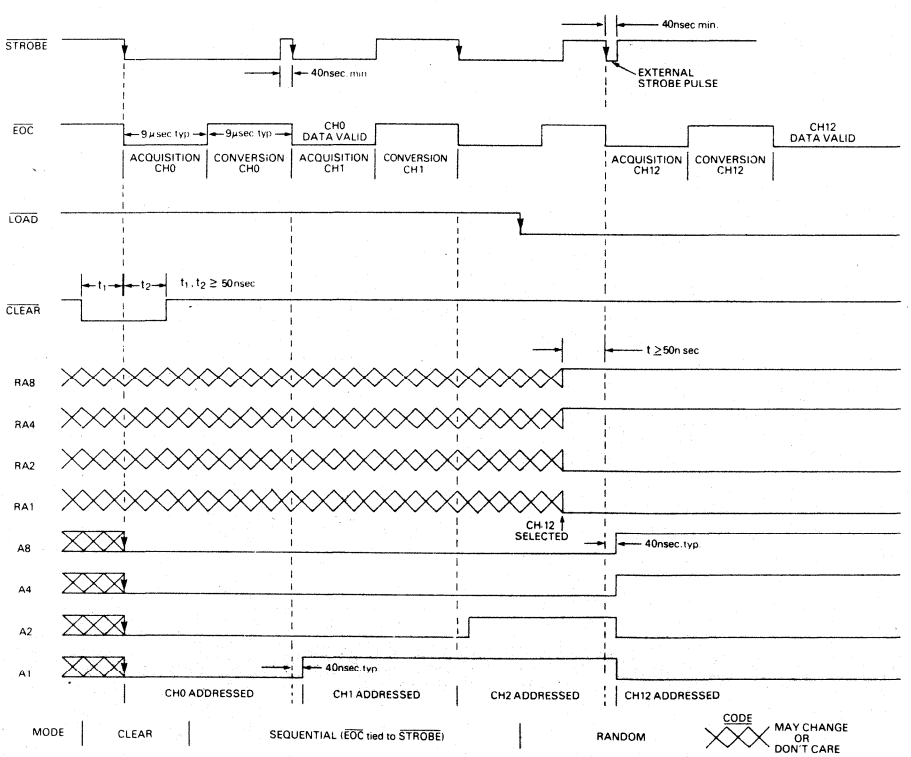
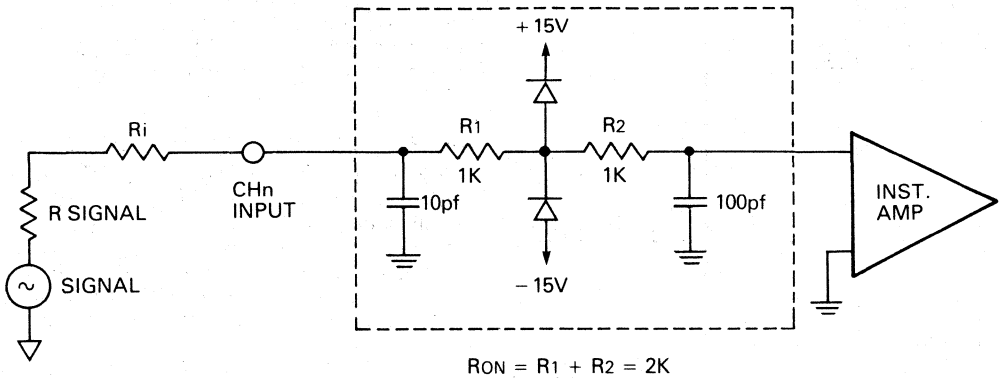


FIG. 3 MULTIPLEXER EQUIVALENT CIRCUIT



INPUT VOLTAGE PROTECTION

As shown in Fig. 3, the multiplexer has reversed biased diodes which protect the input channels from being damaged by overvoltage signals. The HDAS input channels are protected up to 20 V beyond the supplies and can be increased by adding series resistors (Ri) to each channel. This input resistor must limit the current flowing through the protection diodes to 10 mA.

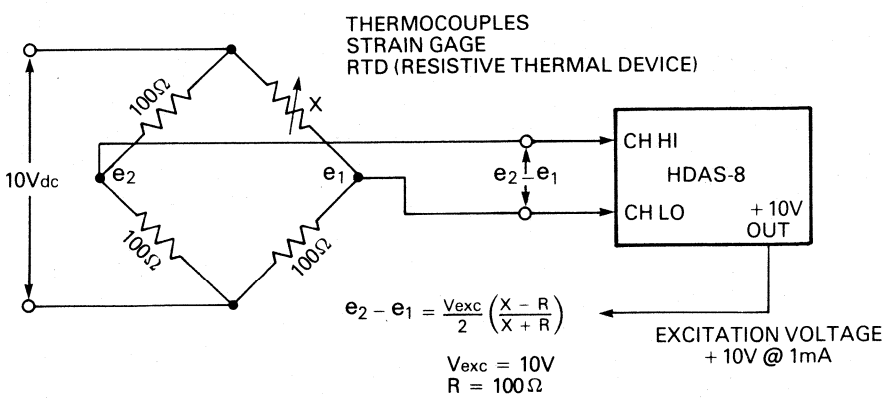
The value of Ri for a specific voltage protection range (Vp) can be calculated by the following formula:

$$Vp = (R\ signal + Ri + Ron)\ (10\ mA)$$

where Ron = 2K

NOTE: Increased input series resistance will increase multiplexer settling time.

FIG. 4 LOW LEVEL INPUTS



Remote monitoring of low level signals can be difficult, especially when analog signals pass through an environment with high levels of electrical noise. One solution is to use an instrumentation amplifier to extract the common mode voltage and amplify the voltage difference. The HDAS-8, an eight channel differential input system, can reject common-mode noise and allow amplification up to a gain of 1000. Direct connections to thermocouples, transducers, strain gages and RTD can be made through shielded twisted pairs. A differential RC filter may be used to attenuate normal mode noise.

FIG. 5 32 CHANNEL SINGLE ENDED DATA ACQUISITION SYSTEM

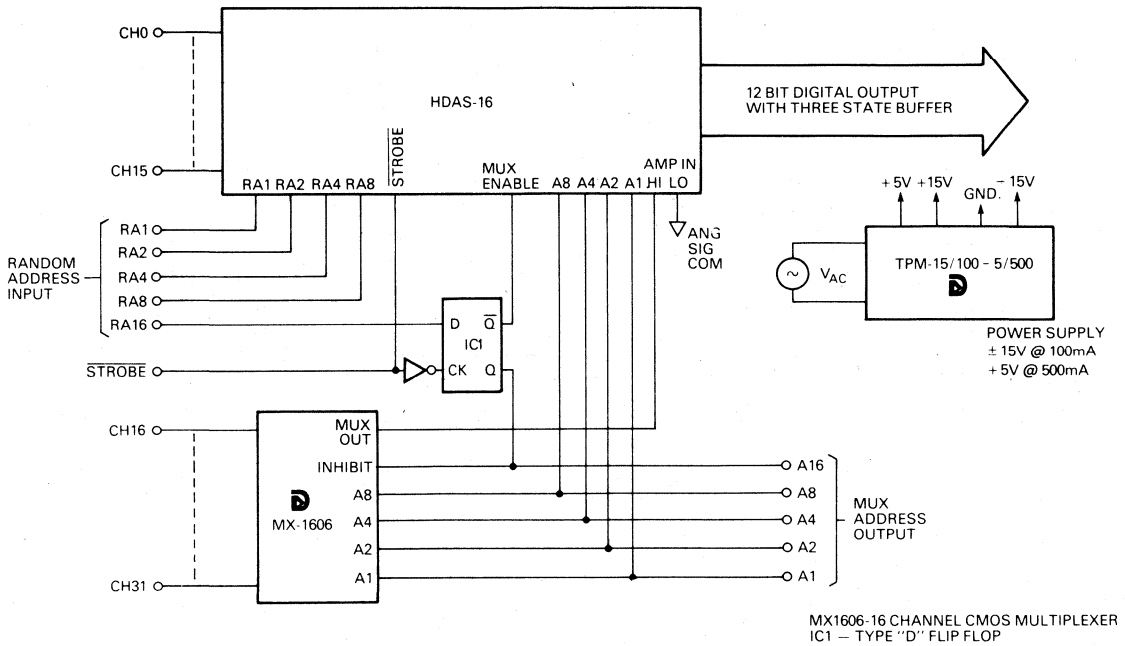
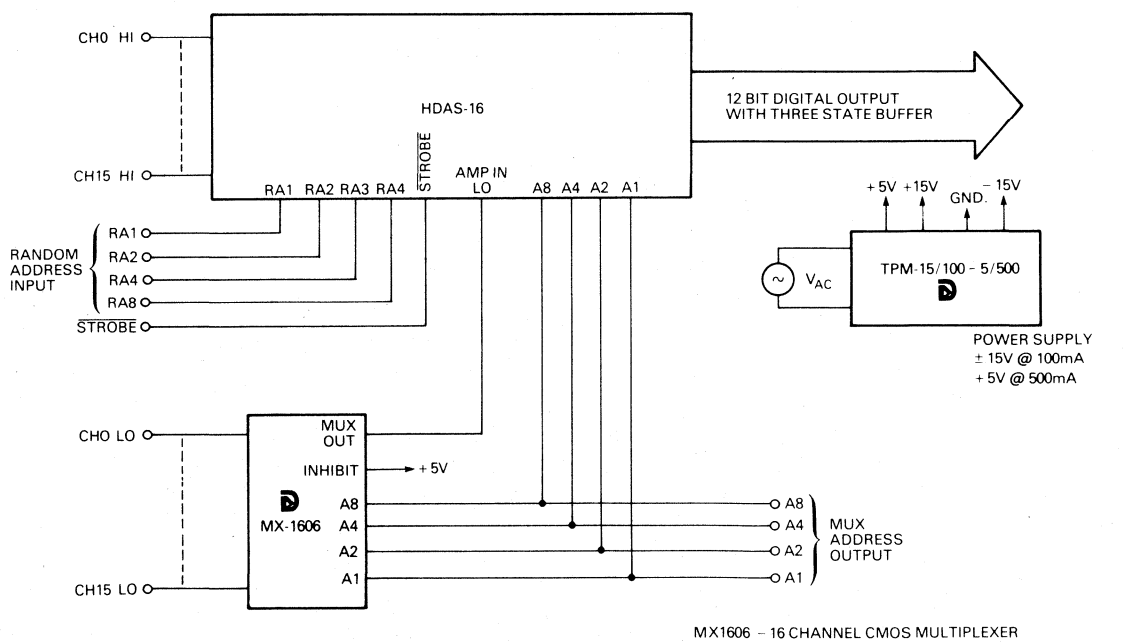


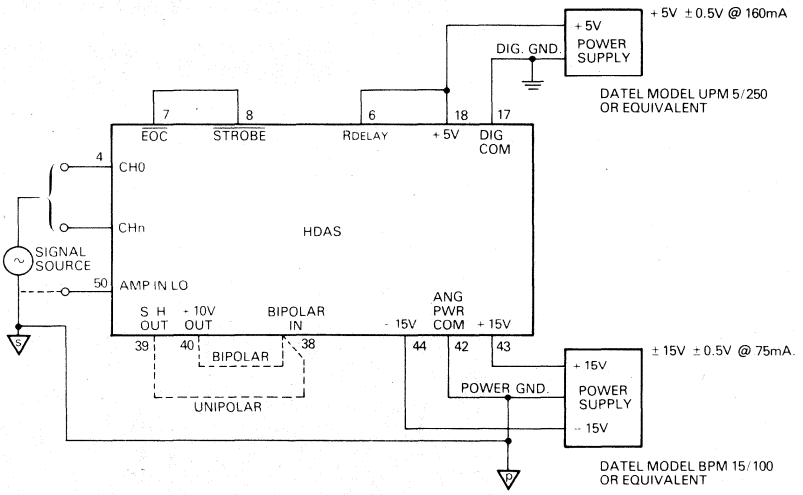
FIG. 6 16 CHANNEL DIFFERENTIAL DATA ACQUISITION SYSTEM



MULTIPLEXER EXPANSION

Fig. 5 shows the interconnection scheme for expanding the multiplexer channel capacity of the HDAS-16 from 16 channels single ended to 32 channels. Fig. 6 shows a similar scheme to expand the HDAS-16 to 16 differential channels. When extending channel capacity, the multiplexer settling time must be extended through the use of R delay (Pin 6). See technical note Z and Table 2 for connection and value selection.

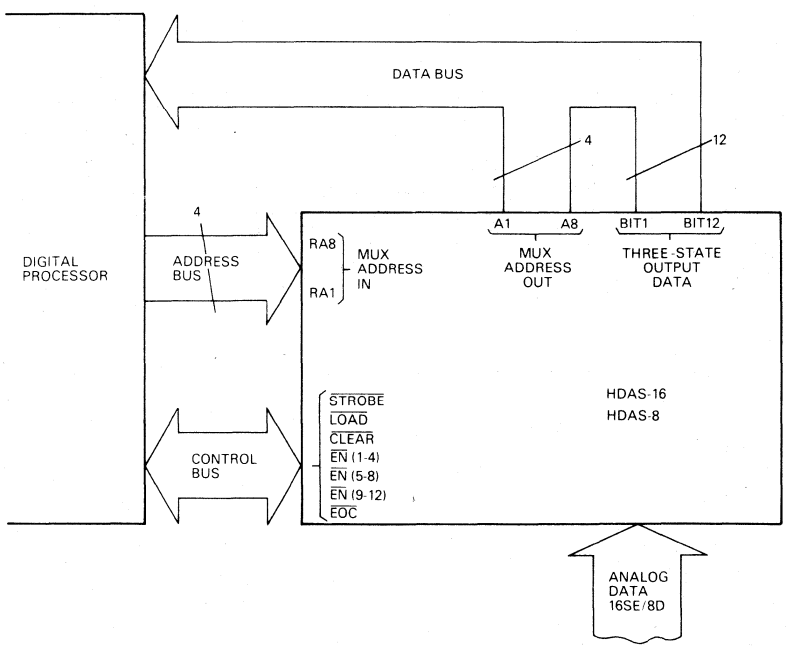
FIG. 7 SIMPLE CONNECTION DIAGRAM



NOTES:

1. For HDAS-16, tie PIN 50 to "signal source common" if possible. Otherwise tie PIN 50 to PIN 41 (ANG SIG COM)
2. BIPOLAR connection yields +10V range. UNIPOLAR connection yields 0 to ±10 V range. Other ranges are created by selecting appropriate value of Rg.
3. DIG COM, ANG PWR COM and ANG SIG COM are internally connected.

FIG. 8 PROCESSOR INTERFACE



Miniature Modular Data Acquisition System MDAS-16, MDAS-8D

FEATURES

- **16 Channels Single Ended or 8 Channels Differential**
- **12 Bits Resolution**
- **50 kHz Throughput Rate**
- **Three-State Outputs**
- **Low Cost**
- **Miniature Size**

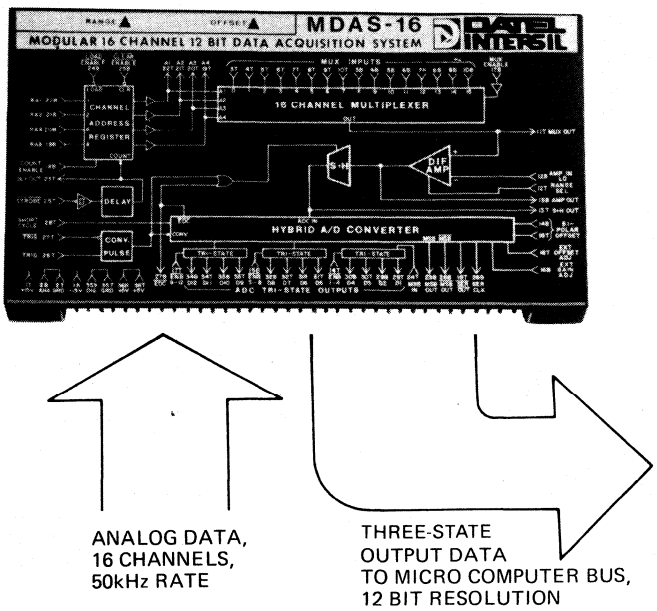
DESCRIPTION

The MDAS-16 and MDAS-8D data acquisition modules are complete, self-contained systems featuring 16 channel single ended or 8 channel differential operation respectively. Resolution is 12 bits and throughput rate is 50kHz. Output data is buffered three-state for interfacing to mini or micro-computer data buses. Output data can be transferred in three 4 bit bytes. Output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation.

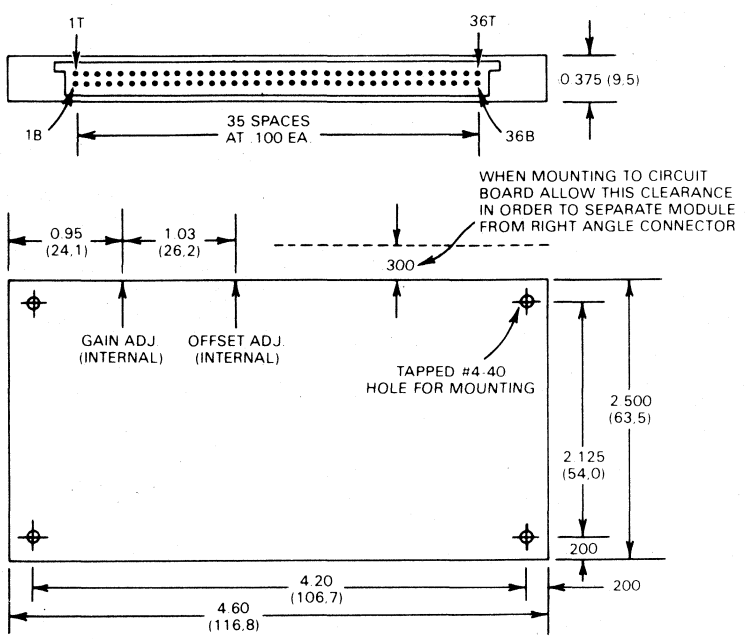
The 4.6 x 2.5 x 0.375 inch size of these modules is ½ inch narrower than other competitive models. The small size and low cost are made possible by extensive use of hybrid and monolithic circuits to reduce parts count and increase reliability. Both models use Datel-Intersil's new ADC-HZ12BGC 12 bit hybrid A/D converter along with a monolithic sample-hold and analog multiplexer.

The MDAS-16 and MDAS-8D feature a high degree of user flexibility with pin-programmable input ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. The systems may be operated in either random or sequential channel addressing modes. For applications where lower than 12 bit resolution can be used, the A/D converter can be short-cycled to achieve a faster conversion rate. Output data is also available in serial form with a gated clock output.

The modules are housed in a shielded steel case. Input-output connections are made by means of a 72-pin connector. The number of channels may be expanded by 32 for the MDAS-16 or by 16 for the MDAS-8D by use of the multiplexer expander modules MDXP-32, and MDXP-32-1.



MECHANICAL DIMENSIONS - INCHES (MM)



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, MDAS-16 & MDAS-8D
(Typical at 25°C, ±15V and +5V supplies unless otherwise indicated)

ANALOG INPUTS

Number of Channels	16 Single Ended (MDAS-16) 8 Differential (MDAS-8D)
Input Voltage Ranges	
unipolar	0 to +5V 0 to +10V
bipolar	±2.5V, ±5V, ±10V
Common Mode Range, min.	±10V
Max. Input Voltage, no damage	±15V
Input Impedance	100 megohms
Input Bias Current	3nA, 10nA max. 0 to 70°C
Input Capacitance	
OFF channel	10 pF
ON channel	100pF

ACCURACY

Resolution	12 Bits
Error, max. 50kHz sampling	±.025% of FSR
Nonlinearity, max.	±½ LSB
Diff. Nonlinearity, max.	±½ LSB
Gain Error	Adj. to zero
Offset Error	Adj. to zero
Temp. Coeff. of Gain, max.	±30ppm/°C
Temp. Coeff. of Offset, max.	±7ppm/°C of FS
Diff. Linearity Tempco, max.	±3ppm/°C of FS
Common Mode Rejec., min.	70 dB at 1 kHz
Monotonicity	0°C to 70°C
Power Supply Rejection	.01%/% Supply

DYNAMIC CHARACTERISTICS

Throughput Rate, max.	50 kHz
Acquisition Time	6 μsec.
Conversion Time	14 μsec.
Aperture Time, max.	100 nsec.
Sample-Hold Droop, max.	200 μV/msec.
Feedthrough, max.	.01%
Channel Crosstalk (Mux.)	-80 dB at 1 kHz

DIGITAL OUTPUTS

Parallel Data Out	12 parallel lines of buffered three-state output data. Drives 12 TTL loads
Coding	Straight binary, offset binary, and two's complement
Serial Out	Output data in MSB first, NRZ format. Straight binary and offset binary coding. Drives 5 TTL loads
Mux Address Out	Buffered output of address register Drives 20 TTL loads
Delay Out	Drives 5 TTL loads
Clock Out	Drives 5 TTL loads
$\overline{\text{EOC}}$ (Status)	Drives 4 TTL loads
MSB Out	Drives 5 TTL loads
$\overline{\text{MSB}}$ Out	Drives 5 TTL loads

DIGITAL INPUTS

$\overline{\text{Enable}}$	Three separate inputs which enable three-state outputs in 4 bit bytes. 1 TTL load
Mux Address In	3 bit (MDAS-8D) or 4 bit (MDAS-16) binary address 1 LS TTL load
$\overline{\text{Strobe}}$	1 LS TTL load with 10K pull-up resistor
A/D Trigger	1 LS TTL load with 10K pull-up resistor
A/D $\overline{\text{Trigger}}$	1 LS TTL Load
Mux Enable	1 TTL load with 10K pull-up resistor
Count Enable	1 LS TTL load with 10K pull-up resistor
$\overline{\text{Load Enable}}$	1 LS TTL load with 10K pull-up resistor
$\overline{\text{Clear Enable}}$	1 LS TTL load with 10K pull-up resistor
MSB In	1 TTL load
Short Cycle	1 TTL load with 10K pull-up resistor

POWER REQUIREMENT

+15VDC ±0.5V @ 65mA
-15VDC ±0.5V @ 60 mA
+5VDC ±0.25V @ 200mA

PHYSICAL ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temperature Range	-25°C to +85°C
Package Size	4.6 x 2.5 x 0.375 inches (116,8 x 63,5 x 9,5 mm)
Package Type	Steel, shielded on 5 sides
Weight	6 oz. (170 g)

NOTES: 1. All outputs are Vout ("O") ≤+0.4V, Vout ("1") ≥+2.4V
2. All inputs are Vin ("0") ≤+0.8V, Vin ("1") ≥+2.0V

ORDERING INFORMATION

MDAS-16 .....
MDAS-8D .....

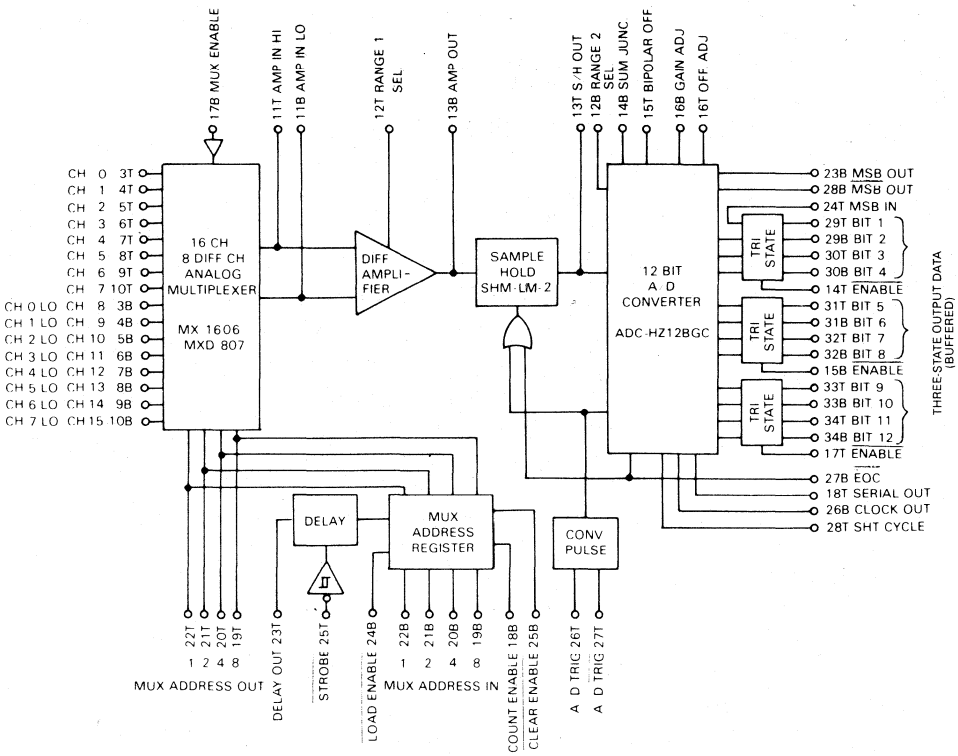
These modules are also available in extended temperature range versions designated with the suffix EX (-25°C to +85°C) or EXX-HS (-55°C to 85°C) with hermetically sealed semiconductor components. Contact factory for price and delivery.

Included with each module is a mating right-angle 72 pin connector. (AMP 3-86063-2). Additional connectors may also be ordered by the following number: 58-2083010 Connector

Trimming Potentiometers:

Multiplexer expander modules are also available. The MDXP-32 adds 32 single ended or 16 differential channels with control logic.
The MDXP-32-1 is identical but without control logic.

BLOCK DIAGRAM MDAS-16, MDAS-8D



PIN CONNECTIONS for MDAS-16

	Top	Bottom	
+15VDC	1T	1B	-15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 8 In
Ch. 1 In	4T	4B	Ch. 9 In
Ch. 2 In	5T	5B	Ch. 10 In
Ch. 3 In	6T	6B	Ch. 11 In
Ch. 4 In	7T	7B	Ch. 12 In
Ch. 5 In	8T	8B	Ch. 13 In
Ch. 6 In	9T	9B	Ch. 14 In
Ch. 7 In	10T	10B	Ch. 15 In
Amplifier In Hi	11T	11B	Amplifier In Lo
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1-4 Out)	14T	14B	Sum. Junc. (Bipolar Off.)
Bipolar Offset	15T	15B	Enable (Bits 5-8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9-12)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out } Mux	19T	19B	8 In } Mux
4 Out } Address	20T	20B	4 In } Address
2 Out } Lines	21T	21B	2 In } Lines
1 Out }	22T	22B	1 In }
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC

*Three-State Outputs

PIN CONNECTIONS for MDAS-8D

	Top	Bottom	
+15VDC	1T	1B	-15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 Hi In	3T	3B	Ch. 0 Lo In
Ch. 1 Hi In	4T	4B	Ch. 1 Lo In
Ch. 2 Hi In	5T	5B	Ch. 2 Lo In
Ch. 3 Hi In	6T	6B	Ch. 3 Lo In
Ch. 4 Hi In	7T	7B	Ch. 4 Lo In
Ch. 5 Hi In	8T	8B	Ch. 5 Lo In
Ch. 6 Hi In	9T	9B	Ch. 6 Lo In
Ch. 7 Hi In	10T	10B	Ch. 7 Lo In
Amplifier In Hi	11T	11B	Amplifier In Lo
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1-4 Out)	14T	14B	Sum. Junc. (Bipolar Off!)
Bipolar Offset	15T	15B	Enable (Bits 5-8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9-12 Out)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out } Mux	19T	19B	8 In } Mux
4 Out } Address	20T	20B	4 In } Address
2 Out } Lines	21T	21B	2 In } Lines
1 Out }	22T	22B	1In }
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC

*Three-State Outputs

TABLE I DESCRIPTION OF CONTROL PIN FUNCTIONS

FUNCTION	PIN	DESCRIPTION
Amplifier In Lo	11B	Analog monitoring point for MDAS-8D. For the MDAS-16 this pin must be grounded.
Amplifier In Hi	11T	Analog monitoring point.
Range 2 Select Range 1 Select	12B 12T	These pins program analog input voltage range. See Table II
Amplifier Out	13B	Analog monitoring point.
Sample Hold Out	13T	Analog monitoring point.
Summing Junction	14B	Used to program analog input voltage range and bipolar offset. See Table II
$\overline{\text{Enable}}$	14T	Input LO enables tri-state outputs for bits 1-4. Input HI inhibits outputs.
$\overline{\text{Enable}}$	15B	Input LO enables tri-state outputs for bits 5-8. Input HI inhibits outputs.
Bipolar Offset	15T	Connects to 14B for bipolar operation and to analog ground for unipolar operation. See Table II
Ext. Gain Adjust	16B	Used to adjust out gain error. Operates independently of the internal adjustment. See External Adjustments diagram.
Ext. Offset Adjust	16T	Used to adjust out offset error. Operates independently of the internal adjustment. See External Adjustments diagram.
Mux Enable	17B	Input HI enables analog multiplexer. Input LO inhibits analog multiplexer.
$\overline{\text{Enable}}$	17T	Input LO enables three-state outputs for bits 9-12. Input HI inhibits outputs.
Count Enable	18B	Input HI enables Mux Address Register. Input LO inhibits Mux address Register.
Mux Address In	19B, 20B, 21B, 22B	Digital inputs for channel address selection in random addressing mode. Straight binary coding. See Table III
Mux Address Out	19T, 20T, 21T, 22T	Straight binary coded output of Mux Address Register.
MSB Out	23B	Bit 1 TTL output of A/D converter. Connect to pin 24T for straight binary or offset binary output coding.
Delay Output	23T	An output delay pulse for 6μsec. to allow for multiplexer and amplifier settling time and sample hold acquisition time. This pin is normally connected to A/D $\overline{\text{Trigger}}$ (pin 27T) to initiate A/D conversion.
$\overline{\text{Load Enable}}$	24B	Input HI for sequential addressing. Input LO for random addressing.
MSB In	24T	Bit 1 input to three-state output buffers. Connect to either pin 23B (MSB Out) or pin 28B ($\overline{\text{MSB}}$ Out).
$\overline{\text{Clear Enable}}$	25B	Input LO and a negative transition on pin 25T resets Mux address counter to zero.
$\overline{\text{Strobe}}$	25T	Negative input transition initiates channel scanning sequence in sequential mode or a conversion in the random mode. A Schmidt trigger input adds hysteresis for good noise rejection.
Clock Output	26B	A/D converter clock pulses for synchronization of serial data. Negative going pulses of approximately 100 nsec. duration.
A/D Trigger	26T	A positive logic transition on this input initiates A/D conversion.
$\overline{\text{EOC}}$ (status)	27B	End of conversion (status) output. Output HI during conversion and LO when conversion is complete.
A/D $\overline{\text{Trigger}}$	27T	A negative logic transition on this input initiates A/D conversion. This pin is normally connected to pin 23T (Delay Output).
$\overline{\text{MSB}}$ Out	28B	Complemented bit 1 TTL output of A/D converter. Connect to pin 24T for two's complement output coding.
Short Cycle	28T	For 12 bit resolution connect this pin to ground. To short cycle A/D converter for lower resolution, connect this pin to output bit n + 1 for a resolution of n bits. Short cycling of the A/D converter can only be done with the $\overline{\text{Enable}}$ inputs (pins 14T, 15B and 17T) LO.

TABLE II INPUT RANGE SELECTION

INPUT RANGE	CONNECT THESE PINS TOGETHER		
	RANGE 1 PIN 12T	RANGE 2 PIN 12B	BIPOLAR OFF. PIN 15T
0 TO +5V	13B	13T	2B OR 2T
0 TO +10V	2B OR 2T	13T	2B OR 2T
±2.5V	13B	13T	14B
± 5V	2B OR 2T	13T	14B
±10V	2B OR 2T	OPEN	14B

TABLE IV
THROUGHPUT RATES VS. NO. BITS FOR SHORT-CYCLED A/D CONVERTER

NO. BITS	THROUGHPUT RATE
12	50 kHz
10	53 kHz
8	57 kHz
4	67 kHz

TABLE III MUX CHANNEL ADDRESSING

← MUX ADDRESS → PIN 19B (8)	20B (4)	21B (2)	22B (1)	17B MUX ENAB.	ON CHANNEL	
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	MDAS-8D (3 BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	MDAS-16 (4 BIT ADDRESS)
1	1	1	1	1	15	

TABLE V
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	-2.4994V +2.4982V
±5V	OFFSET GAIN	-4.9988V +4.9963V
±10V	OFFSET GAIN	-9.9976V +9.9927V

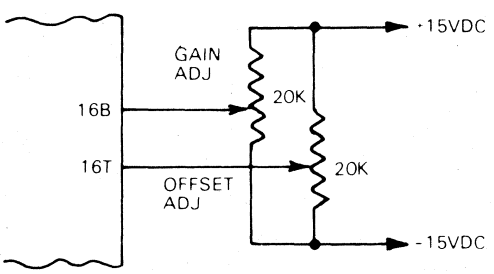


FIG. 1 EXTERNAL ADJUSTMENTS

SET-UP AND CALIBRATION INSTRUCTIONS

1. Select input voltage range desired and connect pins 12B, 12T, and 15T in accordance with Table II. If the MDAS-16 is used, ground pin 11B. Ground all analog channel inputs which are not to be used. Leave pin 17B open.
2. Determine resolution to be used. For full 12 bits, ground pin 28T. For lower resolution requirements, connect pin 28T to bit output n + 1 for n bit resolution. For example: for 8 bit resolution connect pin 28T to pin 33T (Bit 9 Out). To operate the A/D converter in this short cycled mode, the $\overline{\text{Enable}}$ inputs (pins 14T, 15B, and 17T) must be connected to ground thereby enabling the three-state outputs. For 12 bit resolution the three-state outputs can be either enabled or disabled.
3. Select the output coding desired. For straight binary (unipolar) or offset binary (bipolar) connect pin 23B (MSB Out) to pin 24T (MSB In). For two's complement (bipolar) connect pin 28B ($\overline{\text{MSB}}$ Out) to pin 24T.
4. Select desired multiplexer mode. Connect pin 23T (Delay Out) to pin 27T (A/D $\overline{\text{Trigger}}$).

A. **Free Running Sequential Addressing**

Connect pin 27B ($\overline{\text{EOC}}$) to pin 25T ($\overline{\text{Strobe}}$). Leave pins 24B ($\overline{\text{Load Enable}}$) and 25B ($\overline{\text{Clear Enable}}$) open. Sequencing is initiated by a positive logic transition applied to pin 26T (A/D Trigger). Pin 26T must remain HI during free running sequential addressing. Sequencing is stopped by a LO applied to pin 26T.

B. **Triggered Sequential Addressing**

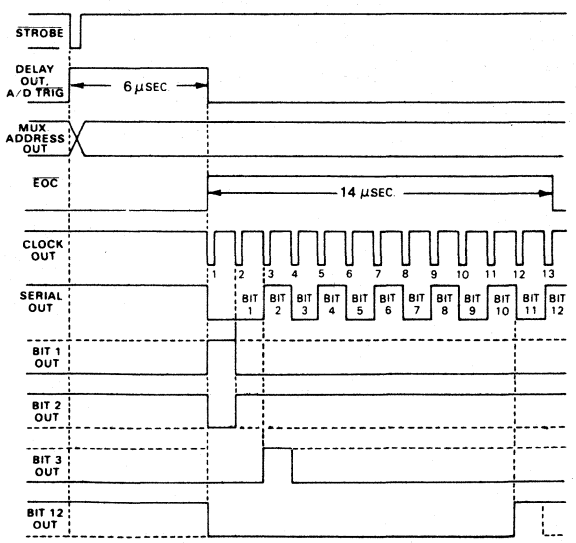
Leave pins 24B ($\overline{\text{Load Enable}}$) and 25B ($\overline{\text{Clear Enable}}$) open. Apply a falling edge trigger to pin 25T ($\overline{\text{Strobe}}$). The negative transition of the strobe will cause the contents of the address counter to be incremented by one.

C. **Random Addressing**

Ground pin 24B ($\overline{\text{Load Enable}}$). Leave pin 25B ($\overline{\text{Clear Enable}}$) open. Each negative transition applied to pin 25T ($\overline{\text{Strobe}}$) will cause the data at pins 19B, 20B, 21B and 22B (Mux Address In) to be loaded into the Address Register. Address inputs must be stable for at least 300 nsec. after negative transition of $\overline{\text{Strobe}}$.

5. Calibration Procedure
   A. Offset and gain adjustments may be made either internally or externally. Self-contained trimming potentiometers are provided for the internal adjustments. For external adjustment, 20K trimming potentiometers must be used with pins 16B and 16T. Connect as shown in Figure 1.
   B. Connect power supplies to the module and a precision voltage source to pin 3T (Chan 0 In). If the MDAS-8D is used, connect pin 3B (Chan 0 LO) to analog ground. Ground pin 25B ($\overline{\text{Clear Enable}}$) and momentarily short pin 25T ($\overline{\text{Strobe}}$) to ground. Use an oscilloscope to monitor the serial output code at pin 18T. Trigger the A/D converter with 50kHz positive going pulses applied to pin 26T (A/D Trigger).
   C. Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + ½ LSB) or the bipolar offset adjustment (-FS + ½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
   D. Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS - 1½ LSB). Adjust the gain trimming potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

MDAS-16, MDAS-8D TIMING DIAGRAM Output Code: 010101010101



NEW

DATEL

12-Bit Programmable Gain Data Acquisition Subsystem MDAS-940

FEATURES

- **16 Channels Single Ended or 8 Channels Differential**
- **12 Bit Resolution**
- **2 Bit Gain Programming**
- **33 kHz Throughput Rate**
- **Resistor-Programmed Low Level Inputs**
- **Three-State Bussable Outputs**

GENERAL DESCRIPTION

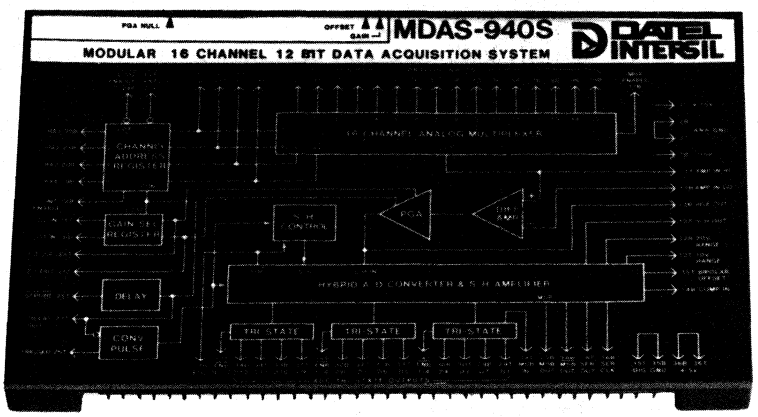
Datel-Intersil's MDAS-940S and MDAS-940D are complete, self-contained data acquisition subsystems featuring 16 channel single-ended or 8 channel differential A/D inputs respectively. Resolution is 12 binary bits with accuracy of ±0.025% at a throughput rate of 33 kHz. Both models contain a Programmable Gain Amplifier with digitally selectable gain ranges of 1, 2, 4 and 8. Gain selection is accomplished through the input of a 2 bit word.

Output data is buffered three-state with 3 separate enable lines brought out for easy interfacing to 4-, 8-, or 16-bit data busses. Data is also available in serial form with a gated clock output. Output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation.

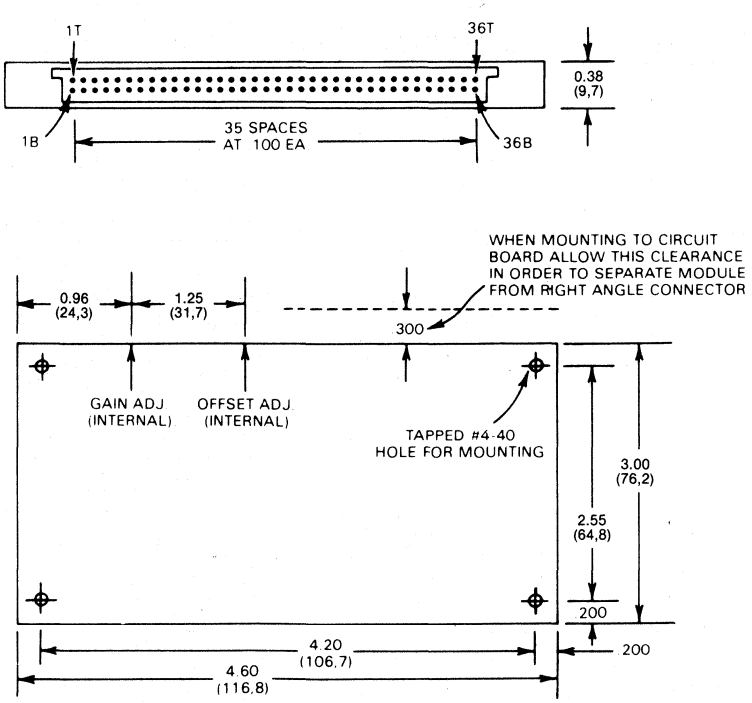
These modules also feature pin-programmable input ranges of 0 to +5V, 0 to +10V, ±5V, and ±10V, which allows for analog measurements with an effective full scale range of 0.625V when the PGA is selected for a gain of 8. Thus, inputs from strain gages, and other low level signal sensors may be accepted without external signal conditioning. The systems may be operated in either random or sequential channel addressing modes.

The extensive use of hybrid and monolithic circuits reduces the parts count, increases reliability, and makes possible the small size and low cost of these modules. Both models use Datel-Intersil's ADC-HS12BGC hybrid A/D converter with internal sample-hold along with a monolithic analog multiplexer.

The modules are housed in a 4.6 × 3.0 × 0.38 inch shielded steel case. Input-output connections are made by means of a 72-pin connector. The number of input channels may be expanded by 32 for the MDAS-940S or by 16 for the MDAS-940D by using Datel-Intersil's multiplexer expander modules MDXP-32 and MDXP-32-1.



MECHANICAL DIMENSIONS - INCHES (MM)



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, MDAS-940S, MDAS-940D

Typical at +25°C, ± 15 VDC and + 5 VDC supplies, G = 1, ± 10V Input Range, unless otherwise noted

ANALOG INPUTS

- **Number of Channels,**
  - **MDAS-940S** ..... 16 Single Ended
  - **MDAS-940D** ..... 8 Differential
- **Input Voltage Range,**
  - **unipolar** ..... 0 to + 5V, 0 to + 10V
  - **bipolar** ..... ± 5V, ± 10V
- **Input Voltage, No Damage, max.** ± 35V
- **Common Mode Range, min.** .. ± 10V
- **Input Impedance** ..... 100 MΩ
- **Input Bias Current, max.**[1] .... 8 nA
- **Input Capacitance,**
  - **OFF Channel to Ground** .. 10 pF
  - **ON Channel to Ground** ... 100 pF

PERFORMANCE

- **Resolution** ..... 12 Binary Bits
- **Accuracy, G = 1** ..... ± .025% of FSR
- **Nonlinearity, max.** ..... ± 1/2 LSB
- **Diff. Nonlinearity, max.** ..... ± 1/2 LSB
- **Gain Range** 1, 2, 4, 8
- **Gain Error** ..... Adj. to Zero
- **Offset Error** ..... Adj. to Zero
- **Temp. Coeff. of Gain, max.** ... ± 30 ppm of FSR[3]/°C
- **Temp. Coeff. of Offset, max.** ± 7 ppm of FSR[3]/°C
- **Diff. Linearity Tempco, max.** .. ± 3 ppm of FSR[3]/°C
- **Common Mode Rejection, min.** 70 dB
- **Monotonicity** ..... 0°C to + 70°C
- **Power Supply Rejection** 0.01%/%

DYNAMIC CHARACTERISTICS

- **Throughput Rate, min.** ..... 33 kHz
- **Conversion Time** ..... 10 μsec
- **Acquisition Time** ..... 20 μsec
- **Aperture Delay Time** ..... 100 nsec
- **Output Enable Delay, max.** ... 30 nsec
- **Hold Mode Droop, max.** ..... 200 nV/μsec
- **Feedthrough, max.** 0.01%
- **Channel Crosstalk (Mux.), 1 kHz** − 80 dB

DIGITAL OUTPUTS

- **Parallel Output Data (Pins 29T-34T, 29B-34B)** ..... 12 Parallel data lines. Data is arranged as three 4-bit, gateable three-state outputs. Drives 12 TTL loads.
- **High Level Output Current (IOH)** ..... − 15 mA
- **Low Level Output Current (IOL)** 24 mA
- **Off State Output Current (IOZH), max.** ..... 20 μA
- **Output Logic Level, HI ("1"), min.**[4] ..... ≥ 2.4V
- **Output Logic Level, LO ("0"), max.**[4] ..... ≤ 0.5V
- **Output Coding** ..... Straight Binary, Offset Binary, and Two's Complement
- **Serial Output Data (Pin 18T)** .. NRZ successive decision pulses out, MSB first. Straight binary and offset binary coding. Drives 15 TTL loads.
- **Clock Out (Pin 26B)** ..... Train of negative going − 5V, 100 nsec pulses at 1.5 MHz rate. Used as shift clock for serial output data. Drives 15 TTL loads.
- **Delay Output (Pin 25T)** ..... Output Delay pulse set for 20 μsec to allow for multiplexer and amplifier settling time and sample-hold acquisition time. Negative going edge initiates conversion if Trigger (Pin 26T) is open or HI. Drives 5 TTL loads.
- **$\overline{\text{EOC}}$ (Status) (Pin 27B)** ..... Conversion status signal. Output HI during conversion, LO when conversion is complete. Drives 4 TTL loads.
- **Mux. Address Out (19T-22T)** .. Binary coded output of Mux. Address Register. Indicates actual channel address code stored in address register. Should be buffered externally if long etch runs or cables are to be driven. Drives 4 TTL loads.
- **Gain Select Out (1 & 2) (27T, 28T)** ..... Binary coded gain stored in Gain Select Register. Drives 5 TTL loads.
- **MSB Out (Pin 23B)** ..... Bit 1 output of A/D converter. Connected to MSB IN (Pin 24T) for straight binary or offset binary coding. Drives 15 TTL loads.
- **$\overline{\text{MSB}}$ Out (Pin 28B)** ..... Complemented Bit 1 output of A/D converter. Connected to MSB IN (Pin 24T) for Two's Complement coding. Drives 14 TTL loads.

DIGITAL INPUTS[5]

- **OUTPUT ENABLE[6] (Pins 14T, 15B, 17T)** ..... Three separate inputs which enable three-state output data in 4 bit bytes. Input LO enables output, Input HI inhibits output. Loading: 1 LS TTL load.
- **$\overline{\text{STROBE}}$ (Pin 25T)** ..... Negative input transition increments channel address register and enables gain code update in sequential mode or starts a conversion when operating in random mode. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
- **Trigger (Pin 26T)** ..... Positive pulse with 100 nsec duration min. Logic LO to HI transition resets A/D converter and initiates next conversion. A Schmidt trigger input provides hysteresis for good noise rejection and a trigger from slowly rising waveforms. May be left open if not used. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
- **Mux Address In (Pins 14B-22B)** ..... 3 bit MDAS-940D or 4 bit (MDAS-940S) binary address input for channel address selection. Data must be present for 70 nsec min. after the HI to LO transition of STROBE. See channel address table. Loading: 1 LS TTL load.
- **$\overline{\text{LOAD ENABLE}}$ (Pin 24B)** ..... Input HI for sequential addressing. Input LO for random addressing. Loads address code for random addressing on HI to LO transition of $\overline{\text{STROBE}}$. May be left open if not used. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
- **$\overline{\text{CLEAR}}$ $\overline{\text{ENABLE}}$ (Pin 25B)** .... Input LO and a negative transition on $\overline{\text{STROBE}}$ (Pin 25T) resets mux. address register to zero. May be left open if not used. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
- **COUNT ENABLE (Pin 18B)** ... Input HI enables mux address register sequencing. Input LO inhibits Mux Address Register Sequencing. Enable delay is 20 nsec. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
- **Mux Enable (Pin 17B)** ..... Input HI enables analog multiplexer. Input LO disconnects analog multiplexer for external channel expansion. May be left open if not used.
- **Gain Select IN (Pins 16T, 16B)** 2 bit binary address to select gain of internal PGA. See GAIN SELECTION CHART. Loading: 1 LS TTL load
- **MSB IN (Pin 24T)** ..... Bit 1 input to three-state output buffers. Loading: 1 TTL load

POWER REQUIREMENTS

- **Analog Supply** ..... + 15 VDC ± 0.5V @ 110 mA regulated
  − 15 VDC ± 0.5V @ 100 mA regulated
- **Logic Supply** ..... + 5 VDC ± 0.25V @ 275 mA regulated

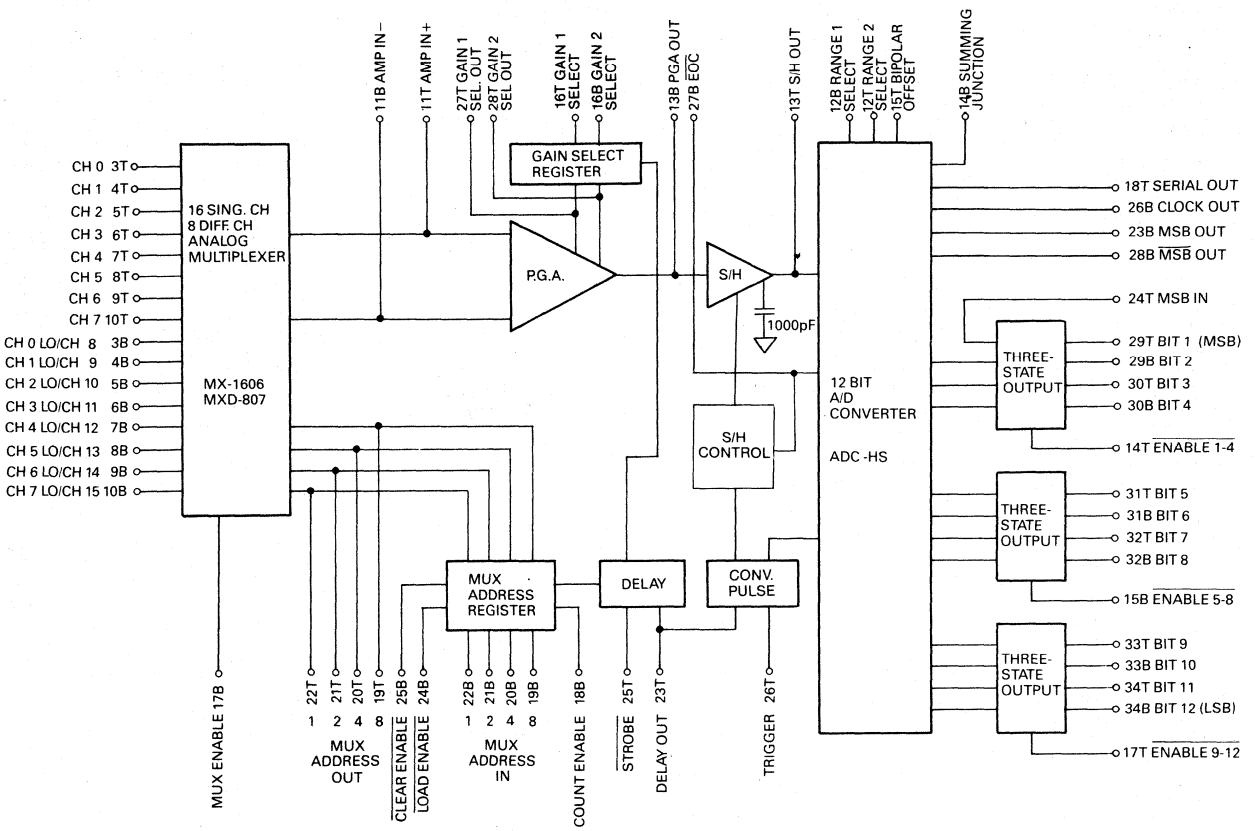
PHYSICAL-ENVIRONMENTAL

- **Operating Temperature Range** ..... 0°C to + 70°C
- **Storage Temperature Range** ... − 25°C to + 85°C
- **Package Size** ..... 4.6 × 3.0 × 0.38 inches (116,8 × 76,2 × 9,7 mm)
- **Package Type** ..... Steel, shielded on 5 sides
- **Weight** ..... 5 oz.

NOTES:

1. Specification is for full temperature range of 0°C to + 70°C.
2. A factory option allows the gain range to be incremented upwards (for example: 10, 20, 40 and 80) for OEM orders. To retain 12 bit linearity, the P.G.A. gain must not exceed 100. For more information contact your nearest Datel-Intersil sales office.
3. FSR is Full Scale Range
4. Logic levels of all other digital outputs are Vout ("1") ≥ + 2.4V and Vout ("0") ≤ + 0.4V.
5. All digital input logic levels are V_{IN} ("1") ≥ + 2.0V and V_{IN} ("0") ≤ + 0.8V.
6. The OUTPUT ENABLE specification refers to three inputs; ENABLE 1-4 (Pin 14T), ENABLE 5-8 (Pin 15b), and ENABLE 9-12 (Pin 17T).

BLOCK DIAGRAM MDAS-940



ORDERING INFORMATION

MODEL	INPUT CHANNEL SELECTION	PRICE (1-9)
MDAS-940D	8 Chan. Differential	
MDAS-940S	16 Chan. Single Ended	

These modules are also available in extended temperature range versions designated with the suffix EX (–25°C to +85°C) or EXX-HS (–55°C to 85°C) with hermetically sealed semiconductor components. Contact factory for price and delivery.

Included with each module is a mating right-angle 72 pin connector. (AMP 3-86063-2). Additional connectors may also be ordered by the following number:
58-2083010 Connector

Multiplexer expander modules are also available. The MDXP-32 adds 32 single ended or 16 differential channels with control logic.
The MDXP-32-1 is identical but without control logic.

PIN CONNECTIONS FOR MDAS-940

	Bottom	Top	
–15VDC	1B	1T	+15VDC
Analog Gnd.	2B	2T	Analog Gnd.
Ch. 8 In/Ch. 0 Lo In	3B	3T	Ch. 0 In/Ch. 0 Hi In
Ch. 9 In/Ch. 1 Lo In	4B	4T	Ch. 1 In/Ch. 1 Hi In
Ch. 10 In/Ch. 2 Lo In	5B	5T	Ch. 2 In/Ch. 2 Hi In
Ch. 11 In/Ch. 3 Lo In	6B	6T	Ch. 3 In/Ch. 3 Hi In
Ch. 12 In/Ch. 4 Lo In	7B	7T	Ch. 4 In/Ch. 4 Hi In
Ch. 13 In/Ch. 5 Lo In	8B	8T	Ch. 5 In/Ch. 5 Hi In
Ch. 14 In/Ch. 6 Lo In	9B	9T	Ch. 6 In/Ch. 6 Hi In
Ch. 15 In/Ch. 7 Lo In	10B	10T	Ch. 7 In/Ch. 7 Hi In
Amplifier In	11B	11T	Amplifier In +
Range 2 Select	12B	12T	Range 1 Select
P.G.A. Out	13B	13T	Sample Hold Out
Sum. Junc.	14B	14T	$\overline{\text{Enable}}$ (Bits 1-4 Out)
$\overline{\text{Enable}}$ (Bits 5-8 Out)	15B	15T	Bipolar Offset
Gain 2 Select In	16B	16T	Gain 1 Select In
Mux Enable	17B	17T	$\overline{\text{Enable}}$ (Bits 9-12)
Count Enable	18B	18T	Serial Out
8 In } Mux	19B	19T	8 Out } Mux
4 In } Address	20B	20T	4 Out } Address
2 In } Lines	21B	21T	2 Out } Lines
1 In }	22B	22T	1 Out }
MSB Out (TTL)	23B	23T	Delay Out
$\overline{\text{Load Enable}}$	24B	24T	MSB In (TTL)
$\overline{\text{Clear Enable}}$	25B	25T	$\overline{\text{Strobe}}$
Clock Out	26B	26T	Trigger
$\overline{\text{EOC}}$ (status)	27B	27T	Gain 1 Select Out
$\overline{\text{MSB}}$ Out (TTL)	28B	28T	Gain 2 Select Out
Bit 2 Out*	29B	29T	Bit 1 Out* (MSB)
Bit 4 Out*	30B	30T	Bit 3 Out*
Bit 6 Out*	31B	31T	Bit 5 Out*
Bit 8 Out*	32B	32T	Bit 7 Out*
Bit 10 Out*	33B	33T	Bit 9 Out*
Bit 12 Out* (LSB)	34B	34T	Bit 11 Out*
Digital Gnd.	35B	35T	Digital Gnd.
+5VDC	36B	36T	+5VDC

*Three-State Outputs

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1T	+15 VDC	Positive analog supply voltage. +15 VDC @ 65 mA typical.
1B	−15 VDC	Negative analog supply voltage. −15 VDC @ 60 mA typical.
2T/2B	Analog Gnd.	Analog common. Analog common and digital common (Pins 35T/35B) are connected within the module and should not be connected externally.
3T/3B through 10T/10B	Ch. In	Analog inputs to multiplexer. MDAS-940S has 16 single-ended inputs. The MDAS-940D has 8 differential inputs.
11T	Amplifier In +	Analog monitoring point for the positive input of the internal Programmable Gain Amplifier.
11B	Amplifier In −	Analog monitoring point for the negative input of the internal Programmable Gain Amplifier. For normal operation on the MDAS-940S this pin must be grounded.
12T	Range 1 Select	A/D converter input resistor. Should be grounded when not being used. See Input Range Selection Chart.
12B	Range 2 Select	A/D converter input resistor. Should be grounded when not being used. See Input Range Selection Chart.
13T	Sample-Hold Output	Sample-Hold output. Connect to desired range select pin for normal operation. See Input Range Selection Chart.
13B	P.G.A. Out	Analog monitoring point for the output of the internal Programmable Gain Amplifier.
14T	$\overline{\text{ENABLE}}$ 1-4	Enable line for three-state output, bits 1-4. Input LO enables output, input HI inhibits output. Max. enable delay is 30 nsec.
14B	Summing Junction	Comparator input for A/D converter, used in range selection. See Input Range Selection Chart. Make no other external connections to prevent performance degradation.
15T	Bipolar Offset	A/D Converter Bipolar Offset. Connect to Summing Junction (Pin 14B) for bipolar operation, or to analog common (Pins 2T/2B) for unipolar operation. See Input Range Selection Chart.
15B	$\overline{\text{ENABLE}}$ 5-8	Enable Line for three-state outputs, bits 5-8. Input LO enables output, input HI inhibits output. Max. enable delay is 30 nsec.
16T/16B	Gain Select IN 1 & 2	Address lines that select gain of internal Programmable Gain Amplifier. Gains of 1,2,4, or 8 may be selected. See Gain Selection Chart.
17T	$\overline{\text{ENABLE}}$ 9-12	Enable line for three-state outputs, bits 9-12. Input LO enables output, input HI inhibits output. Max. enable delay is 30 nsec.
17B	MUX. ENABLE	Enable line for analog multiplexer. Input HI enables multiplexer, Input LO disconnects multiplexer for external channel expansion.

PIN	MNEMONIC	DESCRIPTION
18T	Serial Out	Serial Output data in NRZ format, MSB first. Data is synchronous with Clock OUT (Pin 26B), use negative edge of clock to strobe each bit.
18B	Count Enable	Enable line for Mux. Address Register Sequencing. Input HI enables register sequencing, Input LO inhibits register sequencing. Enable delay is 20 nsec.
19T Through 22T	Mux. Address OUT	Binary coded output of Mux Address Register.
19B Through 22B	Mux. Address IN	Address lines that select one out of 16 (8-MDAS-940D) input channels when operating in the random addressing mode. Straight binary coding.
23T	Delay OUT	20 μsec pulse used to delay start of A/D conversion to allow settling of the multiplexer, amplifier, and sample-hold. Negative going edge initiates A/D conversion.
23B	MSB Out	Bit 1 output of A/D converter. Connected to MSB IN (Pin 24T) for straight binary or offset binary coding.
24T	MSB IN	Bit 1 input to three-state output buffer. Connect to MSB OUT (Pin 23B) for straight or offset binary coding. Connect to $\overline{\text{MSB OUT}}$ (Pin 28B) for Two's Complement coding.
24B	$\overline{\text{LOAD}}$ $\overline{\text{ENABLE}}$	Input HI for sequential addressing. Input LO for random addressing.
25T	STROBE	Negative input transition initiates channel sequencing and gain selection in sequential mode, A/D conversion when in random mode.
25B	$\overline{\text{CLEAR}}$ $\overline{\text{ENABLE}}$	Input LO in conjunction with a negative transition on $\overline{\text{STROBE}}$ (Pin 25T) will reset the mux address register to zero.
26T	Trigger	Logic LO to HI transition resets A/D converter and initiates next conversion.
26B	Clock OUT	A/D converter clock output.
27T	Gain 1 Select OUT	Output 1 of Gain Select Register.
27B	$\overline{\text{EOC}}$	Conversion status signal. Output HI during conversion, LO when conversion is complete.
28T	Gain 2 Select OUT	Output 2 of Gain Select Register.
28B	$\overline{\text{MSB}}$ out	Complimented Bit-1 output of A/D converter. Connected to MSB in (Pin 24T) for two's complement coding.
29T/29B Through 34T/34B	Data Outputs	Three-state digital outputs.
35T/35B	Digital Ground	Digital common. Digital Common and Analog Common (Pins 2T/2B) are connected within the module and should not be connected externally.
36T/36B	Logic Supply	+5 VDC @ 200 mA typical.

1. Select input voltage range desired and connect pins 12B, 12T, and 15T in accordance with Table II. If the MDAS 940S is used, ground pin 11B. Ground all analog channel inputs which are not to be used. Leave pin 17B open.
2. Select the output coding desired. For straight binary (unipolar) or offset binary (bipolar) connect pin 23B (MSB Out) to pin 24T (MSB In). For two's complement (bipolar), connect pin 28B ($\overline{\text{MSB}}$ Out) to pin 24T.
3. Select desired multiplexer mode.

   A. Free Running Sequential Addressing

   Connect pin 27B ($\overline{\text{EOC}}$) to pin 25T ($\overline{\text{Strobe}}$). Leave pins 24B ($\overline{\text{Load Enable}}$) and 25B ($\overline{\text{Clear Enable}}$) open. Sequencing is initiated by a positive logic transition applied to pin 26T (Trigger). Pin 26T must remain HI during free running sequential addressing. Sequencing is stopped by a LO applied to pin 26T.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

MUX CHANNEL ADDRESSING

MUX ADDRESS PIN					ON CHANNEL	
19B	20B	21B	22B	17B		
8	4	2	1	MUX ENAB.	MDAS 940S	MDAS 940D
X	X	X	X	0	—	—
0	0	0	0	1	1	1
0	0	0	1	1	2	2
0	0	1	0	1	3	3
0	0	1	1	1	4	4
0	1	0	0	1	5	5
0	1	0	1	1	6	6
0	1	1	0	1	7	7
0	1	1	1	1	8	8
1	0	0	0	1	9	—
1	0	0	1	1	10	—
1	0	1	0	1	11	—
1	0	1	1	1	12	—
1	1	0	0	1	13	—
1	1	0	1	1	14	—
1	1	1	0	1	15	—
1	1	1	1	1	16	—

INPUT RANGE SELECTION

	CONNECT THESE PINS TOGETHER		
INPUT RANGE	RANGE 1 PIN 12T	RANGE 2 PIN 12B	BIPOLAR OFF. PIN 15T
0 TO + 5V	13T	—	2T or 2B
0 TO + 10V	13T	—	2T or 2B
± 5V	13T	—	14B
± 10V	—	13T	14B

   B. Triggered Sequential Addressing

   Leave pins 24B ($\overline{\text{Load Enable}}$) and 25B ($\overline{\text{Clear Enable}}$) open. Apply a falling edge trigger to pin 25T ($\overline{\text{Strobe}}$). The negative transition of the strobe will cause the contents of the address counter to be incremented by one.

4. CALIBRATION

   A. Connect power supplies to module and ground all analog channel inputs. Monitor PGA Out pin (Pin 13B) and adjust P.G.A. Null adjustment for 0.0000V.

   B. Connect a precision voltage source to pin 3T (Chan 0 In). If the MDAS-940D is used, connect pin 3B (Chan 0LO) to analog ground. Ground pin 25B (Clear Enable) and momentarily short pin 25T (Strobe) to ground. Use an oscilloscope to monitor the serial output code at pin 18T. Trigger the A/D converter with 50kHz positive going pulses applied to pin 26T (Trigger).

   C. Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + ½ LSB) or the bipolar offset adjustment (− FS + ½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

   D. Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+ FS − 1½ LSB). Adjust the gain trimming potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

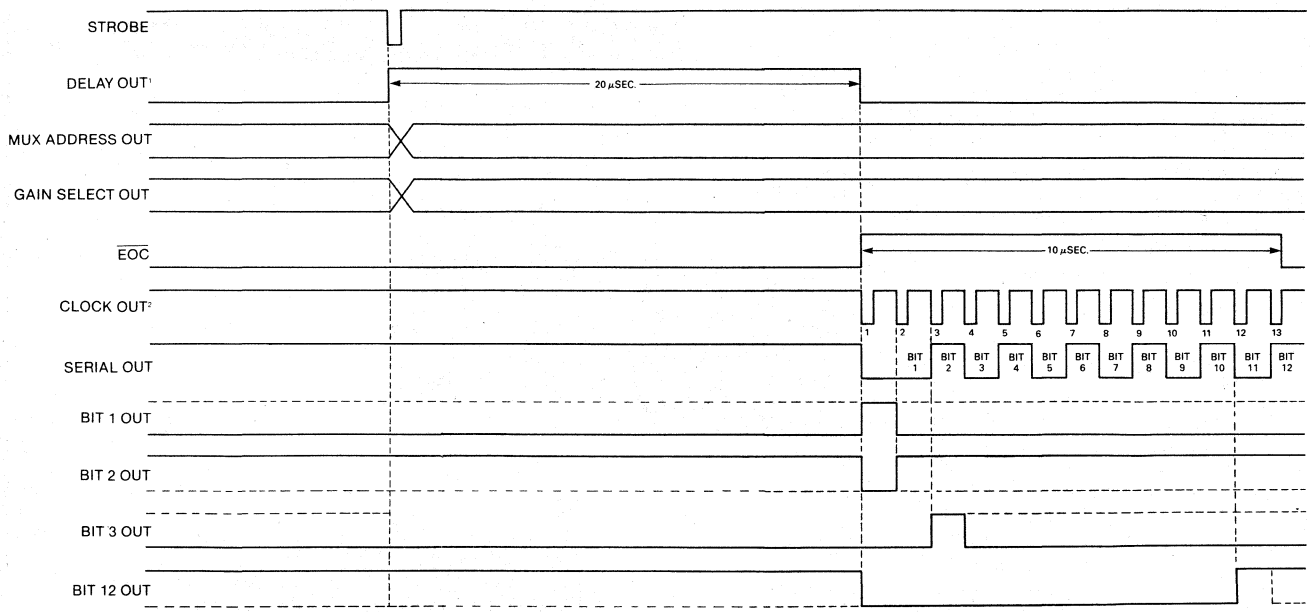
GAIN SELECTION CHART

GAIN SELECT 1	GAIN SELECT 2	PGA GAIN[1]
0	0	1
0	1	2
1	0	4
1	1	8

[1] A factory option allows the gain range to be incremented upwards (for example: 10, 20, 40 and 80) for OEM orders. To retain 12 bit linearity, the P.G.A. gain must not exceed 100. For more information contact your nearest Datel-Intersil sales office.

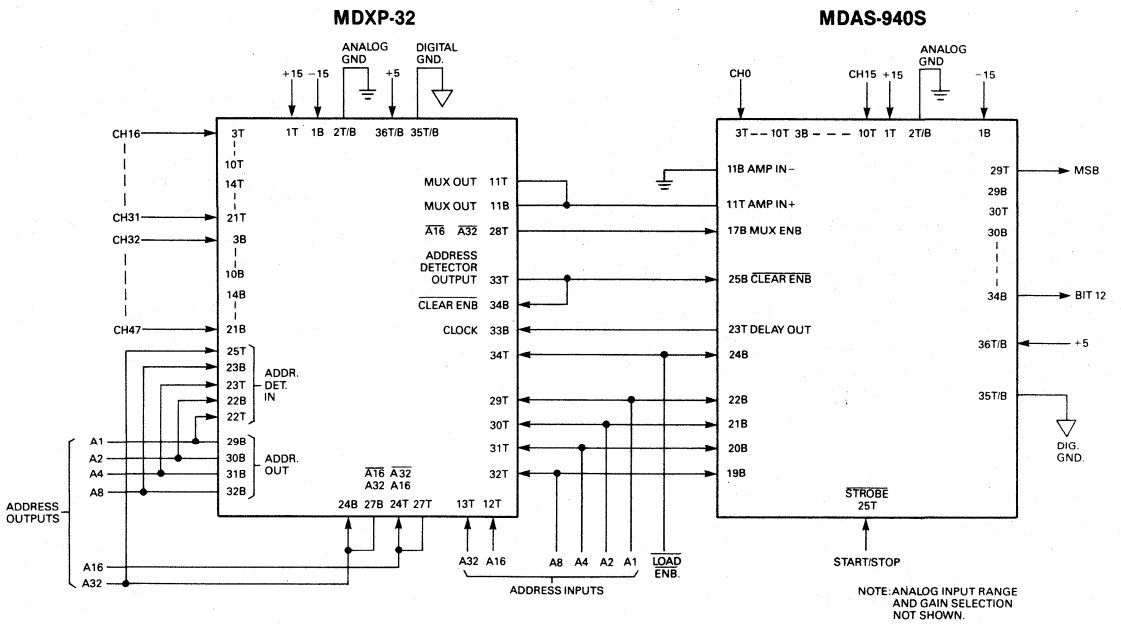
TIMING AND CHANNEL EXPANSION

TIMING DIAGRAM OUTPUT CODE: 010101010101



1. Negative going edge of Delay pulse initiates conversion if Trigger (Pin-26T) is open or HI.
2. Train of negative going −5V, 100 nsec. pulses at 1.5 MHz rate.

CHANNEL EXPANSION WITH MDXP-32 AND MDXP-32-1
SINGLE LEVEL MULTIPLEXING FOR 48 SINGLE-ENDED CHANNELS



Datel-Intersil's MDX-P-32 and MDXP-32-1 are input channel expansion modules that are compatible with the MDAS-940. Both models contain 32 analog multiplex channels which permit expanding the MDAS-940S up to 48 single ended channels and the MDAS-940D up to 24 differential channels. With double level multiplexing up to 256 single ended channels or 128 differential channels can be achieved using 1 MDXP-32 and 7 MDXP-32-1's. Both modules are contained in a 4.6 x 2.5 x 0.375 in. shielded steel case and operate over the 0°C to +70°C temperature range.

Data Acquisition Expander Modules MDXP-32, MDXP-32-1

FEATURES

- **Compatible with MDAS-16 MDAS-8D, or MDAS-940**
- **32 Single Ended Channels**
- **16 Differential Channels**
- **Expansion to 256 Channels**
- **Miniature Module**
- **Low Cost**

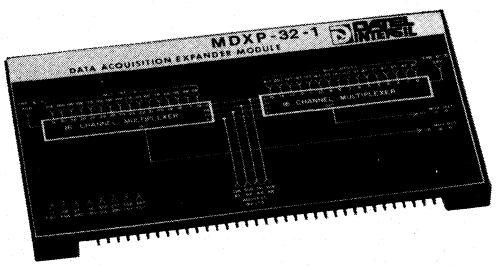
GENERAL DESCRIPTION

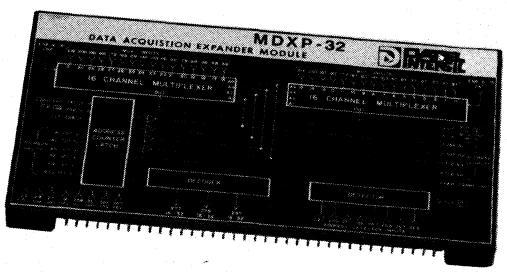
The MDXP-32 and MDXP-32-1 are companion devices to Datel Intersil's MDAS-16, MDAS-8D and MDAS-940 Miniature Modular Data Acquisition Systems. They can also be used with data acquisition systems from other manufacturers. Both models contain 32 analog multiplex channels which permit expanding the MDAS-16 or MDAS-940S up to 48 single ended channels and the MDAS-8D or MDAS-940-D up to 24 differential channels using single level multiplexing. With double level multiplexing up to 256 single ended channels or 128 differential channels can be realized using 1 MDXP-32 and 7 MDXP-32-1's with an MDAS-16, MDAS-8D, or MDAS-940.

The MDXP-32 contains an address counter, address decoder, address detector logic, and two 16 channel analog multiplexers. The MDXP-32-1 contains two 16 channel analog multiplexers and an address decoder. The expanded systems can be operated in three modes: free running sequential addressing, triggered sequential addressing, or random addressing. In sequential operation the system can be short cycled to any number of desired channels less than the maximum by use of the address detector in the MDXP-32. The MDXP-32-1 can be used to expand the MDAS-16 or MDAS-8D for random addressing operation only.

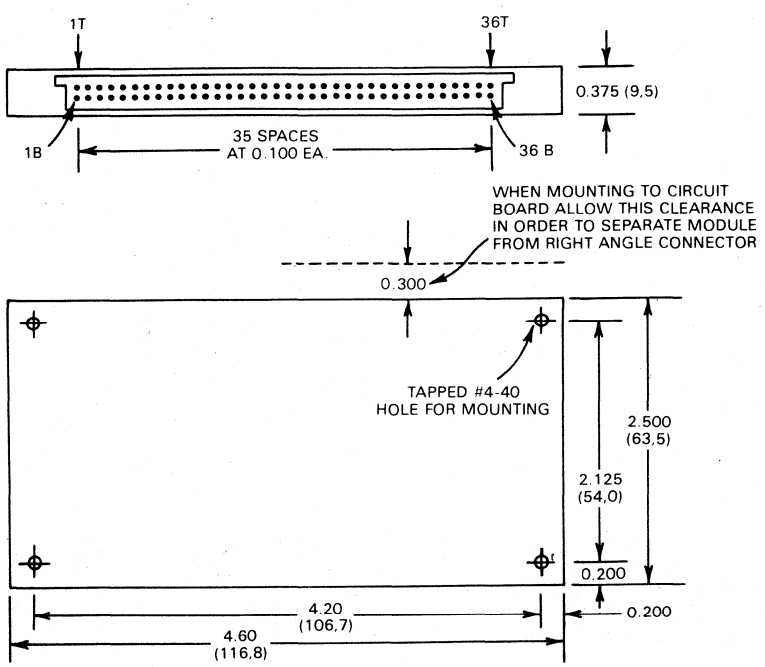
The analog multiplexers in these units are dielectrically isolated CMOS with fully protected inputs. The ON resistance of each channel is typically 1.5K ohms. Transfer accuracies better than 0.01% are achieved if a very high impedance load such as a unity gain buffer amplifier input is used. The channels switch with a break-before-make delay of 80 nsec.

Both the MDXP-32 and MDXP-32-1 are contained in a 4.6 x 2.5 x 0.375 inch (116,8 x 63,5 x 9,5 mm) shielded steel case. Operating temperature range is 0°C to 70°C.





MECHANICAL DIMENSIONS - INCHES (MM)



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, MDXP-32 & MDXP-32-1
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

MAXIMUM RATINGS

Positive Supply Voltage, pin 1T ... +20V
Negative Supply Voltage, pin 1B .. −20V
Logic Supply Voltage, pins 36T & 36B ..... +5.5V
Digital Input Voltages ..... +5.5V
Analog Input Voltages ..... +Supply +20V
−Supply −20V

ANALOG INPUTS

Number of Channels, single ended 32
Number of Channels, differential . 16
Input Voltage Range ..... ±15V
Channel ON Resistance 1.5K
Channel ON Resistance, max. 0°C to 70°C 2.0K
Channel OFF Input Leakage 30pA
Channel ON Input Leakage 100pA

DIGITAL INPUTS

Input Logic Level[1], HI ("1") ..... +2.0V to +5.5V
Input Logic Level[1], LO ("0") ..... 0V to +0.8V
Logic Loading[1] ..... 1 LS TTL load
Address Coding ..... 4 bits (MDXP-32-1)
6 bits (MDXP-32)
Mux Enable Inputs[2], enable ..... HI (+4.0V to +Supply)
disable ..... LO (0 to +0.8V)

DIGITAL OUTPUTS

Output Logic Level, HI ("1") ..... +2.4V Min.
Output Logic Level, LO ("0") ..... +0.4V Max.
Output Drive Capability ..... 10 LS TTL loads

PERFORMANCE

Transfer Error, max.[3] 0.01%
Channel Crosstalk, 1 kHz ..... −80 dB
Turn ON Time ..... 500 nsec.
Turn OFF Time ..... 300 nsec.
Break-Before-Make Delay ..... 80 nsec.
Inhibit/Enable Delay ..... 300 nsec.

POWER REQUIREMENT ..... +15VDC ±0.5V @ 10mA
−15VDC ±0.5V @ 4mA
+5VDC ±0.25V @ 100mA[4]

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range ... 0°C to 70°C
Storage Temperature Range ..... −25°C to +85°C
Package Size ..... 4.6 x 2.5 x 0.375 inches
116,8 x 63,5 x 9,5 mm
Package Type ..... Steel, shielded on 5 sides
Weight ..... 6 oz. (170 g.)

NOTES:

1. All digital inputs except for Mux Enable Inputs on both models and Address Inputs on MDXP-32-1.
2. The logic levels are also the same for the Address Inputs on MDXP-32-1.
3. For zero source impedance and ⩾ 20 megohm load impedance.
4. MDXP-32 only. The MDXP-32-1 does not use +5V power.

ORDERING INFORMATION

MDXP-32 .....
MDXP-32-1 .....

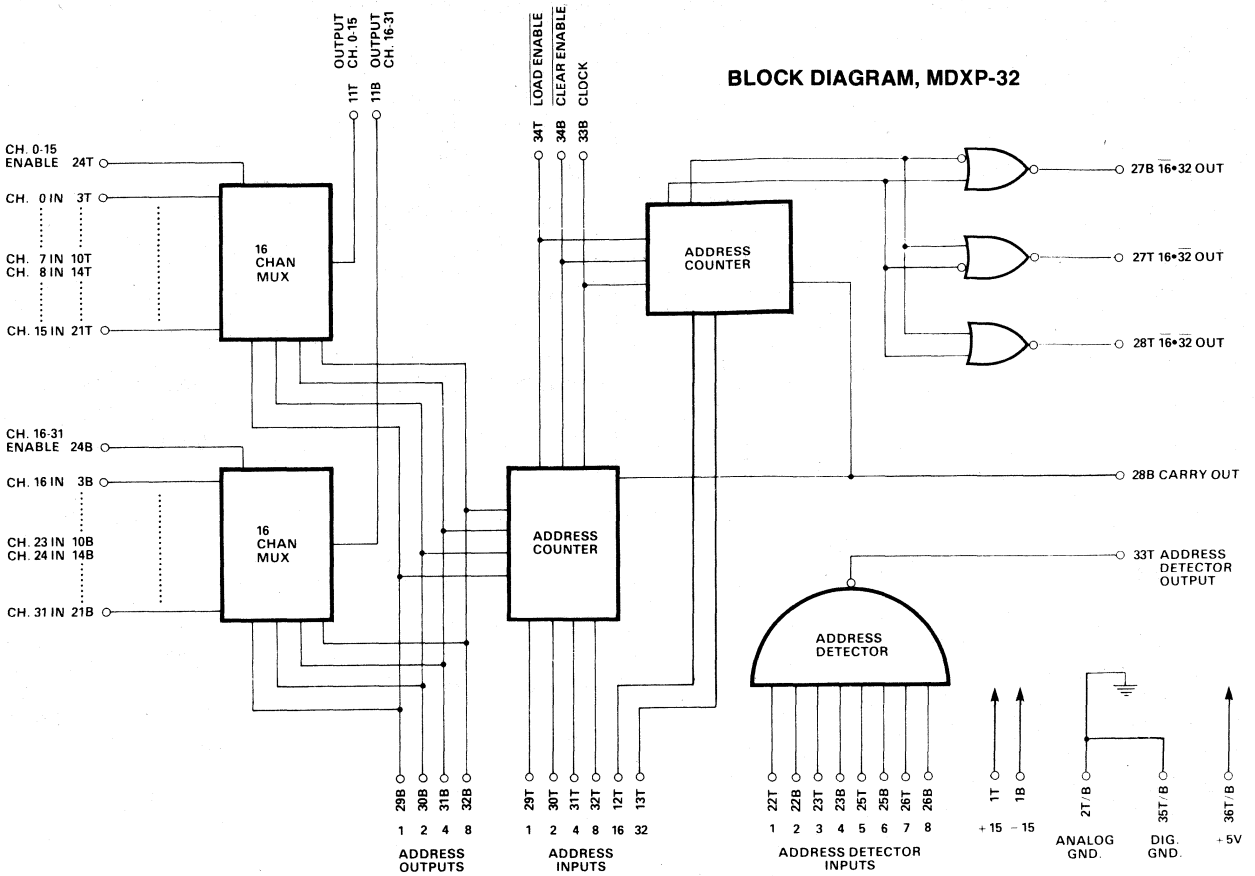
Included with each module is a mating right-angle 72-pin connector. Additional connectors may also be ordered by the following number.

58-2083010 Connector

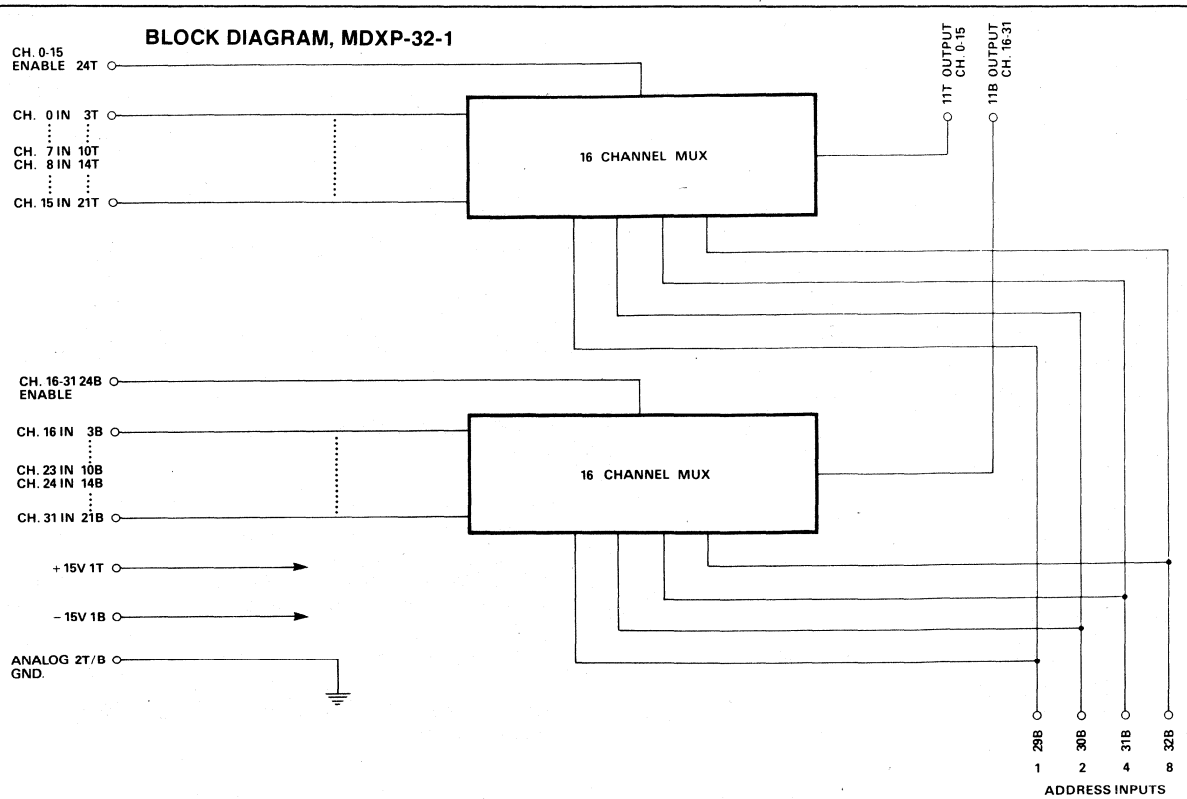
THE MDXP-32 AND MDXP-32-1 ARE COVERED BY GSA CONTRACT

BLOCK DIAGRAMS

BLOCK DIAGRAM, MDXP-32



BLOCK DIAGRAM, MDXP-32-1



INPUT/OUTPUT CONNECTIONS

PIN CONNECTIONS for MDXP-32

	Top	Bottom	
+15VDC	1T	1B	−15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 16 In
Ch. 1 In	4T	4B	Ch. 17 In
Ch. 2 In	5T	5B	Ch. 18 In
Ch. 3 In	6T	6B	Ch. 19 In
Ch. 4 In	7T	7B	Ch. 20 In
Ch. 5 In	8T	8B	Ch. 21 In
Ch. 6 In	9T	9B	Ch. 22 In
Ch. 7 In	10T	10B	Ch. 23 In
Output, Ch. 0-15	11T	11B	Output, Ch. 16-31
16 In } Address	12T	12B	NC
32 In } Inputs	13T	13B	NC
Ch. 8 In	14T	14B	Ch. 24 In
Ch. 9 In	15T	15B	Ch. 25 In
Ch. 10 In	16T	16B	Ch. 26 In
Ch. 11 In	17T	17B	Ch. 27 In
Ch. 12 In	18T	18B	Ch. 28 In
Ch. 13 In	19T	19B	Ch. 29 In
Ch. 14 In	20T	20B	Ch. 30 In
Ch. 15 In	21T	21B	Ch. 31 In
Addr. Det. In 1	22T	22B	Addr. Det. In 2
Addr. Det. In 3	23T	23B	Addr. Det. In 4
Enable Ch. 0-15	24T	24B	Enable Ch. 16-31
Addr. Det. In 5	25T	25B	Addr. Det. In 6
Addr. Det. In 7	26T	26B	Addr. Det. In 8
$\overline{16 \cdot 32}$ Out	27T	27B	$\overline{16 \cdot 32}$ Out
$\overline{16 \cdot 32}$ Out	28T	28B	Carry Out
1 In }	29T	29B	1 Out }
2 In } Address	30T	30B	2 Out } Address
4 In } Inputs	31T	31B	4 Out } Outputs
8 In }	32T	32B	8 Out }
$\overline{\text{Address Det. Out}}$	33T	33B	$\overline{\text{Clock}}$
Load Enable	34T	34B	Clear Enable
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC

PIN CONNECTIONS for MDXP-32-1

	Top	Bottom	
+15VDC	1T	1B	−15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 16 In
Ch. 1 In	4T	4B	Ch. 17 In
Ch. 2 In	5T	5B	Ch. 18 In
Ch. 3 In	6T	6B	Ch. 19 In
Ch. 4 In	7T	7B	Ch. 20 In
Ch. 5 In	8T	8B	Ch. 21 In
Ch. 6 In	9T	9B	Ch. 22 In
Ch. 7 In	10T	10B	Ch. 23 In
Output, Ch. 0-15	11T	11B	Output, Ch. 16-31
NC	12T	12B	NC
NC	13T	13B	NC
Ch. 8 In	14T	14B	Ch. 24 In
Ch. 9 In	15T	15B	Ch. 25 In
Ch. 10 In	16T	16B	Ch. 26 In
Ch. 11 In	17T	17B	Ch. 27 In
Ch. 12 In	18T	18B	Ch. 28 In
Ch. 13 In	19T	19B	Ch. 29 In
Ch. 14 In	20T	20B	Ch. 30 In
Ch. 15 In	21T	21B	Ch. 31 In
NC	22T	22B	NC
NC	23T	23B	NC
Enable Ch. 0-15	24T	24B	Enable Ch. 16-31
NC	25T	25B	NC
NC	26T	26B	NC
NC	27T	27B	NC
NC	28T	28B	NC
NC	29T	29B	1 In }
NC	30T	30B	2 In } Address
NC	31T	31B	4 In } Inputs
NC	32T	32B	8 In
NC	33T	33B	NC
NC	34T	34B	NC
NC	35T	35B	NC
NC	36T	36B	NC

DESCRIPTION OF CONTROL PIN FUNCTIONS

FUNCTION	PIN	DESCRIPTION
Load Enable	34T	Input HI for sequential addressing and LO for random addressing. Connect to MDAS Load Enable (pin 24B).
Clear Enable	34B	When input is LO a negative transition on the MDAS Strobe resets Address counter to zero. Connect to MDAS Clear Enable (pin 25B).
Clock	33B	Each LO to HI transition at this input increments the address counter. Connect to MDAS Delay Out (pin 23T).
Carry Out	28B	Output carry of the address counter which is used in double level multiplexing. Connect to MDAS Count Enable (pin 18B).
Address Detector Inputs	22T thru 26T 22B thru 26B	NAND gate inputs used to short cycle the number of channels in sequential mode. When all inputs are HI the Address Counter can be reset. Connect to Address Outputs and leave unused inputs open.
Address Detector Output	33T	For short cycled sequential operation connect to Clear Enable on MDXP-32 (pin 34B) and MDAS (pin 25B). When output goes LO the Address Counter stops and is reset to zero when a negative transition is applied to the MDAS Strobe (pin 25T).
16·32 Out	28T	Decoder output enables channels 0 to 15 of the multiplexer for single level multiplexing. Connect to MDAS (pin 17B) for single-ended operation and MDXP-32 (pins 24B and 24T) for differential operation.
16·32 Out	27T	Decoder output enables channels 16 to 31 of the multiplexer for single-level multiplexing. Connect to pin 24T for single-ended operation and MDAS (pin 17B) for differential operation.
16·32 Out	27B	Decoder output enables channels 32 to 47 of the multiplexer for single-level multiplexing. Connect to pin 24B for single-ended operation and leave unconnected for differential operation.
Address Inputs	29T thru 32T	Input channel address. Connect to MDAS Address Inputs for single-level multiplexing.
Mux Enable	24B, 24T	Input HI enables multiplexer.

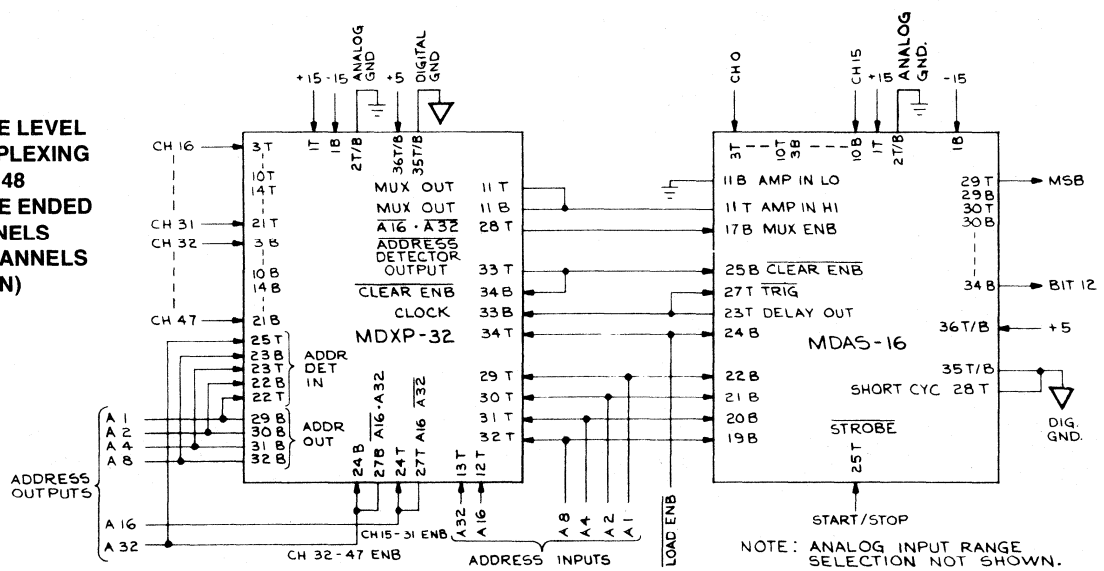
APPLICATION NOTES

SINGLE LEVEL MULTIPLEXING

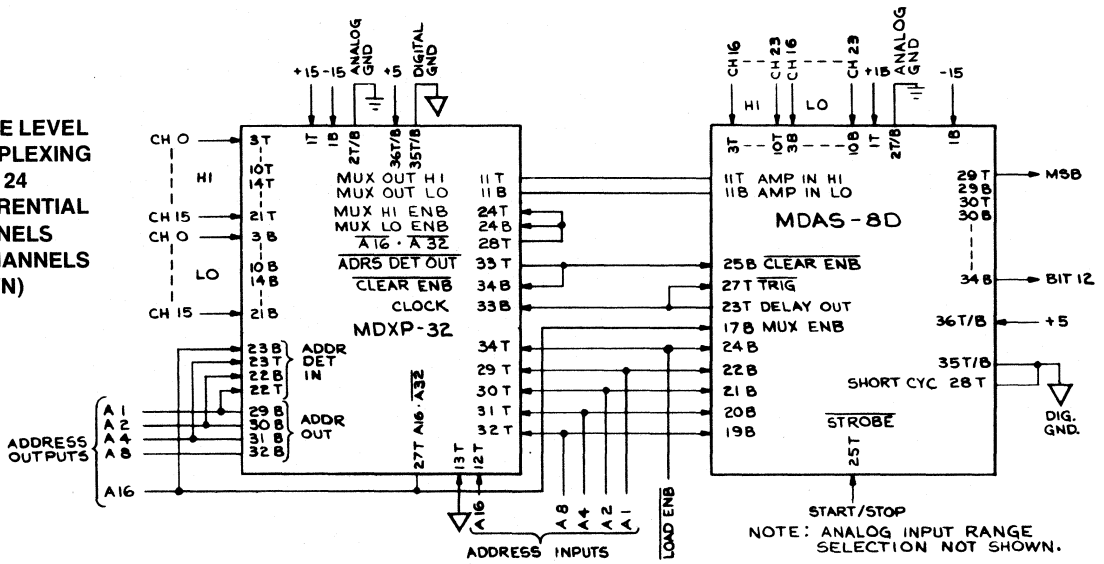
1. For up to 48 single-ended channels or up to 24 differential channels, single level multiplexing is used. This requires one MDAS-16 or MDAS-940S and one MDXP-32 or one MDAS-8D or MDAS-940D and one MDXP-32.
2. The three Address Decoder outputs are used in single level multiplexing only, to control the Mux Enable inputs as follows:

   $\overline{16} \cdot \overline{32}$ Output selects Channels 0 to 15 (MDAS pin 17B)
   $16 \cdot \overline{32}$ Output selects Channels 16 to 31 (MDXP-32 pin 24T)
   $\overline{16} \cdot 32$ Output selects Channels 32 to 47 (MDXP-32 pin 24B)
3. Address inputs 1, 2, 4, 8 are common to both MDAS and MDXP-32. Address inputs 16 and 32 are applied to the MDXP-32 only.
4. For short cycling, which is required for sequential operation for any number of channels less than 256, the Address Outputs of the MDXP-32 are connected to the Address Detector Inputs. The rule is to connect Address Outputs whose binary value equals the number of the last channel in sequence. Note that channels are counted from 0 to 47. For example, for 37 channels the Address Outputs 4 and 32 would be used (adding up to 36).

SINGLE LEVEL MULTIPLEXING UP TO 48 SINGLE ENDED CHANNELS (48 CHANNELS SHOWN)



SINGLE LEVEL MULTIPLEXING UP TO 24 DIFFERENTIAL CHANNELS (24 CHANNELS SHOWN)



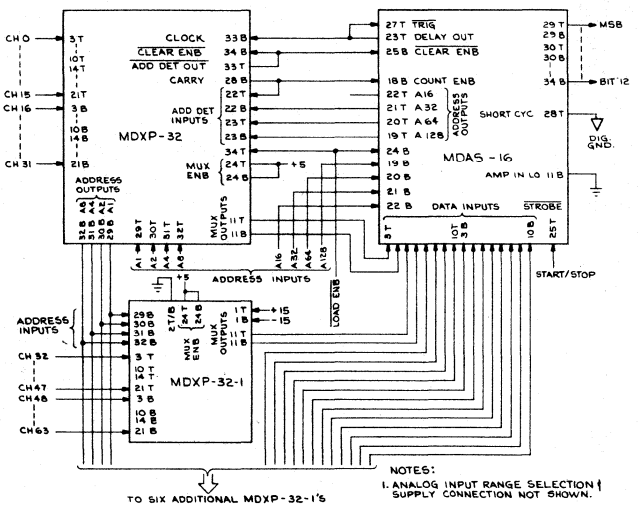
APPLICATION NOTES

DOUBLE LEVEL MULTIPLEXING

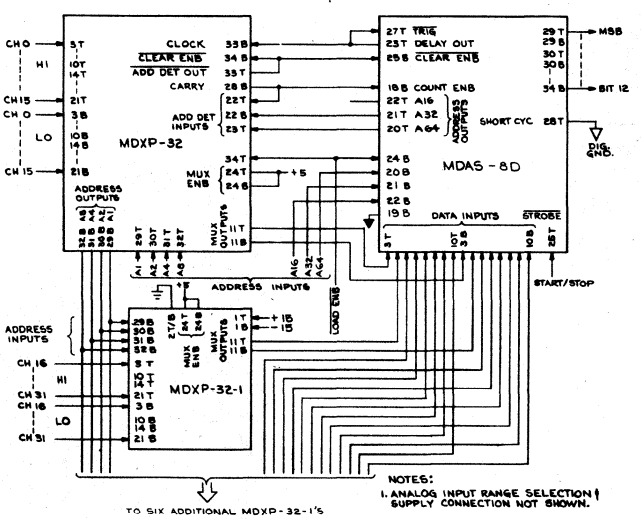
1. For more than 48 single ended channels or more than 24 differential channels, double level multiplexing is required. Up to 256 single ended and up to 128 differential channels may be achieved by double level multiplexing. This technique uses all the channels of the MDAS for the second level of multiplexing so that these channels cannot be used as input channels.
2. One MDXP-32 and one MDAS-16 or MDAS-940S give 32 single ended channels, and each added MDXP-32-1 gives another 32 channels. Likewise, one MDXP-32 and one MDAS-8D or MDAS-940D give 16 differential channels and each added MDXP-32-1 gives another 16 channels.
3. With double level multiplexing the Mux Enable inputs of the MDXP-32 and MDXP-32-1's are connected to +5V to permanently enable them.
4. One input to the Address Detector Inputs is the Carry Out (pin 28B). As a result of this connection the other Address Detector Inputs are determined from the desired number of channels as follows:

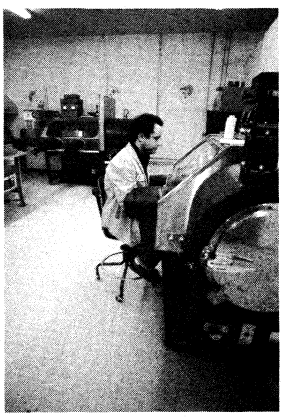
   Channel No. − 15 = Binary value of Address Outputs
   Remembering that the channel count is from 0 to 255 the address output required for 157 channels would be
   156 − 15 = 140
   This requires binary Address Outputs of 128, 8, and 4.
5. In the case of using the maximum 256 channels, the connection from the Address Detector Output (pin 33T) to Clear Enable (pin 34B) is left open and no Address Detector Inputs are required.

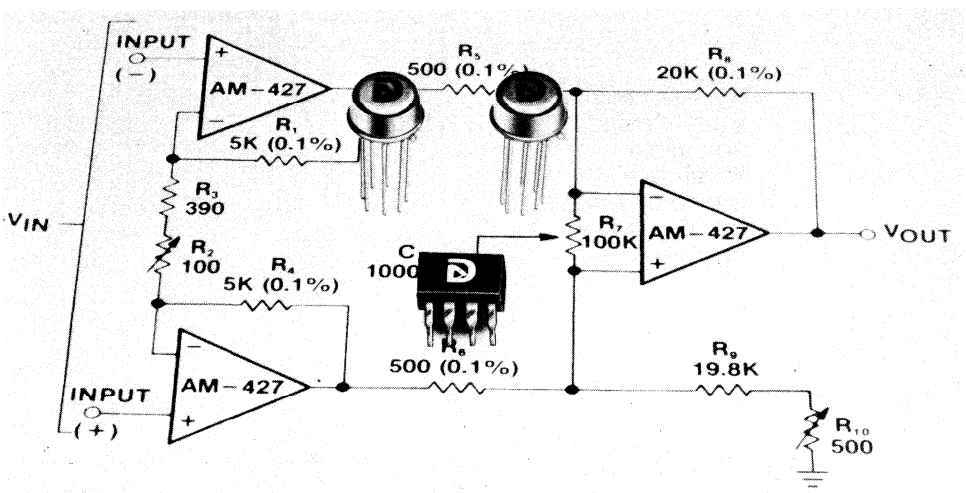
DOUBLE LEVEL MULTIPLEXING FOR UP TO 256 SINGLE ENDED CHANNELS (240 CHANNELS SHOWN)

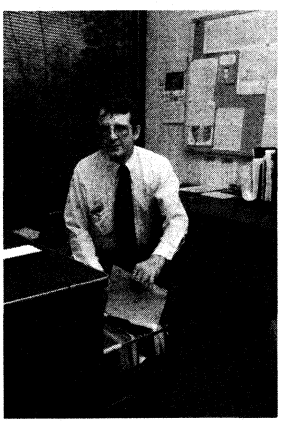


DOUBLE LEVEL MULTIPLEXING FOR UP TO 128 DIFFERENTIAL CHANNELS (112 CHANNELS SHOWN)






INPUT
(−)
AM−427
+
−
R1
5K (0.1%)
R5
500 (0.1%)
R8
20K (0.1%)
R3
390
VIN
R2
100
R4
5K (0.1%)
C
1000
R7
100K
AM−427
VOUT
R6
500 (0.1%)
R9
19.8K
INPUT
(+)
AM−427
R10
500



OPERATIONAL AMPLIFIERS

INSTRUMENTATION AMPLIFIERS

ISOLATION AMPLIFIERS

Operational-Amplifier Technology

Operational and Instrumention Amplifiers

The front end of a data acquisition system extracts the desired analog signal from a physical parameter by means of a transducer and then amplifies and filters it. An amplifier and filter are critical components in this initial signal processing.

The amplifier must perform one or more of the following functions: boost the signal amplitude, buffer the signal, convert a signal current into a voltage, or extract a differential signal from common mode noise.

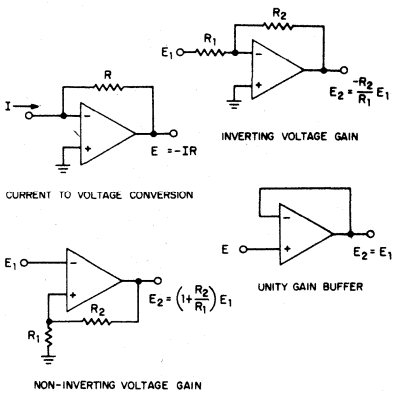


Figure 1. Operational Amplifier Configurations

To accomplish these functions requires a variety of different amplifier types. The most popular type of amplifier is an *operational amplifier* which is a general purpose gain block with differential inputs. The op amp may be connected in many different closed loop configurations, of which a few are shown in Figure 1. The gain and bandwidth of the circuits shown depend on the external resistors connected around the amplifier. An operational amplifier is a good choice in general where a single-ended signal is to be amplified, buffered, or converted from current to voltage.

In the case of differential signal processing, the *instrumentation amplifier* is a better choice since it maintains high impedance at both of its differential inputs and the gain is set by a resistor located elsewhere in the amplifier circuit. One type of instrumentation amplifier circuit is shown in Figure 2. Notice that no gain-setting resistors are connected to either of the input terminals. Instrumentation amplifiers have the following important characteristics.

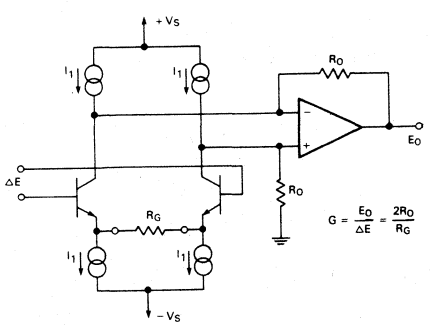


Figure 2. Simplified Instrumentation Amplifier Circuit

1. High impedance differential inputs.
2. Low input offset voltage drift.
3. Low input bias currents.
4. Gain easily set by means of one or two external resistors.
5. High common-mode rejection ratio.

Common Mode Rejection

Common-mode rejection ratio is an important parameter of differential amplifiers. An ideal differential input amplifier responds only to the voltage difference between its input terminals and does not respond at all to any voltage that is common to both input terminals (common-mode voltage). In nonideal amplifiers, however, the common-mode input signal causes some output response even though small compared to the response to a differential input signal.

The ratio of differential and common-mode responses is defined as the common-mode rejection ratio. *Common-mode rejection ratio of an amplifier is the ratio of differential voltage gain to common-mode voltage gain and is generally expressed in dB.*

$$CMRR = 20 \log_{10} \frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common-mode voltage gain. CMRR is a function of frequency and therefore also a function of the impedance balance between the two amplifier input terminals. At even moderate frequencies CMRR can be significantly degraded by small unbalances in the source series resistance and shunt capacitance.

Other Amplifier Types

There are several other special amplifiers which are useful in conditioning the input signal in a data acquisition system. An *isolation amplifier* is used to amplify a differential signal which is superimposed on a very high common-mode voltage, perhaps several hundred or even several thousand volts. The isolation amplifier has the characteristics of an instrumentation amplifier with a very high common-mode input voltage capability.

Another special amplifier, the *chopper stabilized amplifier*, is used to accurately amplify microvolt level signals to the required amplitude. This amplifier employs a special switching stabilizer which gives extremely low input offset voltage drift. Another useful device, the *electrometer amplifier*, has ultra-low input bias currents, generally less than one picoampere and is used to convert extremely small signal currents into a high level voltage.

Settling Time

A parameter that is specified frequently in data acquisition and distribution systems is *settling time*. The term settling time originates in control theory but is now commonly applied to amplifiers, multiplexers, and D/A converters.

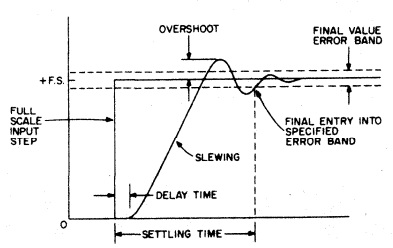


Figure 3. Amplifier Settling Time

Settling time is defined as *the time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value*. The method of application of the input step may vary depending on the type of circuit, but the definition still holds. In the case of a D/A converter, for example, the step is applied by changing the digital input code whereas in the case of an amplifier the input signal itself is a step change.

The importance of settling time in a data acquisition system is that certain analog operations must be performed in sequence, and one operation may have to be accurately settled before the next operation can be initiated. Thus a buffer amplifier preceding an A/D converter must have accurately settled before the conversion can be initiated.

Settling time for an amplifier is illustrated in Figure 3. After application of a full scale step input there is a small delay time following which the amplifier output slews, or changes at its maximum rate. *Slew rate* is determined by internal amplifier currents which must charge internal capacitances.

As the amplifier output approaches final value, it may first overshoot and then reverse and undershoot this value before finally entering and remaining within the specified error band. Note that settling time is measured to the point at which the amplifier output *enters* and *remains* within the error band. This error band in most devices is specified to either ±0.1% or ±0.01% of the full scale transition.

Amplifier Characteristics

Settling time, unfortunately, is not readily predictable from other amplifier parameters such as bandwidth, slew rate, or overload recovery time, although it depends on all of these. It is also dependent on the shape of the amplifier open loop gain characteristic, its input and output capacitance, and the dielectric absorption of any internal capacitances. An amplifier must be specifically designed for optimized settling time, and settling time is a parameter that must be determined by testing.

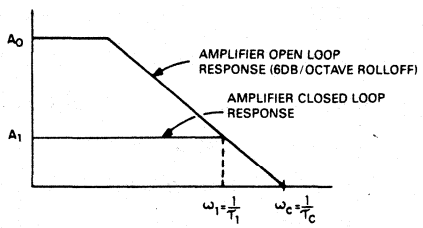


Figure 4. Amplifier Single-Pole Open Loop Gain Characteristic

One of the important requirements of a fast settling amplifier is that it have a single-pole open loop gain characteristic, i.e., one that has a smooth 6 dB per octave gain roll-off characteristic to beyond the unity gain crossover frequency. Such a desirable characteristic is shown in Figure 4.

It is important to note that an amplifier with a single-pole response can never settle faster than the time indicated by the number of closed loop time constants to the given accuracy. Figure 5 shows output error as a function of the number of time constants τ where

$$\tau = \frac{1}{\omega} = \frac{1}{2\pi f}$$

and f is the closed loop 3 dB bandwidth of the amplifier.

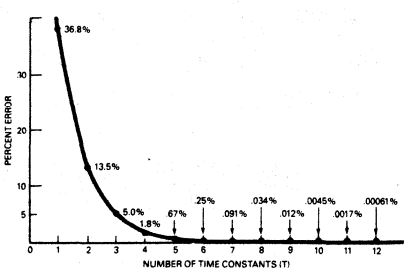


Figure 5. Output Settling Error as a Function of Number of Time Constants

Actual settling time for a good quality amplifier may be significantly longer than that indicated by the number of closed loop time constants due to slew rate limitation and overload recovery time. For example, an amplifier with a closed loop bandwidth of 1 MHz has a time constant of 160 nsec. which indicates a settling time of 1.44 μsec. (9 time constants) to 0.01% of final value. If the slew rate of this amplifier is 1V/μsec., it will take more than 10 μsec. to settle to 0.01% for a 10V change.

If the amplifier has a nonuniform gain roll-off characteristic, then its settling time may have one of two undesirable qualities. First, the output may reach the vicinity of the error band quickly but then take a long time to actually enter it; second, it may overshoot the error band and then oscillate back and forth through it before finally entering and remaining inside it.

Modern fast settling operational amplifiers come in many different types including modular, hybrid, and monolithic amplifiers. Such amplifiers have settling times to 0.1% or 0.01% of 2 μsec. down to 100 nsec. and are useful in many data acquisition and conversion applications.

Glossary of Operational-Amplifier Terms

BANDWIDTH: The frequency at which the gain of an amplifier or other circuit is reduced by 3 dB from its DC value; also the range of frequencies within which the attenuation is less than 3 dB from the center frequency value.

BUFFER AMPLIFIER: An amplifier employed to isolate the loading effect of one circuit from another.

CHOPPER-STABILIZED AMPLIFIER: An operational amplifier which employs a special DC modulator-demodulator circuit to reduce input offset voltage drift to an extremely low value.

COMMON-MODE REJECTION RATIO: For an amplifier, the ratio of differential voltage gain to common-mode voltage gain, generally expressed in dB.

$$\text{CMRR} = 20 \log_{10} \frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common mode voltage gain.

COMMON-MODE VOLTAGE RANGE: The range of voltages on the input terminals for which the amplifier is operational.

DATA AMPLIFIER: See *Instrumentation Amplifier.*

ELECTROMETER AMPLIFIER: An amplifier characterized by ultra-low input bias current and input noise which is used to measure currents in the picoampere region and lower.

FULL POWER FREQUENCY: The maximum frequency at which an amplifier, or other device, can deliver rated peak-to-peak output voltage into rated load at a specified distortion level.

GAIN-BANDWIDTH PRODUCT: The product of gain and small signal bandwidth for an operational amplifier or other circuit. This product is constant for a single-pole response.

INPUT BIAS CURRENT: The average of the two input currents at zero output voltage.

INPUT CAPACITANCE: The capacitance looking into either input terminal with the other grounded.

INPUT DYNAMIC RANGE: In an amplifier, the maximum permissible peak-to-peak voltage across the input terminals which does not cause the output to slew rate limit or distort. Mathematically it is found as

$$\text{IDR (Input Dynamic Range)} \frac{\text{SR}}{\pi \text{GB}}$$

where SR is the slew rate and GB is gain bandwidth.

INPUT NOISE CURRENT: The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT NOISE VOLTAGE: The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

INPUT OFFSET CURRENT: The difference in the currents into the two input terminals with the output at zero volts.

INPUT OFFSET CURRENT DRIFT: The ratio of the change in the offset current to the change in temperature producing it.

INPUT OFFSET VOLTAGE: That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET VOLTAGE DRIFT: The ratio of the change in the offset voltage to the change in temperature producing it.

INPUT RESISTANCE: The resistance looking into either input terminal with the other grounded.

INPUT RESISTANCE, COMMON MODE: The resistance looking into both inputs, with inputs tied together.

INPUT RESISTANCE, DIFFERENTIAL: The value of resistance between two ungrounded inputs.

INPUT VOLTAGE RANGE: The range of voltages on the input terminals for which the amplifier operates within specifications.

INSTRUMENTATION AMPLIFIER: An amplifier circuit with high impedance differential inputs and high common-mode rejection. Gain is set by one or two resistors which do not connect to the input terminals.

ISOLATION AMPLIFIER: An amplifier which is electrically isolated between input and output in order to be able to amplify a differential signal superimposed on a high common-mode voltage.

LARGE-SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

LONG TERM STABILITY: The variation in data converter accuracy due to time change alone. It is commonly specified in percent per 1000 hours or per year.

NORMAL-MODE REJECTION: The attenuation of a specific frequency or band of frequencies appearing directly across two electrical terminals.

OUTPUT CURRENT: The output current available from the amplifier at some specified output voltage.

OUTPUT IMPEDANCE: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_I).

OUTPUT RESISTANCE: The small signal resistance seen at the output with the output voltage near zero.

OUTPUT SHORT CIRCUIT CURRENT: The maximum output current available from the amplifier with the output shorted to ground (for other specified potential).

OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

PROGRAMMABLE GAIN AMPLIFIER: An amplifier with a digitally controlled gain for use in data acquisition systems.

RISE TIME: The time required for an output voltage step to change from 10% to 90% of its final value.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value.

SLEW RATE: The maximum rate of change of the output of an operational amplifier or other circuit. Slew rate is limited by internal charging currents and capacitances and is generally expressed in volts per microsecond.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier with no load and the output at zero volts.

TRANSIENT RESPONSE: The closed loop step-function response of the amplifier under small-signal conditions.

UNITY GAIN BANDWIDTH: The frequency range from D.C. to that frequency where the amplifier open loop gain is unity.

Quick selection: High-performance op amps

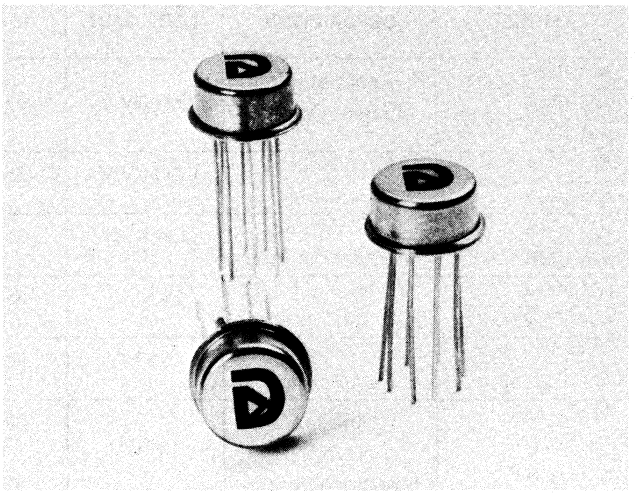
	MODEL	DESCRIPTION	DC OPEN LOOP GAIN	SETTLING TIME 10V to 0.1%	SLEW RATE	GAIN BANDWIDTH	INPUT OFFSET VOLTAGE, MAX.
	AM-101A AM-101B	Optimized for Capacitive Loads	300 KV/V	1.0 μs	45 V/μS	5.5 MHz	Adj to Zero
	AM-303A AM-303B	Modular, High Voltage Op Amp	10^6 V/V	2.5 μs	100 V/μs	10 MHz	± 1 mV
	AM-410-2C	Wideband, JFET Input, Compensated	100 KV/V	2.0 μs	8 V/μs	18 MHz	± 1.5 mV
	AM-410-2M		150 KV/V	1.7 μs			± 1.0 mV
	AM-411-2C	Wideband, JFET Input, Uncompensated	100 KV/V	1.0 μs	40 V/μs	50 MHz	± 1.5 mV
	AM-411-2M		150 KV/V	0.85 μs	50 V/μs	60 MHz	± 1.0 mV
NEW	AM-427-1A	Low-Cost Instrumentation Grade Amplifier	6.3×10^5 V/V		1.7 V/μs	5 MHz	100 μV
NEW	AM-427-1B		10^6 V/V				25 μV
NEW	AM-427-1M		6.3×10^5 V/V				100 μV
NEW	AM-427-2A	Low-Cost Instrumentation Grade Amplifier	6.3×10^5 V/V		1.7 V/μs	5 MHz	100 μV
NEW	AM-427-2B		10^6 V/V				25 μV
NEW	AM-427-2M		6.3×10^5 V/V				100 μV
NEW	AM-430A	Ultra Low Drift, Chopperless Op Amp	100 KV/V	11 μs	0.5 V/μs	2.5 MHz	± 75 μV
NEW	AM-430B						± 25 μV
NEW	AM-430M						± 75 μV
	AM-453-2C	Low Noise, Wideband Op Amp	100 KV/V	- - -	13 V/μs	10 MHz	± 4 mV
	AM-453-2M						
	AM-460-2C	Wideband, Fast Settling Op Amp	150 KV/V	1.5 μs	7 V/μs	12 MHz	± 3 mV
	AM-460-2M						
	AM-462-1	Wideband Fast Settling	150 KV/V	1.0 μs	35 V/μs	100 MHz	± 3 mV
	AM-462-1M						
	AM-462-2		150 KV/V	1.0 μs	35 V/μs	100 MHz	± 3 mV
	AM-462-2M						
	AM-464-2	High Voltage Output	100 KV/V	- - -	5 V/μs	4 MHz	± 6 mV
	AM-464-2M						± 4 mV
	AM-470-2C	Low power, High Performance	300 KV/V	- - -	20 V/μs	1.0 MHz	± 5 mV
	AM-470-2M						± 3 mV
	AM-490-2A	Ultra Low Drift Chopper Stabilized	5×10^8 V/V	- - -	2.5 V/μs	3 MHz	± 20 μV
	AM-490-2B						
	AM-490-2C						
	AM-490-2M						
NEW	AM-7650-1	Low-Cost Chopper Stabilized	10^6V/V	- - -	2.5 V/μs	2 MHz	± 5 μV
NEW	AM-7650-2						

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

These high-performance, modular and monolithic operational amplifiers are a good choice for innumerable applications involving low-level signal conditioning, instrumentation and control circuits, portable and remote instrumentation, A/D input buffering and D/A output amplification.

The AM-427 is a low-cost instrumentation grade amplifier that combines ultra-low noise operation with exceptional D.C. Performance. Significant features include a typical input noise voltage density of 3.5 nv$\sqrt{Hz}$ and a input noise current density as low as 0.4pA $\sqrt{Hz}$.

The new AM-430 is an ultra-low drift, chopperless, operational amplifier. It is specifically designed for accurate, low-level signal applications where low noise, low drift, and precise closed-loop gain are required.



INPUT OFFSET VOLTAGE DRIFT	OUTPUT	COMMON MODE REJECTION	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
40 μV/°C	± 10V @ ± 20 mA	93 dB	1.12 × 1.12 × 0.4 in (28.4 × 28.4 × 10 mm)	Module	0 to + 70	—
20 μV/°C						
50 μV/°C	± 140 V @ ± 25 mA	100 dB	1.8 × 2.4 × 0.61 in (45.7 × 61 × 15.4 mm)	Module	0 to + 70	—
20 μV/°C						
15 μV/°C	± 11V @ ± 8 mA	80 dB	8-pin TO-99	Monolithic	0 to + 70	302
5 μV/°C	± 12V @ ± 10 mA				− 55 to + 125	
15 μV/°C	± 11V @ ± 8 mA	80 dB	8-pin TO-99	Monolithic	0 to + 70	
5 μV/°C	± 12V @ ± 10 mA				− 55 to + 125	
1.8 μV/°C	± 11V @ ± 18 mA	100 dB	8-pin DIP	Monolithic	0 to + 70	306
0.6 μV/°C		114 dB			0 to + 70	
1.8 μV/°C		100 dB			− 55 to + 125	
1.8 μV/°C	± 11V @ ± 18 mA	100 dB	8-pin TO-99	Monolithic	0 to + 70	
0.6 μV/°C		114 dB			0 to + 70	
1.8 μV/°C		100 dB			− 55 to + 125	
1.3 μV/°C	± 10V @ ± 25 mA	100 dB	8-pin TO-99	Monolithic	0 to + 70	310
0.6 μV/°C						
1.3 μV/°C					− 55 to + 125	
30 μV/°C	± 12V @ ± 20 mA	80 dB	8-pin TO-99	Monolithic	0 to + 70	316
					− 55 to + 125	
10 μV/°C	± 10V @ ± 10 mA	74 dB	8-pin TO-99	Monolithic	0 to + 70	312
					− 55 to + 125	
15 μV/°C	± 10V @ ± 10 mA	74 dB	14-pin DIP	Monolithic	0 to + 70	
					− 55 to + 125	
15 μV/°C	± 10V @ ± 10 mA	74 dB	8-pin TO-99	Monolithic	0 to + 70	
					− 55 to + 125	
15 μV/°C	± 35V @ ± 10 mA	74 dB	8-pin TO-99	Monolithic	0 to + 70	316
	± 35V @ ± 12 mA	80 dB			− 55 to + 125	
5 μV/°C	± 12V @ ± 10 mA	80 dB	8-pin TO-99	Monolithic	0 to + 70	—
					− 55 to + 125	
1.0 μV/°C	± 10V @ ± 7 mA	120 dB	8-pin TO-99	Monolithic	0 to + 70	—
0.3 μV/°C						
0.1 μV/°C						
0.6 μV/°C					− 55 to + 125	
0.05 μV/°C	± 4.7V	120 dB	14-pin DIP	Monolithic	0 to + 70	300
			8-pin TO-99			

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

Quick selection: High-speed op amps

	MODEL	DESCRIPTION	DC OPEN LOOP GAIN	SETTLING TIME to 0.1%	SLEW RATE	GAIN BANDWIDTH	INPUT OFFSET VOLTAGE, MAX.	INPUT OFFSET VOLTAGE DRIFT
	AM-100A	Fast Settling Modular Op Amp	300 KV/V	550 ns	45 V/μs	13.5 MHz	Adj to Zero	50 μV/°C
	AM-100B							25 μV/°C
	AM-100C							10 μV/°C
	AM-102A	Fast Settling Follower	103 KV/V	550 ns	140 V/μs	32 MHz	Adj to Zero	40 μV/°C
	AM-102B							20 μV/°C
	AM-103A	Fast Settling Modular Op Amp	130 KV/V	350 ns	400 V/μs	32 MHz	Adj to Zero	40 μV/°C
	AM-103B							20 μV/°C
	AM-450-2	Wideband Fast Settling Op Amp	25 KV/V	330 ns	30V/μs	12 MHz	±4 mV	20 μV/°C
	AM-450-2M							
	AM-452-2	Wideband Fast Settling	15 KV/V	200 ns	120 Vμs	20 MHz	±5 mV	30 μV/°C
	AM-452-2M							
	AM-500GC	Ultra-fast Hybrid Inverting Op Amp	10^6 V/V	200 ns to 0.01%	1000 V/μs	100 MHz	+3 mV	5 μV/°C
	AM-500MC							7 μV/°C
	AM-500MR							10 μV/°C
	AM-500MM							
NEW	AM-1435-MC	Ultra-fast Settling Wideband Hybrid Op Amp	10^5 V/V	70 ns to 0.01%	300 V/μs	1000 MHz	±5 mV	5μV/°C
NEW	AM-1435MR							
NEW	AM-1435MM							

Quick selection: Instrumentation

	MODEL	DESCRIPTION	GAIN RANGE	GAIN NON-LINEARITY	SETTLING TIME	INPUT IM-PEDANCE	INPUT OFFSET VOLTAGE, MAX.
	AM-201A	High Performance Module	1 to 1000	0.01%	20 μs	10^9 Ω	Adj to Zero
	AM-201B						
	AM-201C						
	AM-542MC	High Performance Hybrid Digitally Selectable Gain Ranges	1 to 1024	0.005%	150 μs	10^9 Ω	±50 μV
	AM-542MR						
	AM-542MM						
	AM-543MC		1 to 128	0.01%	6 μs	10^{12} Ω	±50 μV
	AM-543MR						
	AM-543MM						
NEW	AM-551MC	Low Cost, High Performance Hybrid	1 to 1000	0.01%	2 μs	10^{12} Ω	±1 mV × G
NEW	AM-551MR						
NEW	AM-551MM						

Quick selection:

	MODEL	DESCRIPTION	ISOLATION VOLTAGE	GAIN RANGE	GAIN NON-LINEARITY	INPUT RESISTANCE
NEW	AM-227	Low-Cost Precision Isolation Amplifier	±1000 VDC	10 to 1000	±0.005%	100 MΩ
NEW	SCM-100A	Low-Cost, Four Channel Isolation Amplifier	±1000 VDC	1 to 1000	±0.03%	100 MΩ
NEW	SCM-100B					
NEW	SCM-101				±0.02%	
NEW	SCM-102	4-chan RTD condition	±1000 VDC	166.6 V/V or 50 V/V	±0.01%	100 MΩ
NEW	SCM-103	4-chan Strain gage cond.				

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OUTPUT	COMMON MODE REJECTION	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE TEMPERATURE RANGE (°C)	SEE PAGE
± 10V @ ± 20 mA	70 dB	1.12 x 1.12 x 0.4 in (28.4 x 28.4 x 10 mm)	Module	0 to + 70	—
± 10V @ ± 20 mA	93 dB	1.12 x 1.12 x 0.4 in (28.4 x 28.4 x 10 mm)	Module	0 to + 70	—
± 10V @ ± 20 mA	70 dB	1.12 x 1.12 x 0.4 in (28.4 x 28.4 x 10 mm)	Module	0 to + 70	—
± 10V @ ± 10 mA	74 dB	8 pin TO-99	Monolithic	0 to + 70 – 55 to + 125	—
± 10V @ ± 10 mA	74 dB	8-pin TO-99	Monolithic	0 to + 70 – 55 to + 125	—
± 10V @ ± 50 mA		14-pin DIP	Hybrid	0 to + 70 – 25 to + 85 – 55 to + 125	320
± 7V @ ± 14 mA	100 dB	14-pin DIP	Hybrid	0 to + 70 – 25 to + 85 – 55 to + 125	322

amplifiers

INPUT OFFSET VOLTAGE DRIFT	OUTPUT	COMMON MODE REJECTION	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
± 1.0 μV/°C	± 10V @ ± 5 mA	100 dB	1.5 × 1.5 × 0.375 in (38.1 × 38.1 × 9.5 mm)	Module	0 to + 70	—
± 0.5 μV/°C		106 dB				
± 0.25 μV/°C		114 dB				
1 μV/°C	± 10.5V @ ± 5 mA	86 dB	24-pin DIP	Hybrid	0 to + 70 – 25 to + 85 – 55 to + 125	324
5 μV/°C						
10 μV/°C						
30 μV/G + 30 μV/°C	± 11V @ ± 1 mA	86 dB	24-pin DIP	Hybrid	0 to + 70 – 25 to + 85 – 55 to + 125	
35 μV/G + 30 μV/°C						
40 μV/G + 30 μV/°C						
15 μV/°C	± 11V @ ± 5 mA	100 dB	16-pin DIP	Hybrid	0 to + 70 – 25 to + 85 – 55 to + 125	328

Isolation amplifiers

COMMON MODE REJECTION	INPUT OFFSET VOLTAGE	OUTPUT	PACKAGE	TECHNOLOGY	OPERATING TEMPERATURE RANGE	SEE PAGE
176 dB	± 150 μv	± 10V @ ± 5 mA	1.2 × 2.8 × 0.375 in (30 × 70 × 4.5 mm)	Module	0 to + 70	330
156 dB	± 20 μV	± 5V @ ± 5 mA	2 × 4 × 0.4 in (50.8 × 101.6 × 10.2 mm)	Module	0 to + 70	332
145 dB	± 50 μV					
94 dB	± 150 μV	± 5V @ 1 mA ± 5V @ 5 mA	2 × 4 × 0.4 in (50.8 × 101.6 × 10.2 mm)	Module	0 to + 70	336

NEW

DATEL

Low Cost Chopper Stabilized Op. Amp., AM-7650

FEATURES

- ±5 μV Max. Input Offset
- .05 μV/°C Max. Offset Drift
- Low Cost
- 120 dB Min. CMRR
- 10 pA Max. Input Bias

GENERAL DESCRIPTION

The AM-7650 is a low cost, monolithic chopper stabilized operational amplifier fabricated using CMOS technology. The amplifier consists of a main d.c. amplifier, nulling amplifier, output clamp, compensation circuit, and switches controlled by a two-phase oscillator. The extremely low offset voltage drift, 0.05 μV/°C maximum, and the initial input offset voltage of only ±5 μV maximum eliminate the requirement for external zero adjustment in most applications.

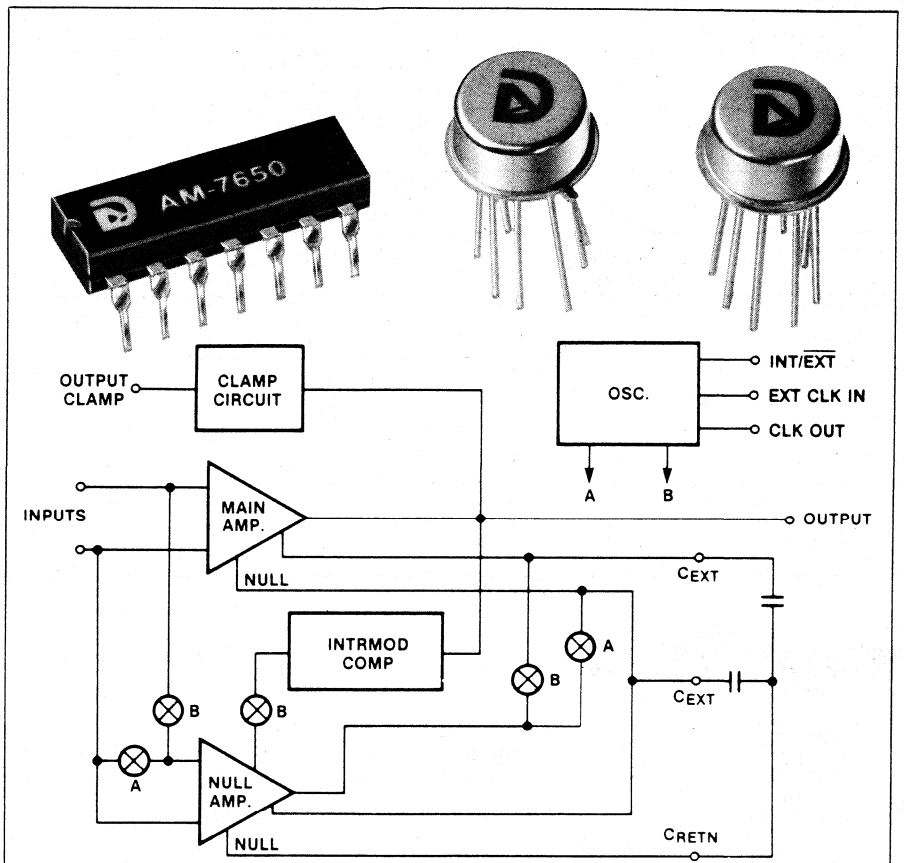
The amplifier achieves its low offset by comparing the input voltages to a nulling amplifier that spends alternate clock phases nulling itself and the main amplifier. Two external capacitors, the only external components necessary, are required to store the correcting potentials on the two amplifier nulling inputs. The compensation circuit minimizes the intermodulation between the applied signal and the chopping frequency. The output clamp circuit reduces the over-load recovery time of the amplifier.

Besides providing virtually glitch-free output and very fast recovery from overloads, the AM-7650 offers differential inputs, maximum input bias current of 10 pA, input noise voltage of only 2 μV P-P, and an input resistance of $10^{12}\Omega$. Unity gain bandwidth product is 2 MHz, CMRR is 120 dB minimum and the open loop gain is a minimum of 120 dB. Long term stability is typically 100 nV/$\sqrt{\text{mnth}}$.

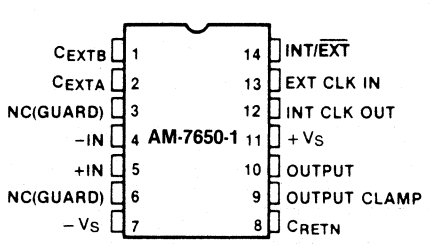
The clock oscillator and all the other circuitry is entirely self-contained, however, the AM-7650-1 includes a provision for the use of an external clock, if required for a particular application. In addition, the AM-7650 is internally compensated for unity gain operation.

Any application where system performance can be significantly improved by a reduction in input offset voltage and bias current is right for the AM-7650. These applications would include inverting or noninverting amplifier configurations, strain gauge pre-amplifiers, nulling amplifiers, and low offset comparator circuits.

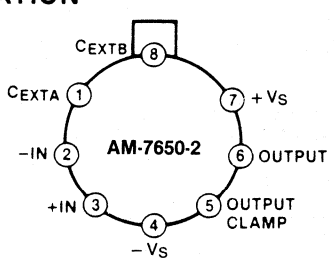
The AM-7650-1 is packaged in a 14 pin DIP and the AM-7650-2 is packaged in a 8 lead, hermetically sealed TO-99 case. Models are available in the 0 to +70°C operating temperature range.



PIN CONFIGURATION



14 PIN DIP



8 PIN TO-99

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PACKAGE	PRICE (1-24)
AM-7650-1	0 to +70°C	Plastic DIP	
AM-7650-2	0 to +70°C	TO-99	

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-7650
Typical at 25°C, ± 5V supplies unless otherwise noted

	AM-7650-1	AM-7650-2
MAXIMUM RATINGS		
Power Supply Voltage (+ V_S to − V_S)	18V	
Input Voltage	(+ V_S + 0.3) to (− V_S − 0.3)	
Lead Temperature (soldering, 10 sec)	300°C	
Oscillator Control Voltage (Pins 12, 14)[1]	± V_S	
Current into any Pin	10 mA	
Current into any Pin while operating[2]	100 μA	
Total Power Dissipation	375 mW	250 mW
INPUT CHARACTERISTICS		
Input Resistance	$10^{12}\Omega$	
Input Offset Voltage, max.[3]	± 5 μV	
Input Bias Current, max.[4]	10 pA	
Input Offset Current	0.5 pA	
OUTPUT CHARACTERISTICS		
Output Voltage Swing, min.[5]	± 4.7V	
Output Short Circuit Duration	Indefinite	
PERFORMANCE		
Large Signal Voltage Gain, min.[6]	10^6V/V	
Input Offset Voltage Drift, max.	0.05 μV/°C	
Long Term Stability	100 nV/$\sqrt{\text{month}}$	
Common Mode Voltage Range, min.	− 5.0V	
max.	+ 1.5V	
Common Mode Rejection Ratio, min.	120 dB	
Power Supply Rejection Ratio, min.	120 dB	
Input Noise Voltage[7]	2 μV P-P	
Input Noise Current, 10 Hz	0.01 pA/Hz	
Unity Gain Bandwidth	2.0 MHz	
Slew Rate[8]	2.5V/μS	
Rise Time	0.2 μS	
Overshoot	20%	
Internal Chopping frequency,[9] min.	120 Hz	
max.	375 Hz	
Clamp ON Current[10], min.	25 μA	
max.	200 μA	
Clamp OFF Current[10]	1 pA	
POWER REQUIREMENT		
Power Supply Range (+ V_S to − V_S), min.	4.5V	
max.	16V	
Power Supply Current (no load), max.	3.5 mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to + 70°C	
Storage Temperature Range	− 55°C to + 150°C	
Package	14 Pin Plastic DIP	8 Pin TO-99

NOTES:

1. AM-7650-1 only. Voltage on EXT CLOCK IN = (+ V_S − 6.0V)
2. Limiting input current to 100 μA is recommended to avoid latch-up problems. Typically 1 mA is safe, however, it is not guaranteed.
3. Specified at 25°C. Typically ± 1.0 μV over temperature (0°C to + 70°C).
4. Specified at 25°C. Typically 35 pA over temperature (0°C to + 70°C). Doubles every 10°C.
5. OUTPUT CLAMP not connected. R_L = 10 kΩ. With R_L = 100kΩ, the output voltage swing is typically ± 4.95V.
6. R_L = 10 kΩ.
7. R_S = 100Ω. 0 to 10 Hz.
8. C_L = 50 pF, R_L = 10 kΩ.
9. Pins 12 and 14 open (DIP).
10. See Technical Note 2.

TECHNICAL NOTES

1. Null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (for the AM-7650-1) or the − V_S pin (for the AM-7650-2). This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} (or − V_S for TO-99). C_{EXTA} and C_{EXTB} have optimum values which depend on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. If an external clock is used, the value of C_{EXTA} and C_{EXTB} should be scaled approximately in proportion in order to maintain the same relationship between the chopping frequency and the nulling time constant. A high quality film-type capacitor such as mylar is preferred, however, a ceramic or other lower-grade capacitor may be suitable for many applications. For the quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) are recommended.
2. To reduce overload recovery time which is inherent with chopper-stabilized amplifiers, tie the OUTPUT CLAMP to the inverting input pin or summing junction. A current path between this point and the output pin occurs just before the device output saturates. Thus, uncontrolled differential inputs are avoided, along with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.
3. To avoid latch-up, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latch-up, even under fault conditions.
4. All of the AM-7650's inputs are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided as this can cause degraded diode junction characteristics, which may result in increased input-leakage currents.
5. The open loop gain of this amplifier will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the device is used strictly for DC applications, the lower gain is of little consequence since the DC gain of this device is greater than 120 dB with loads down to 1 kΩ.
   For wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or greater. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.
6. Due to thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc., special precautions should be made to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High impedance loads are preferable, and good separation from surrounding heat-dissipation elements is recommended.
7. Care must be taken in the assembly of printed circuit boards to take full advantage of the AM-7650's low input currents. The boards should be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination. Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and the adjacent metal runs. Input guarding of the 8-pin TO-99 package can be accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when the device is inserted into the board. The guard which is a conductive ring surrounding the inputs, is connected to a low impedance point that is approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard. The pin configuration of the 14-pin DIP version is designed to facilitate guarding since the pins adjacent to the inputs are not used.

Wide Bandwidth, FET Input Monolithic Operational Amplifier AM-410 & AM-411 SERIES

FEATURES

- **60 MHz — Gain Bandwidth**
- **50 V/μsec — Slew Rate**
- **850 nsec — Settling to 0.1%**
- **150,000 — Open Loop Gain**
- **5 μV/°C — Input Offset Voltage Drift**
- **$10^{12}\Omega$ — Input Impedance**

GENERAL DESCRIPTION

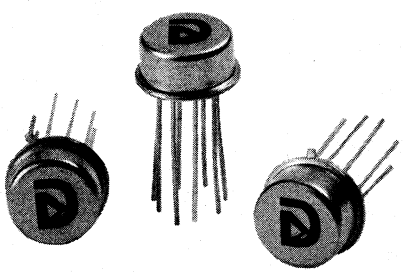
The AM-410 and AM-411 series are monolithic wideband operational amplifiers manufactured with FET/bipolar technology. Active laser trimming of the input stage complements the high frequency capabilities of these amplifiers with excellent input characteristics. Features available on both devices include an input offset voltage of 1 mV maximum with a temperature drift of typically 5 μV/°C, input bias current of 50 pA maximum, and an input impedance of $10^{12}\Omega$. All devices provide a ±11V output at 8 mA, and open loop voltage gain of up to 150,000.

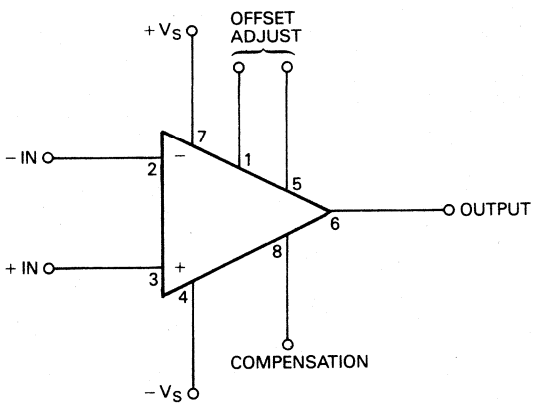
The AM-410 devices are compensated for unity gain operation. The dynamic characteristics of these devices include 10 MHz unity gain bandwidth, 8V/μsec slew rate, and a settling time of 1.7 μsec.

The AM-411 series units are uncompensated devices that are stable at closed loop gains of greater than 10 without external compensation. These units feature dynamic characteristics that include 60 MHz gain bandwidth, 50V/μ slew rate, and a settling time of 850 nsec.

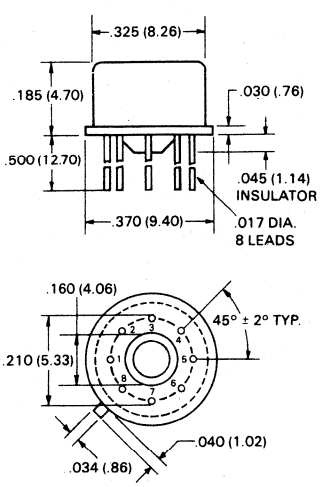
These devices are ideal for use in sample and hold circuits, active filters, A/D input buffering, D/A output amplification and a wide variety of signal conditioning applications.

All models are available in both 0°C to +70°C operating temperature range or −55°C to +125°C for suffix M models. All devices are packaged in a hermetically sealed, 8 pin, TO-99 case.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET ADJUST
2	−INPUT
3	+INPUT
4	−Vs
5	OFFSET ADJUST
6	OUTPUT
7	+Vs
8	BANDWIDTH CONTROL
CASE IS CONNECTED TO -SUPPLY	

DATEL-INTERSIL, INC. 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-410, AM-411

Typical at 25°C, ±15 VDC supplies, unless otherwise noted.

	AM-410-2C	AM-410-2M	AM-411-2C	AM-411-2M
MAXIMUM RATINGS				
Power Supply Voltage	±20VDC			
Differential Input Voltage	40V			
Peak Output Current	Full Short Circuit Protection			
Internal Power Dissipation[1]	300mW			
INPUT CHARACTERISTICS				
Input Offset Voltage, max.[2]	1.5mV	1.0mV	1.5mV	1.0mV
Input Offset Current, max.	50pA	10pA	50pA	10pA
Input Bias Current, max.	100pA	50pA	100pA	50pA
Input Resistance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$
Common Mode Voltage Range, min.	±10V	±10V	±10V	±10V
OUTPUT CHARACTERISTICS				
Output Voltage Swing, min.[3]	±11V	±12V	±11V	±12V
Short Circuit Output Current, min.	±8mA	±10mA	±8mA	±10mA
Output Impedance	40Ω	30Ω	40Ω	30Ω
PERFORMANCE				
D.C. Open Loop Gain[4]	100K V/V	150K V/V	100K V/V	150K V/V
Full Power Bandwidth[5]	125KHz	150KHz	625KHz	625KHz
Gain Bandwidth Product, G=10	18MHz	18MHz	50MHz	60MHz
Slew Rate[6]	8 V/μsec	8 V/μsec	40 V/μsec	50 V/μsec
Rise Time[6]	20 nsec	15 nsec	20 nsec	**20 nsec**
Settling Time,[7] 10V to 0.1%	2.0 μsec	1.7 μsec	1.0 μsec	.85 μsec
Input Offset Voltage Drift	15 μV/c°	5 μV/c°	15 μV/c°	5 μV/c°
Common Mode Rejection Ration	86 dB	86 dB	86 dB	86 dB
Power Supply Rejection Ratio	86 dB	86 dB	94 dB	94 dB
POWER REQUIREMENTS				
Voltage, Rated Performance	±15VDC			
Operating Voltage Range	±5VDC to ±20VDC			
Supply Current, max.				
Suffix — 2C	8mA			
Suffix — 2M	7mA			
PHYSICAL ENVIRONMENT				
Operating Temperature Range				
Suffix — 2C	0°C to +70°C			
Suffix — 2M	-55°C to +125°C			
Storage Temperature Range	-65°C to +150°C			
Package, Hermetically Sealed	TO -99			

NOTES:

1. Derate by 6.8 mW/°C for operation at ambient temperatures above +75°C.
2. 2mV max. at full operating temperature for devices with a -2M suffix. 3.5 mV max. for devices with a -2C suffix.
3. R_L = 10KΩ.
4. Vout = ±10V, R_L =2KΩ.
5. R_L = 2KΩ.
6. G = 10 for AM-411, G = 1 for AM-410.
7. G = -10 for AM-411, G = -1 for AM-410.
8. At full operating temperature, Vsupp. = ±10VDC to ±20VDC.

TECHNICAL NOTES

1. It is recommended that these amplifiers be operated with power supply lines decoupled to ground with .01μF ceramic capacitors. Decoupling capacitors should be located as close to the amplifier power pins as possible.
2. Input offset voltage may be adjusted to zero, if required, by connecting the amplifier as shown in the external offset and bandwidth compensation diagram. The trimming potentiometer used should be 100K cermet type with a temperature coefficient less than 100 ppm/°C (available from Datel-Intersil as part no. TP-100K). It should be noted that adjustment of initial offset voltage may affect the input offset voltage drift tempco.
3. When the AM-410 or AM-411 are used to drive heavy capacitive loads (≥ 100 pF)a small value resistor should be connected in series with the output and inside the feedback loop. Resistance values of approximately 100Ω are suggested.
4. When large values of feedback resistance are used, a small capacitor in parallel with the feedback resistor will neutralize the pole introduced by the input capacitance. Capacitor values of approximately 3 pF should be sufficient to stabilize high feedback resistance configurations.
5. The AM-411 is an uncompensated operational amplifier that is stable at closed loop gains of greater than 10 without external compensation. For stable operation in a unity gain configuration a suggested compensation circuit is given.

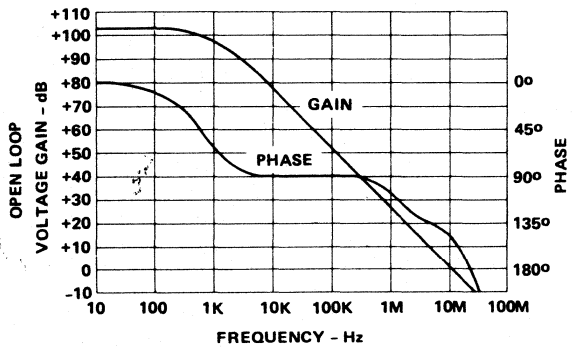
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
AM-410-2C	0°C To +70°C
AM-410-2M	-55°C To +125°C
AM-411-2C	0°C To +70°C
AM-411-2M	-55°C To +125°C

Trimming Potentiometer: TP100K

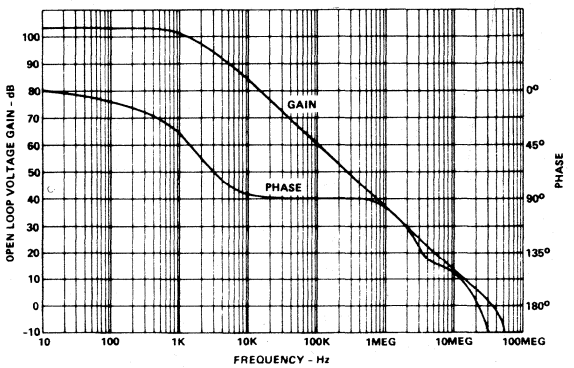
TYPICAL PERFORMANCE CURVES

OPEN LOOP FREQUENCY RESPONSE



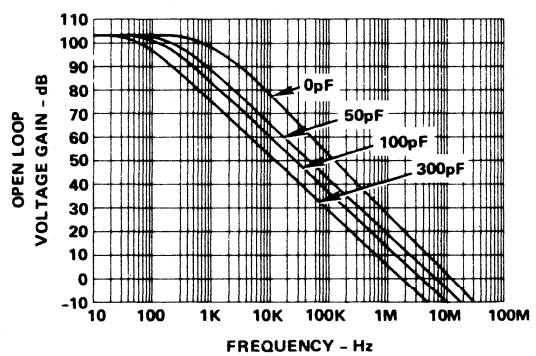
AM-410

OPEN LOOP FREQUENCY RESPONSE



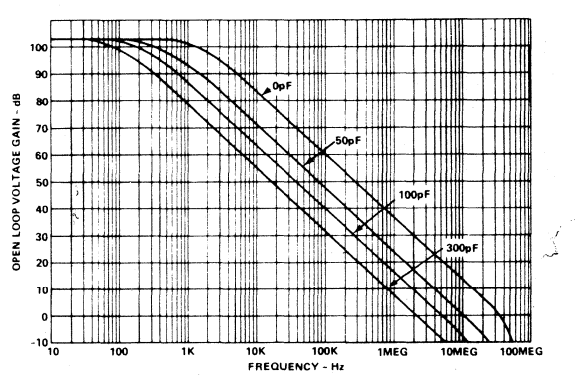
AM-411

OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CAPACITANCES



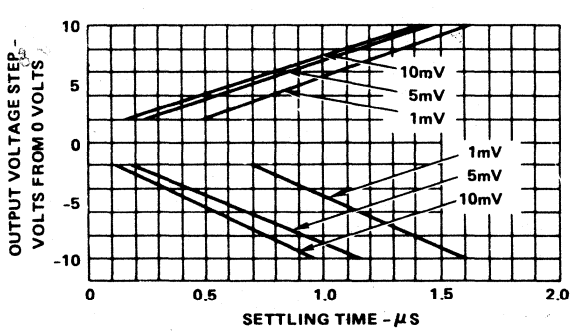
AM-410

OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES



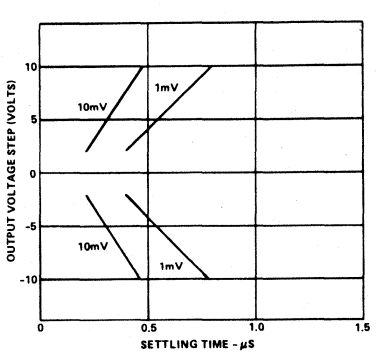
AM-411

SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



AM-410

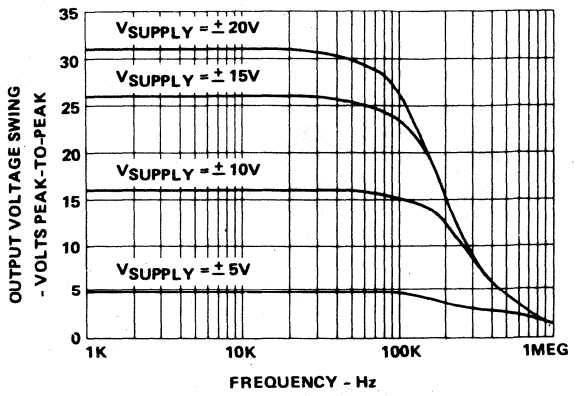
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



AM-411

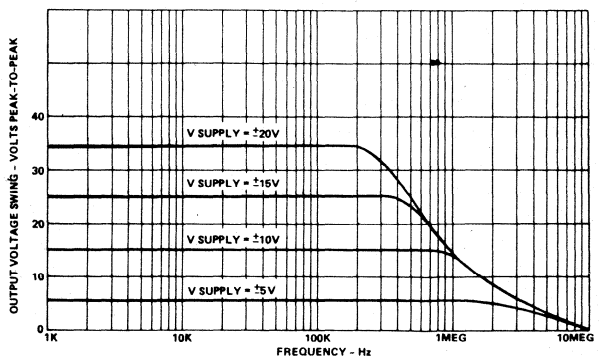
TYPICAL PERFORMANCE CURVES

OUTPUT VOLTAGE SWING VS FREQUENCY



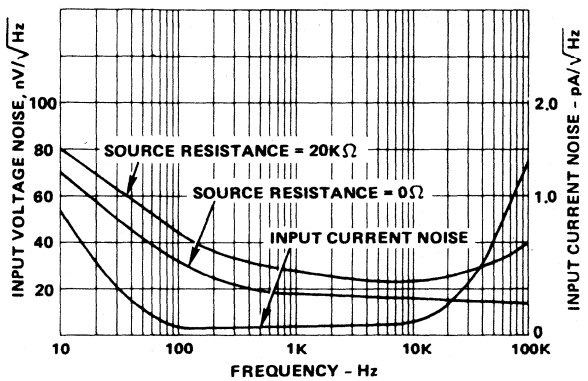
AM-410

OUTPUT VOLTAGE SWING VS FREQUENCY



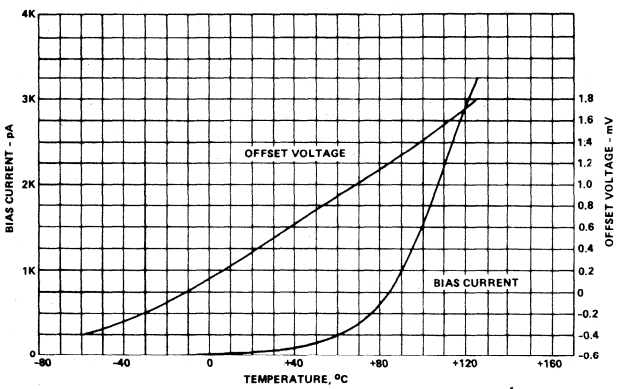
AM-411

INPUT VOLTAGE AND CURRENT NOISE VS FREQUENCY



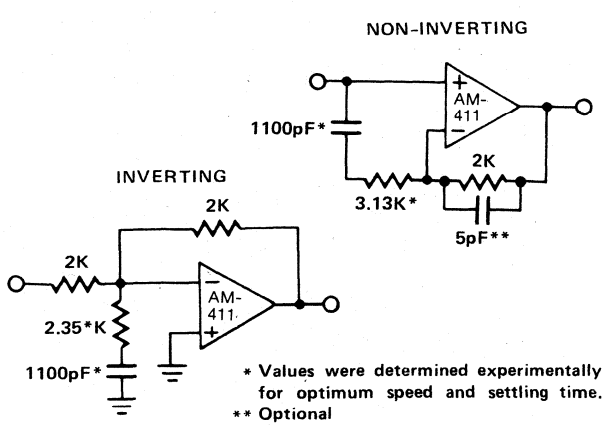
AM-410 AND AM-411

INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



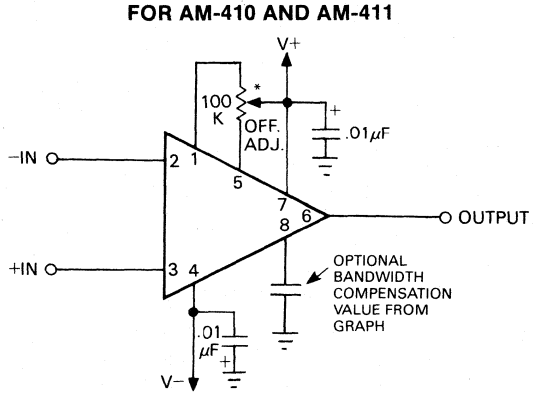
AM-410 AND AM-411

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY ON AM-411



* Values were determined experimentally for optimum speed and settling time.
** Optional

EXTERNAL OFFSET ADJUST AND BANDWIDTH COMPENSATION FOR AM-410 AND AM-411



*AVAILABLE FROM DATEL-INTERSIL PART NO. TP100K

DATEL INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

NEW

DATEL

Ultra Low Noise Operational Amplifier AM-427

FEATURES

- 5.5 nV/√Hz Max. Noise Density
- 0.08 μV P-P Low Frequency Noise
- 25 μV Max. Input Offset Voltage
- ±40 nA Max. Input Offset Current
- 0.6 μV/°C Max. Offset Voltage Drift

GENERAL DESCRIPTION

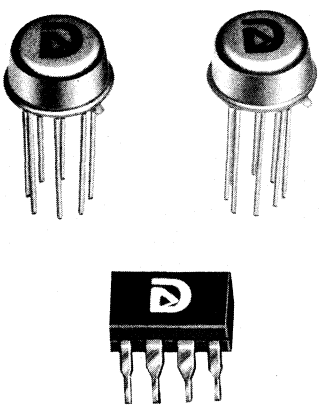
The AM-427 is a low cost monolithic instrumentation grade amplifier that combines ultra-low noise operation with exceptional DC performance. Input noise voltage density is typically 3.5 nV/√Hz at 10 Hz while input noise current density is as low as 0.4 pA/√Hz.

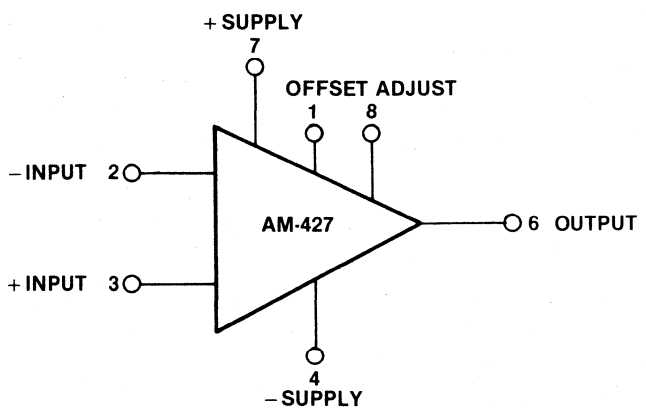
Other significant features include a maximum input offset voltage of 25 μV, eliminating the need for external zeroing in most applications. Maximum input offset voltage drift is only 0.6 μV/°C. The AM-427 is internally compensated to provide a phase margin of 70° in the unity gain mode which eliminates peaking and ringing in low gain feedback applications. Output voltage is typically ±13.5V at ±6.75 mA load current with a short circuit protected output.

Dynamic characteristics include an 8 MHz gain bandwidth product and 2.8V/μS slew rate. Power supply rejection ratio and common mode rejection ratio are both in excess of 120 dB.

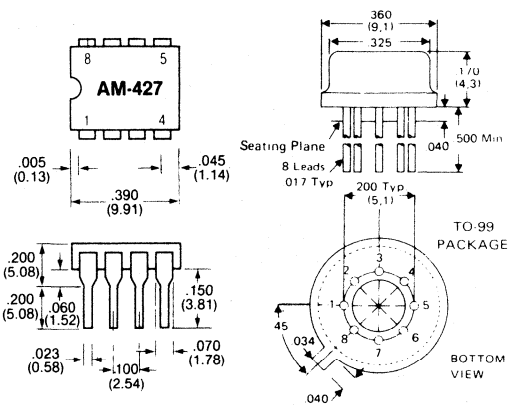
The AM-427 is an ideal choice for applications requiring high accuracy, low drift and low noise performance such as the amplification of low level transducer signals.

The AM-427 is available for operation over the industrial, −25°C to +85°C, and military, −55°C to +125°C temperature ranges. Models are packaged in either an 8 pin, hermetically sealed TO-99 case or an 8 pin ceramic DIP.





MECHANICAL DIMENSIONS INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET VOLTAGE ADJ
2	−INPUT
3	+INPUT
4	−SUPPLY VOLTAGE
5	N.C.
6	OUTPUT
7	+SUPPLY VOLTAGE
8	OFFSET VOLTAGE ADJ.

DATEL-INTERSIL, 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL., (617) 339-9341/ TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-427

Typical at 25 °C, ± 15 VDC supplies, unless otherwise noted.

MAXIMUM RATINGS	A	B	M
Power Supply Voltage		± 22V	
Input Voltage		± 22V	
Differential Input Voltage		± 0.7V	
Power Dissipation		658 mW	
INPUT CHARACTERISTICS			
Input Voltage Range, min.		± 11V	
Input Resistance, diff. mode, min.	0.8 MΩ	1.5 MΩ	0.8 MΩ
Input Offset Voltage, max.	100 μV	25 μV	100 μV
Input Bias Current, max.	± 80 nA	± 40 nA	± 80 nA
Input Offset Current, max.	75 nA	35 nA	75 nA
OUTPUT CHARACTERISTICS			
Output Voltage, min.[1]		± 11V	
Output Current, S.C. protected, min.		± 18 mA	
Output Resistance, open loop[2]		70Ω	
PERFORMANCE			
DC Open Loop Gain, min.[3]	116 dB	120 dB	116 dB
Input Offset Voltage Drift, max.[4]	1.8 μV/ °C	0.6 μV/ °C	1.8 μV/ °C
Long Term Stability	2 μV/mo	1 μV/mo	2 μV/mo
Input Bias Current Drift, max.	± 700 pA/ °C	± 200 pA/ °C	± 700 pA/ °C
Input Offset Current Drift, max.	600 pA/ °C	150 pA/ °C	600 pA/ °C
Common Mode Rejection Ratio, min.[5]	100 dB	114 dB	100 dB
Input Noise Voltage, max., 0.1 to 10 Hz	0.25 μV p-p	0.18 μV p-p	0.25 μV p-p
Input Noise Voltage Density, max., 10 Hz	8 nV/√Hz	5.5 nV/√Hz	8 nV/√Hz
Input Noise Current Density, max., 1 KHz	0.6 pA/√Hz	0.6 pA/√Hz	0.6 pA/√Hz
Power Supply Rejection Ratio, min.	94 dB	100 dB	94 dB
Gain Bandwidth Product, min		5.0 MHz	
Slew Rate, min		1.7V/μS	
POWER REQUIREMENT			
Voltage, Rated Performance		± 15 VDC	
Quiescent Current, max.	± 5.7 mA	± 4.7 mA	± 5.7 mA
Power Dissipation	170 mW	140 mW	170 mW
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range:			
AM-427A,B		− 25 °C to + 85 °C	
AM-427M		− 55 °C to + 125 °C	
Storage Temperature Range		− 65 °C to + 150 °C	
Package, AM-427-1		8 Pin Ceramic DIP	
AM-427-2		8 Pin Hermetically Sealed TO-99	

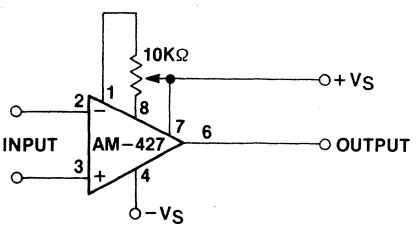
NOTES:

1. RL = 600Ω.
2. Output Voltage = 0, output current = 0.
3. R_L = 2 kΩ, V_{OUTPUT} = ± 10V.
4. Guaranteed unnulled or when nulled with an 8 kΩ to 20 kΩ potentiometer.
5. Common mode voltage = ± 11V.
6. V_S = ± 4V to ± 18V.

TECHNICAL NOTES

1. In order to maintain the specified drift performance, both input pins should be maintained at the same relative temperature. This is to avoid stray thermoelectric voltages which are generated by the dissimilar metals at the contacts of the input terminals.
2. To obtain the best possible linearity, circuit design should call for the minimum output current required by the application to assure high gain performance and excellent linearity, the output current range should be held to a maximum of ± 10mA.
3. The AM-427 provides stable operation with load capacitances of up to 2000 pF and ± 10 volt swings. Larger capacitances should be decoupled with a 50Ω decoupling resistor. To avoid additional phase shifting and phase margin, a 20 pF capacitor should be used in parallel with the feedback resistor when the value of the feedback resistor is greater than 2 kΩ.
4. If adjustment of offset voltage is required, a 10 kΩ trimpot can be used without degrading the offset voltage drift specifications. A 1 kΩ to 1 MΩ trimpot can be used, however, a 0.1 to 0.2 μV/ °C degradation may occur. Trimming to a value other than zero will create a drift of (offset voltage/ 300)μV/ °C. A 10 kΩ offset trimpot will yield an adjustment range of ± 4 mV. A smaller trimpot in conjunction with fixed resistors can be used to obtain a smaller adjustment range with higher sensitivity and resolution.

TYPICAL CONNECTION DIAGRAM

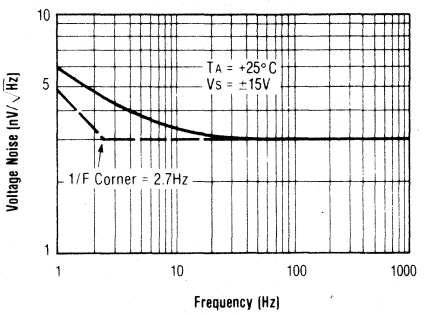


ORDERING INFORMATION

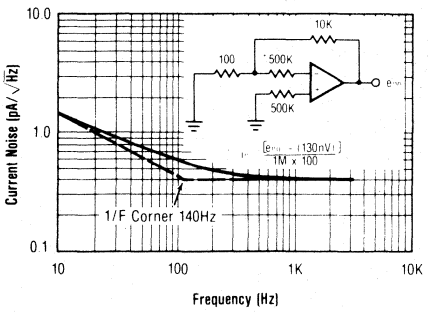
MODEL	PACKAGE	PRICE (1-24)
AM-427-1A	8 Pin Ceramic DIP	
AM-427-1B	8 Pin Ceramic DIP	
AM-427-1M	8 Pin Ceramic DIP	
AM-427-2A	8 Pin TO-99	
AM-427-2B	8 Pin TO-99	
AM-427-2M	8 Pin TO-99	

TYPICAL PERFORMANCE

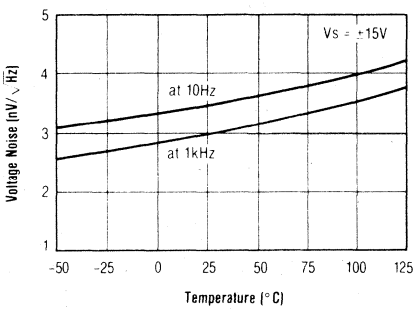
Voltage Noise vs Frequency



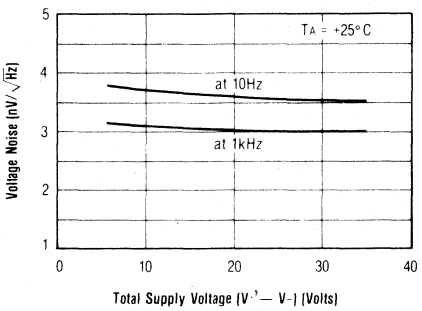
Current Noise vs Frequency



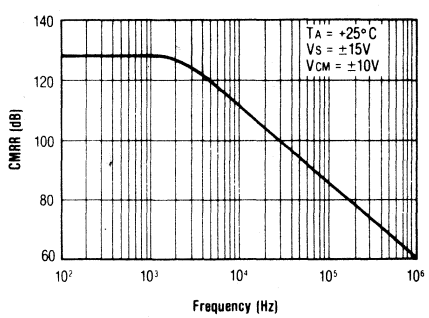
Voltage Noise vs Temperature



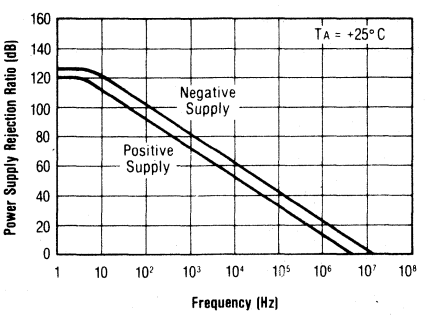
Voltage Noise vs Supply Voltage



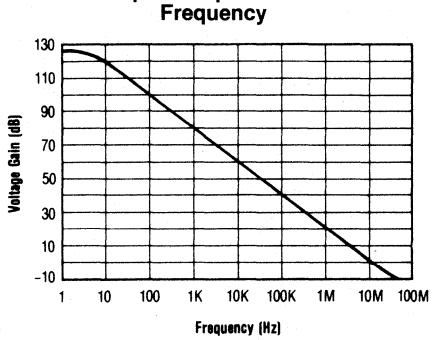
CMRR vs Frequency



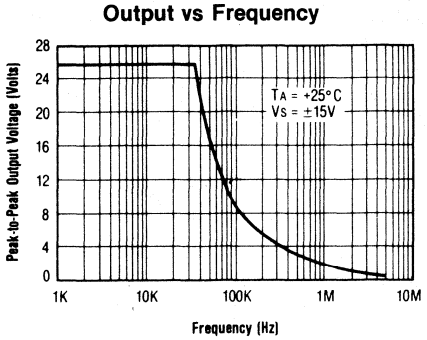
PSRR vs Frequency



Open Loop Gain vs Frequency

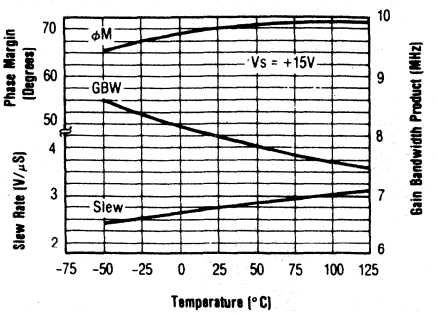


Maximum Undistorted Output vs Frequency

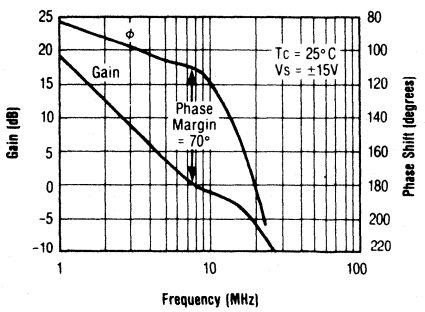


TYPICAL PERFORMANCE AND APPLICATIONS

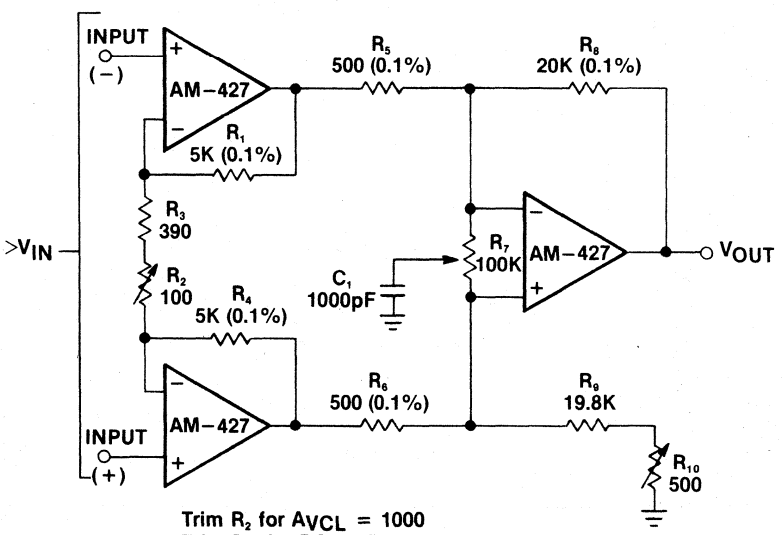
Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature



Gain, Phase Shift vs Frequency



INSTRUMENTATION AMPLIFIER



Trim R_2 for A_{VCL} = 1000
Trim R_{10} for DC CMRR
Trim R_7 for Minimum V_{OUT} at V_{CM} = 20Vp-p, 10kHz

The AM-427 is particularly useful in instrumentation applications. In a single difference amplifier configuration, the AM-427 exhibits excellent common mode rejection and spot noise voltage so low, it is dominated by the resistor Johnson noise.

The three amplifier configuration shown avoids the low input impedance characteristics of difference amplifiers. Because of the additional amplifiers used, the spectral noise voltage will increase from a typical of 3 nV/$\sqrt{Hz}$ to approximately 4.9 nV/$\sqrt{Hz}$. The overall gain of the circuit is set at 1000, and with balanced source resistors, a CMRR of 100 dB is achieved.

NEW

DATEL

Ultra-Low Drift, Monolithic Operational Amplifier AM-430

FEATURES

- 0.6 μV/°C Max. Drift
- 25 μV Max. Input Offset Volt.
- 2.5 MHz Bandwith
- 10^7 Open Loop Gain
- 9 nV / $\sqrt{Hz}$ Voltage Noise
- ±4 nA Max. Bias

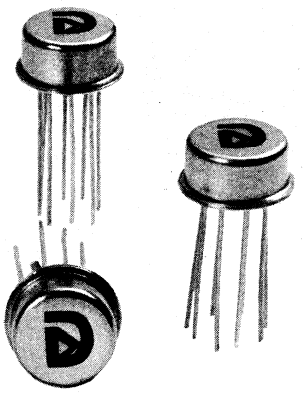
GENERAL DESCRIPTION

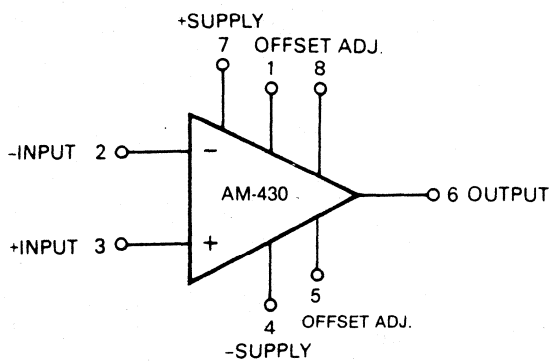
The AM-430 is a chopperless, ultra-low drift monolithic operational amplifier. Excellent input characteristics in conjunction with 2.5 MHz unity gain bandwidth make this amplifier extremely useful for precision integrator, biomedical, and low level signal amplification applications. This amplifier features 25 μV maximum input offset voltage, eliminating the need for external zeroing in most applications, and a maximum input offset voltage drift of only 0.6 μV/°C; specifications that rival those of more expensive chopper stabilized amplifiers.

Other significant features include 10^7open loop voltage gain, 100 dB minimum common mode rejection ratio, and ±4 nA maximum bias current. The AM-430 also has low input noise characteristics of 9 nV / $\sqrt{Hz}$ voltage noise density and 0.2 pA / $\sqrt{Hz}$ current noise density. Output voltage range is ±10V minimum at ±25 mA load current with a short circuit protected output.

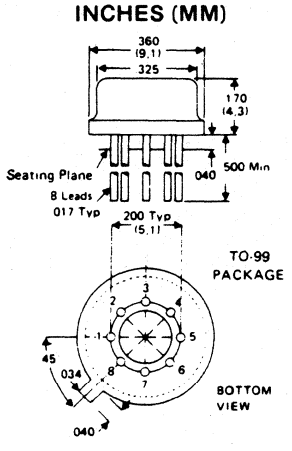
Dynamic characteristics include a settling time of 11 μsec to 0.1%, and a minimum slew rate of 0.5V/μsec. Its unique combination of specifications make the AM-430 ideal for transducer amplification, threshold detector applications, low drift active filters and precision D/A converter output amplifiers.

The AM-430 is available in three versions of which one is a military temperature range model. All models are packaged in a hermetically sealed 8 pin TO-99 case.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE All leads gold plated KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET ADJ.
2	− INPUT
3	+ INPUT
4	− SUPPLY VOLTAGE
5	OFFSET ADJ.*
6	OUTPUT
7	+ SUPPLY VOLTAGE
8	OFFSET ADJ.*

*Pins 5 and 8 are internally connected.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

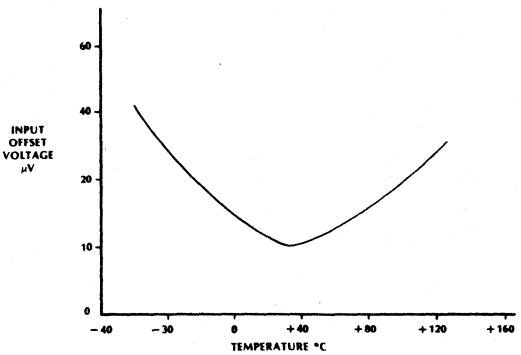
SPECIFICATIONS, AM-430
Typical at +25°C, ±15VDC supplies, unless otherwise noted.

	A	B	M
MAXIMUM RATINGS[1]			
Power Supply Voltage		±20V	
Differential Input Voltage		±15V	
Power Dissipation[2]		300 mW	
INPUT CHARACTERISTICS			
Common Mode Voltage Range, min.[3]		±12V	
Input Resistance, diff. mode		30 MΩ	
Input Offset Voltage, max.	75 μV	25 μV	75 μV
Input Bias Current, max.	±4 nA	±2 nA	±4 nA
Input Offset Current, max.	4 nA	2 nA	4 nA
OUTPUT CHARACTERISTICS			
Output Voltage, min.[4]		±10V	
Output Current, S.C. protected, min.		±25 mA	
Output Resistance, open loop[5]		45Ω	
PERFORMANCE			
DC Open Loop Gain, min.[6]		120 dB	
Input Offset Voltage Drift, max.	1.3 μV/°C	0.6 μV/°C	1.3 μV/°C
Input Bias Current Drift, max.		40 pA/°C	
Input Offset Current Drift, max.		40 pA/°C	
Common Mode Rejection Ratio, min.		100 dB	
Input Noise Voltage Density, 1 kHz		9 nV/√Hz	
Input Noise Current Density, 1 kHz		0.2 pA/√Hz	
Power Supply Rejection Ratio, min.[7]		100 dB	
DYNAMIC CHARACTERISTICS			
Unity Gain Bandwidth		2.5 MHz	
Full Power Frequency		10 kHz	
Slew Rate, min.		0.5 V/μS	
Settling Time, 10V to 0.1%[8]		11 μS	
Rise Time		340 nS	
POWER REQUIREMENT			
Voltage, Rated Performance		±15 VDC	
Quiescent Current, max.[9]		1.3 mA	
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range:			
AM-430A,B		0° to +70°C	
AM-430M		−55°C to +125°C	
Storage Temperature Range		−65°C to +150°C	
Package, Hermetically Sealed		TO-99	

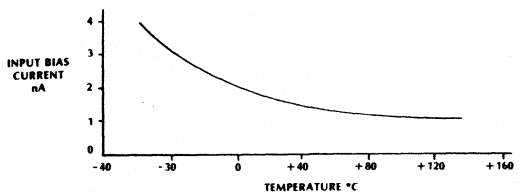
NOTES:
1. Maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at temperatures above +75°C.
3. Specified at full operating temperature.
4. R_L = 600Ω.
5. Measured under open loop conditions, f = 100 Hz.
6. Vout = ±10V, R_L = 2kΩ.
7. Vsupp = ±5 VDC to ±20 VDC. Specified at full operating temperature.
8. G = −1.
9. Specified at full operating temperature.

PERFORMANCE

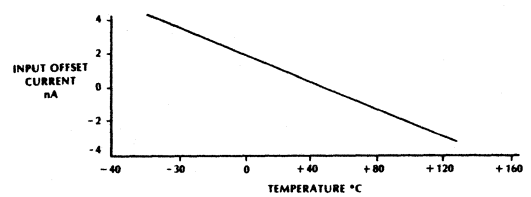
TYPICAL INPUT OFFSET VOLTAGE VS. TEMP.



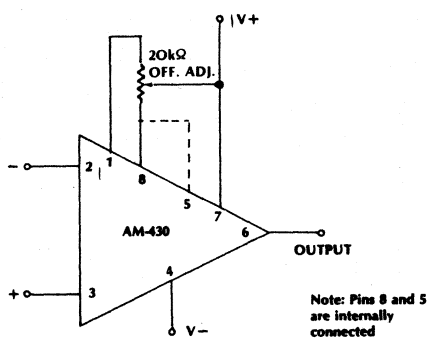
TYPICAL INPUT BIAS CURRENT VS. TEMP.



TYPICAL INPUT OFFSET CURRENT VS. TEMP.



CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	INPUT OFFSET VOLTAGE DRIFT	PRICE (1-24)
AM-430A	1.3 μV/°C max.	
AM-430B	0.6 μV/°C max.	
AM-430M	1.3 μV/°C max.	

Wide Bandwidth, Fast Settling Monolithic Operational Amplifiers AM-450 & AM-460 Series

FEATURES

- **120V/μsec. Slew Rate**
- **100 MHz Gain Bandwidth**
- **200 nsec. Settling to 0.1%**
- **300 Meg. Input Impedance**
- **Bipolar Differential Inputs**
- **5 nA Input Offset Current**

GENERAL DESCRIPTION

Datel-Intersil's AM-450 and AM-460 series bipolar input op amps provide a wide spectrum of capabilities required for high-speed, wide bandwidth signal processing applications. Features available within these two high-performance families include a 100 MHz gain-bandwidth product (AM-462), a 120V/μsec slew rate (AM-452), 300 Meg input impedance (AM-460 and AM-462) and 200 nsec settling time to 0.1% of full scale (AM-452).

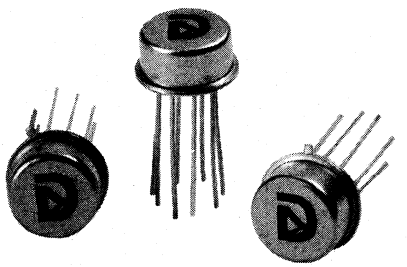
All models provide a full ±10V output at 10 mA and may be operated in non-inverting as well as inverting modes. Other features common to these units are low input offset currents and low input offset voltages as well as common mode rejection ratios typically greater than 90 dB.

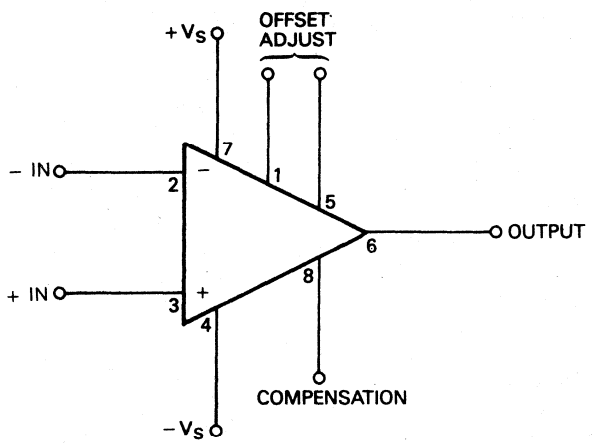
The AM-460 devices are bipolar operational amplifiers with very high impedance differential inputs, making them particularly well suited to applications as high speed comparators, wideband active filters and low distortion oscillators.

Both AM-450 and the AM-460 series units find many applications as fast acquisition sample and hold amplifiers, D/A output amplifiers, A/D input buffer amplifiers, pulse amplifiers, and fast integrators.

The AM-462-1 and AM-462-1M are packaged in a 14 pin ceramic DIP. All other models are packaged in an 8 lead, hermetically sealed TO-99 package with standard pin out, allowing them to be used easily as pin for pin replacements for general purpose IC operational amplifiers.

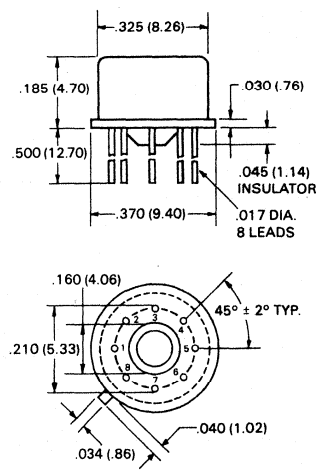
All models are available in 0°C to +70C operating temperature range or in -55°C to +125°C for suffix M models.



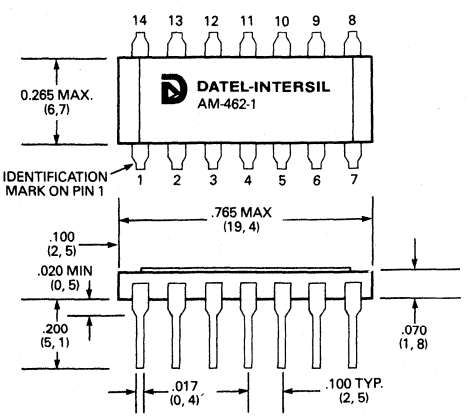


MECHANICAL DIMENSIONS
INCHES (MM)

TO-99



14-PIN DUAL INLINE CERAMIC PACKAGE
MODEL AM-462-1 AND AM-462-1M



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-450 AND AM-460 SERIES
(Typical @ +25°C, ±15 VDC Supplies, R_L + 2K, Unless Otherwise Noted)

	AM-450	AM-452	AM-460	AM-462
MAXIMUM RATINGS				
Power Supply Voltage	±20V	±20V	±22.5V	±22.5V
Differential Input Voltage	±15V	±15V	±12V	±12V
Peak Output Current	50 mA	50 mA	S.C. Prot.	S.C. Prot.
INPUT CHARACTERISTICS				
Common Mode Voltage Range[1], min.	±10V	±10V	±11V	±11V
Input Resistance	50 Meg	100 Meg	300 Meg	300 Meg
Input Resistance, min.	20 Meg	20 Meg	40 Meg	40 Meg
Input Offset Voltage	±4 mV	±5 mV	±3 mV	±3 mV
Input Offset Current, typ.	20 nA	20 nA	5 nA	5 nA
max.	50 nA	50 nA	25 nA	25 nA
Input Bias Current, typ.	125 nA	125 nA	5 nA[6]	5 nA
max.	250 nA	250 nA	25 nA	25 nA
OUTPUT CHARACTERISTICS				
Output Voltage, min.	±10V	±10V	±10V	±10V
Output Current, min.[7]	±10 mA	±10 mA	±10 mA	±10 mA
PERFORMANCE				
DC Open Loop Gain[2]	25K V/V	15K V/V	150K V/V	150K V/V
Full Power Bandwidth[2]	500 KHz	1600 KHz	75 KHz	600 KHz
Gain Bandwidth Product	12 MHz	20 MHz	12 MHz	100 MHz
Slew Rate	30V/μsec	120V/μsec	7V/μsec	35V/μsec
Settling Time, 10V to 0.1%	330 nsec[3]	200 nsec[3]	1.5μsec[4]	1.0 μsec
Common Mode Rejection Ratio[5], typ.	90 dB	90 dB	100 dB	100 dB
max.	74 dB	74dB	74 dB	74 dB
Input Offset Voltage Drift	20 μV/°C	30 μV/°C	10 μV/°C	15 μV/°C
External Compensation Required	None	Gains <3	Gains <3	Gains <5
Power Supply Rejection Ratio	90 dB	90 dB	90 dB	90 dB
POWER REQUIREMENTS				
Voltage, Rated Performance	±15 VDC	±15 VDC	±15 VDC	±15 VDC
Operating Voltage Range, min.	±10V	±10V	±5V	±5V
max.	±20V	±20V	±22.5V	±22.5V
Supply Current, max.	6 mA	6 mA	4 mA	4 mA
PHYSICAL-ENVIRONMENTAL				
Oper. Temp. Range, -1 & -2 Models	0°C to +70°C			
-1M & -2M Models	-55°C to +125°C			
Storage Temp. Range	-65°C to +150°C			
Package Type, -2 & -2M Models	TO-99			
-1 & -1M Models	14 Pin Ceramic DIP			

NOTES:
1. At Full Temperature
2. V_{OUT} = ±10V
3. C_L 50 pF
4. C_L = 100 pF
5. For ±5V Common Mode Range
6. 15nA typ. for AM-460-2M only
7. AM-460 and AM-462 outputs are short circuit protected

ORDERING INFORMATION

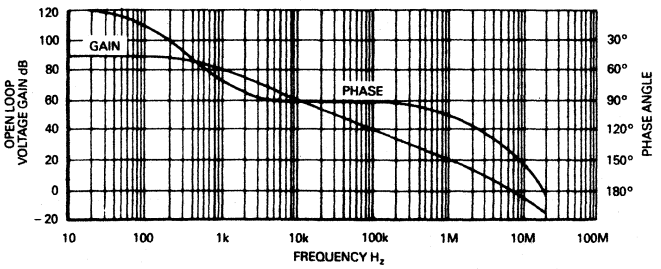
MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
AM-450-2	0°C to +70°C	
AM-450-2M	-55°C to +125°C	
AM-452-2	0°C to +70°C	
AM-452-2M	-55° to +125°C	
AM-460-2	0°C to +70°C	
AM-460-2M	-55° to +125°C	
AM-462-1, 2	0°C to +70°C	
AM-462-1M, 2M	-55° to +125°C	

Trimming Potentiometers: TP100K, TP20K

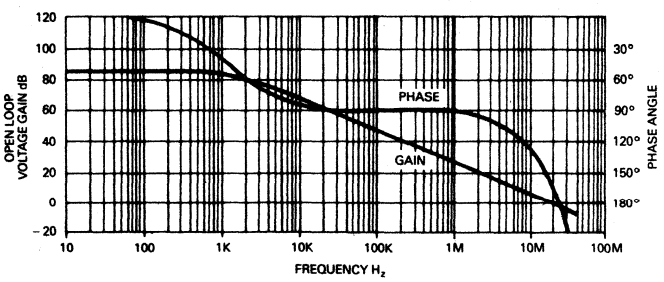
THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

TYPICAL OPEN LOOP FREQUENCY AND PHASE RESPONSE

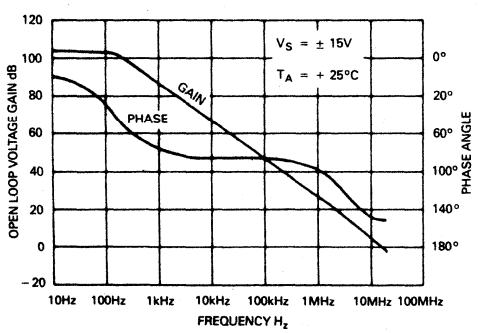
AM-450



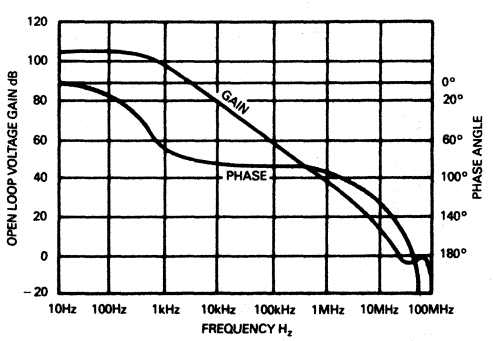
AM-452



AM-460



AM-462



CONNECTIONS

INPUT/OUTPUT CONNECTIONS

ALL -2 AND -2M MODELS

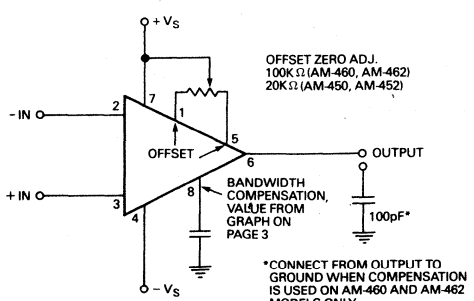
PIN	FUNCTION
1	OFFSET ADJUST
2	-INPUT
3	+INPUT
4	-Vs
5	OFFSET ADJUST
6	OUTPUT
7	+Vs
8	BANDWIDTH CONTROL
ON AM-460, AM-462 THE CASE IS CONNECTED TO-SUPPLY	

AM-462-1 AND AM-462-1M ONLY

PIN	FUNCTION
3	OFFSET ADJUST
4	-INPUT
5	+INPUT
6	-Vs
9	OFFSET ADJUST
10	OUTPUT
11	+Vs
14	BANDWIDTH CONTROL
ALL OTHER PINS ARE NO CONNECTION. CASE IS CONNECTED TO -SUPPLY	

EXTERNAL OFFSET ADJUSTMENT AND BANDWIDTH COMPENSATION (ALL MODELS)

EXTERNAL OFFSET ADJUSTMENT AND BANDWIDTH COMPENSATION (ALL MODELS)



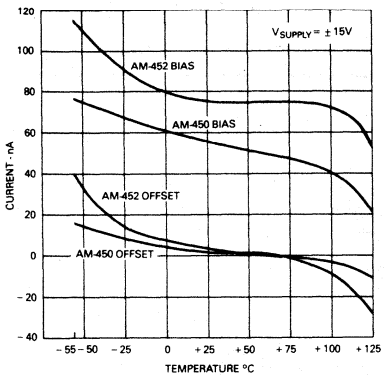
*CONNECT FROM OUTPUT TO GROUND WHEN COMPENSATION IS USED ON AM-460 AND AM-462 MODELS ONLY

NOTE: PINS SHOWN FOR TO-99 CASE

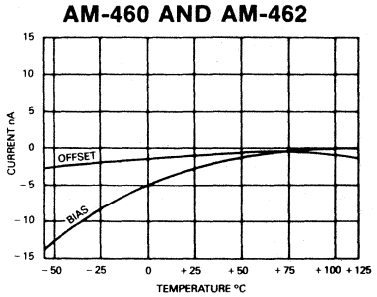
TYPICAL PERFORMANCE CURVES

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

AM-450 AND AM-452

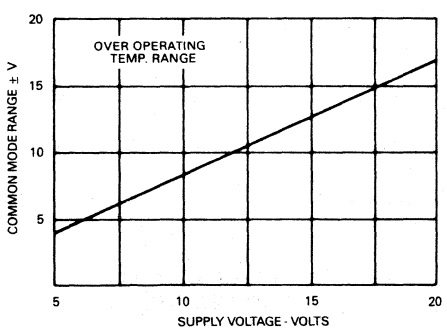


AM-460 AND AM-462



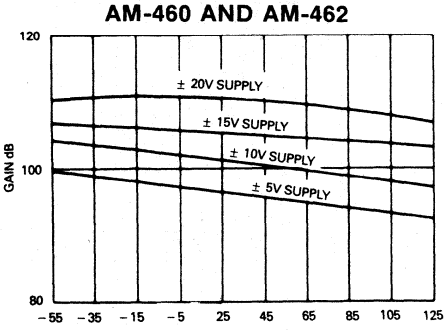
COMMON MODE VOLTAGE RANGE Vs SUPPLY VOLTAGE

AM-460 AND AM-462



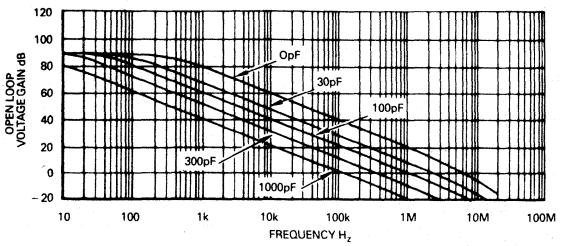
OPEN LOOP VOLTAGE GAIN Vs TEMPERATURE

AM-460 AND AM-462



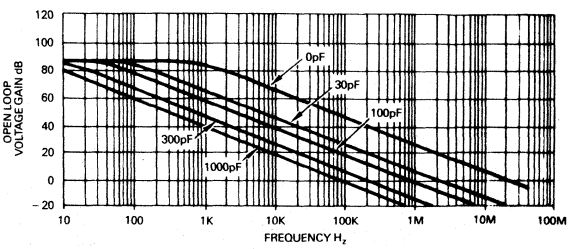
OPEN LOOP FREQUENCY RESPONSE AND EXTERNAL BANDWIDTH COMPENSATION

AM-450



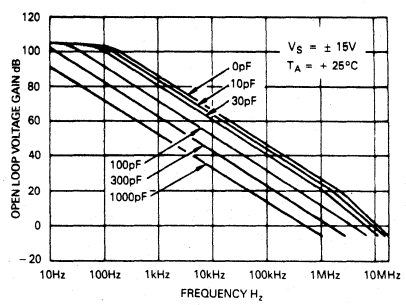
NOTE: EXTERNAL COMPENSATION COMPONENTS ARE NOT REQUIRED FOR STABILITY, BUT MAY BE ADDED TO REDUCE BANDWIDTH IF DESIRED.

AM-452



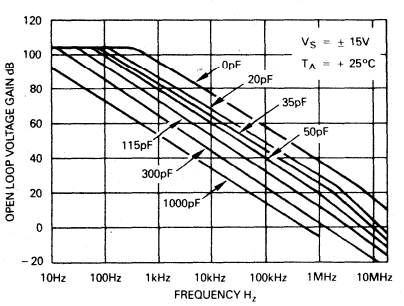
NOTE: EXTERNAL COMPENSATION IS REQUIRED FOR CLOSED LOOP GAIN <3.

AM-460



NOTE: EXTERNAL COMPENSATION COMPONENTS ARE NOT REQUIRED FOR STABILITY, BUT MAY BE ADDED TO REDUCE BANDWIDTH IF DESIRED. IF EXTERNAL COMPENSATION IS USED, ALSO CONNECT 100pF CAPACITOR FROM OUTPUT TO GROUND.

AM-462



NOTE: EXTERNAL COMPENSATION IS REQUIRED FOR CLOSED LOOP GAIN <5. IF EXTERNAL COMPENSATION IS USED, ALSO CONNECT 100pF CAPACITOR FROM OUTPUT TO GROUND.

Low Noise, Wideband Monolithic OP AMP AM-453-2

FEATURES

- **4 nV/√Hz Wideband Noise Voltage**
- **0.6 pA/√Hz Wideband Noise Current**
- **13V/μsec. Slew Rate**
- **20 mA Output Current**
- **±3V to ±20V Supply Range**

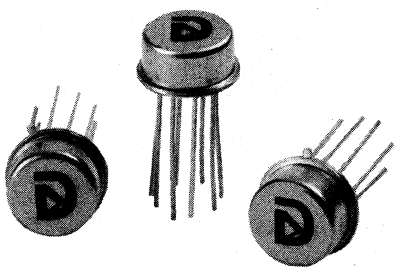
GENERAL DESCRIPTION

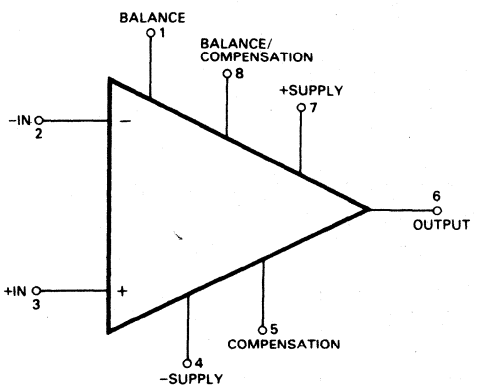
The AM-453-2 is a high performance, low noise monolithic operational amplifier. It offers better noise characteristics, improved output drive capability and extended small signal and power bandwidths when compared with standard operational amplifiers.

Typical input noise voltage is less than 7nV/ √Hz at 30Hz and drops to 4 nV/ √Hz for frequencies greater than 200 Hz. Input noise current is typically 2.5 pA/ √Hz at 30 Hz falling to only 0.6 pA/ √Hz for frequencies above 1 KHz. Along with low noise performance, the AM-453-2 has a gain bandwidth product of 10 MHz and a full power frequency response that typically extends to 200 KHz for an output swing of ±10V. In addition, the amplifier has the capability to drive 600Ω at 10V (RMS) when supplied by ±18V. The AM-453-2 is internally compensated for a gain of three or greater while frequency response may be optimized for various applications by the addition of an external compensation capacitor. Other features include a minimum common mode rejection ratio of 80 dB, 13V/μsec. slew rate, input overvoltage protection by diodes and a large supply voltage range extending from ±3V to ±20V.

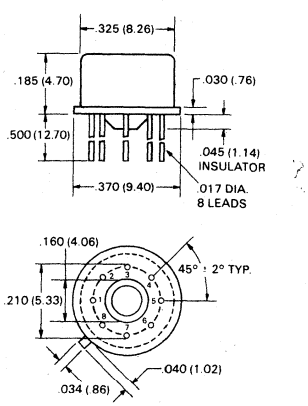
Its low noise, wideband, extended output characteristics make the AM-453-2 exceptionally well-suited to applications in instrumentation and control circuits, data acquisition circuits, wideband transducer amplification and audio frequency analog signal processing including active filters.

Packaged in an 8 lead hermetically sealed TO-99 case, the AM-453-2 is available in two operating temperature ranges, 0°C to 70°C or -55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BALANCE
2	-INPUT
3	+INPUT
4	-SUPPLY
5	COMPENSATION
6	OUTPUT
7	+SUPPLY
8	BAL./COMP.

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS — AM-453-2
Typical at 25°C, ±15V Supply unless otherwise noted

MAXIMUM RATINGS

Maximum Supply Voltage	±22V
Max. Common Mode Voltage Range	±V Supply
Maximum Differential Input Voltage[1]	±0.5V
Maximum Power Dissipation	680 mW

INPUT CHARACTERISTICS

Input Offset Voltage	0.5 mV typ., 4 mV max.
Input Offset Current	20 nA typ., 300 nA max.
Input Bias Current	500 nA typ., 1.5 μA max.
Input Resistance	100 KΩ
Common Mode Voltage Range	±12V min.

OUTPUT CHARACTERISTICS

Output Voltage	±12V min.
Output Current, S.C. Protected	±20 mA
Output Resistance	0.3Ω

PERFORMANCE

Input Offset Voltage Drift[2]	30μV/°C
Input Noise Voltage, 30 Hz	7 nV/$\sqrt{Hz}$
Input Noise Voltage, 200 Hz – 100 KHz	4 nV/$\sqrt{Hz}$
Input Noise Current, 30 Hz	2.5 pA/$\sqrt{Hz}$
Input Noise Current, 1 KHz – 100 KHz	0.6 pA/$\sqrt{Hz}$
Common Mode Rejection Ratio	100 dB typ. 80 dB min.
Power Supply Sensitivity	10 μV/V
D.C. Open Loop Gain	100,000 V/V
Full Power Frequency, ±10V Output	200 KHz
Unity Gain Bandwidth	10 MHz
Slew Rate	13V/μs

POWER REQUIREMENTS

Supply Voltage Rated Performance	±15V
Supply Voltage Range	±3V to ±20V
Supply Current	4 mA typ., 8 mA max.

PHYSICAL ENVIRONMENTAL

Operating Temperature Range	
AM-453-C	0°C to +70°C
AM-453-M	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Package, Hermetically Sealed	TO-99

NOTES:

1. Since the inputs are protected against overvoltage by diodes differential input exceeding 0.6V will cause large current flows unless current limiting resistors are used. Maximum current should be limited to ±10 mA.
2. 30μV/°C typical for C models only, 30μV/°C maximum for M models.

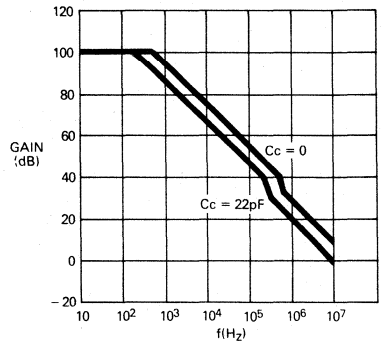
ORDERING INFORMATION

	OPERATING TEMP. RANGE
AM-453-2C	0°C to +70°C
AM-453-2M	-55°C to +125°C
Trimming Pot TP 100K	Cermet, 100 ppm/°C

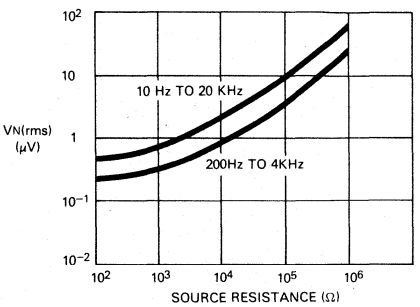
THE AM-453 AMPLIFIERS ARE COVERED BY GSA CONTRACT

TYPICAL PERFORMANCE

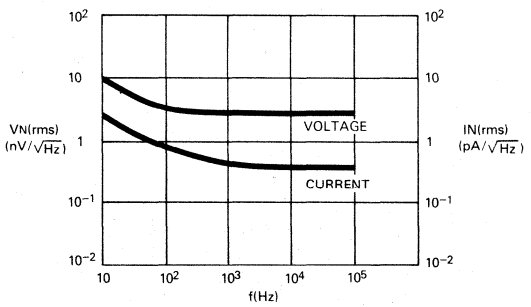
OPEN LOOP FREQUENCY RESPONSE



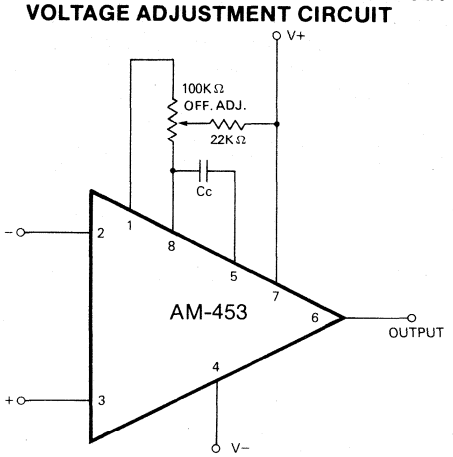
BROADBAND INPUT NOISE VOLTAGE



INPUT NOISE VOLTAGE AND CURRENT VS. FREQUENCY



FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT



High Voltage, Monolithic Operational Amplifier AM-464-2

FEATURES

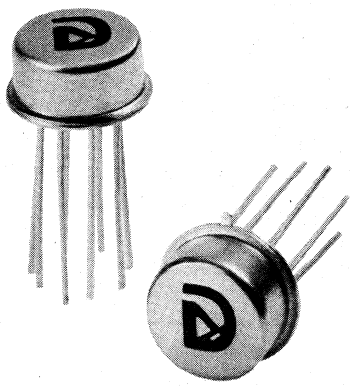
- ±35V Output Swing
- ±10V to ±40V Supply
- 4 MHz Gain Bandwidth
- 5V/μsec. Slew Rate
- 74 dB min. CMRR

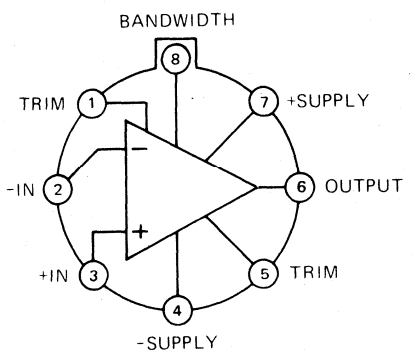
GENERAL DESCRIPTION

The AM-464-2 is a monolithic IC operational amplifier with an input common mode voltage range of ±35V and an output voltage swing of ±35V when operated from a ±40 supply. Along with high voltage performance this amplifier has a 4 MHz gain bandwidth product and a 5V/μsec. output slew rate. It is particularly useful in data conversion circuits and other signal processing applications where higher than normal common mode voltage and output voltage swings are required. The AM-464-2 is internally compensated for all gains and has an on-chip temperature sensing, output current-limiting circuit for absolute output short-circuit protection.

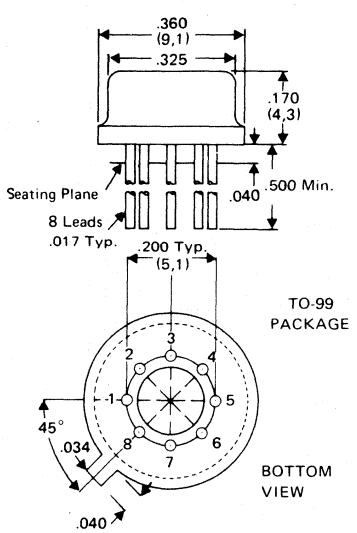
Other features of this amplifier include: common mode rejection of 74 dB minimum, input bias current of 30nA maximum, and open loop voltage gain of 100,000 minimum. The output slew rate of 5 volts per microsecond gives a 70 volt peak to peak sinusoidal output voltage at up to 23 kHz. The power supply voltage can range from ±10V to ±40 VDC to give output swings from ±5V to ±35V. Power supply quiescent current is only 3.2mA typical.

The AM-464-2 is packaged in an 8 lead, hermetically sealed TO-99 case and may be used as a pin for pin replacement for general purpose IC operational amplifiers such as 741, 101, and 108 for higher voltage applications. Operating temperature range is 0°C to 70°C for the AM-464-2 and −55°C to +125°C for the AM-464-2M.





MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: All leads gold plated KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	TRIM
2	-IN
3	+IN
4	-SUPPLY
5	TRIM
6	OUTPUT
7	+SUPPLY
8	BANDWIDTH (C_B)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, AM-464-2
(Typical at 25°C, ±40V Supply, unless otherwise noted)

MAXIMUM RATINGS
- Input Overvoltage ..... ±37V max.
- Supply Voltage ..... ±50V max.
- Internal Power Dissipation ..... 680 mW

INPUT CHARACTERISTICS
- Common Mode Voltage Range ..... ±35V min.
- Input Impedance, AM-464-2 ..... 200 Meg.Ω
- AM-464-2M ..... 250 Meg.Ω
- Input Offset Voltage, AM-464-2 ..... ±6 mV max.
- AM-464-2M ..... ±4 mV max.
- Input Bias Current, AM-464-2 ..... 30 nA max.
- AM-464-2M ..... 25 nA max.
- Input Offset Current, AM-464-2 ..... 30 nA max.
- AM-464-2M ..... 12 nA max.

OUTPUT CHARACTERISTICS
- Output Voltage ..... ±35V min.
- Output Current[1], AM-464-2 ..... ±10 mA min.
- AM-464-2M ..... ±12 mA min.
- Output Resistance ..... 500 Ohms
- Stable Capacitive Load ..... 100 pF

PERFORMANCE
- DC Gain, 5 KΩ Load ..... 100K V/V min.
- Common Mode Rejection[2], AM-464-2 ..... 74 dB min.
- AM-464-2M ..... 80 dB min.
- Input Offset Voltage Drift ..... 15μV/°C
- Input Offset Current[3], AM-464-2 ..... 50 nA max.
- AM-464-2M ..... 35 nA max.
- Input Noise Voltage, 10 Hz-10 KHz ..... 3 μV RMS

DYNAMIC CHARACTERISTICS
- Unity Gain Bandwidth ..... 4 MHz
- Slew Rate ..... 5V/μsec.
- Full Power Frequency, 70V p-p ..... 23 KHz

POWER REQUIREMENT
- Voltage, Rated Performance ..... ±40 VDC
- Power Supply Voltage Range ..... ±10 to ±40 VDC
- Quiescent Current, AM-464-2 ..... 4.5 mA max.
- AM-464-2M ..... 3.8 mA max.

PHYSICAL ENVIRONMENTAL
- Operating Temperature Range, AM-464-2 ..... 0°C to +70°C
- AM-464-2M ..... −55°C to +125°C
- Storage Temperature Range ..... −65°C to +150°C
- Package, Hermetically Sealed TO-99

NOTES:
1. Overload protected by current limiting and temperature sensing.
2. For common mode voltage = ±30V.
3. At maximum operating temperature.

ORDERING INFORMATION

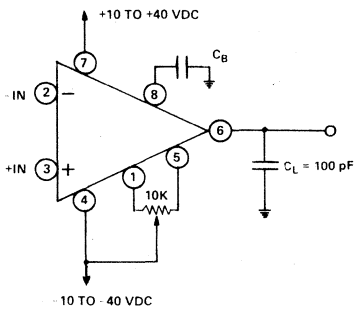
MODEL	OPER. TEMP RANGE	PRICE (1-24)
AM-464-2	0°C to +70°C	
AM-464-2M	−55°C to +125°C	

Trimming Potentiometer: TP 10K

THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

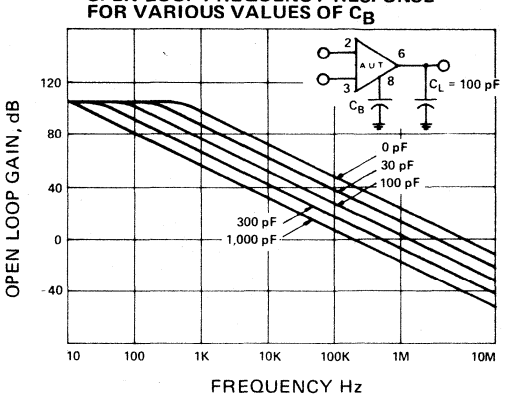
PERFORMANCE PARAMETERS

OFFSET TRIMMING AND BANDWIDTH REDUCTION

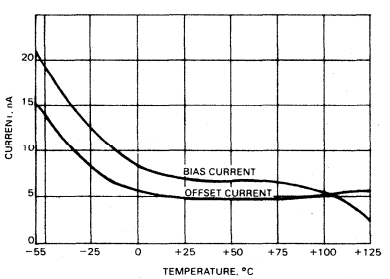


NOTES:
C_B is not required for stability since amplifier is internally compensated. It may be used to reduce bandwidth, however. C_L = 100 pF may be required for stability if external C_B is used.

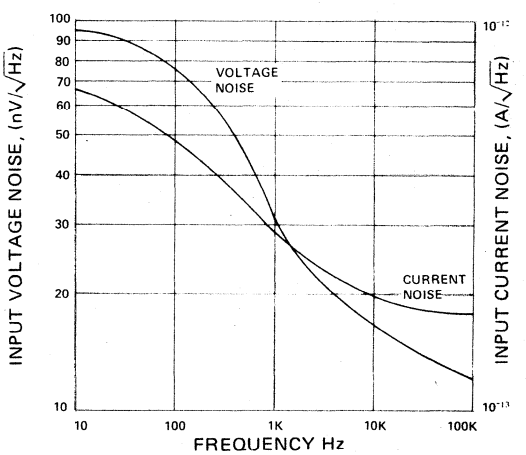
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF C_B



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



INPUT NOISE CHARACTERISTICS



Ultra-Fast Microelectronic Operational Amplifiers AM-500 Series

FEATURES

- **200 nsec. Settling to .01%**
- **1000V/μsec. Slew Rate**
- **100 MHz min. Gain-Bandwidth**
- **10^6 Open Loop Gain**
- **1μV/°C Drift**
- **±50 mA Output Current**

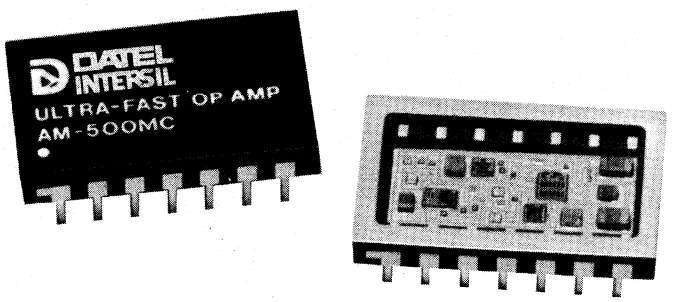
GENERAL DESCRIPTION

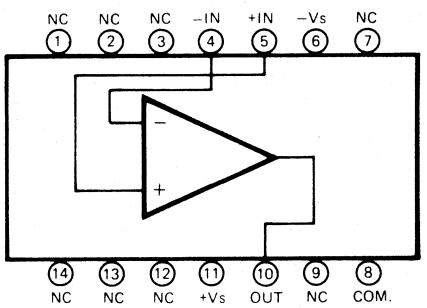
The AM-500 series amplifiers are ultra-fast settling operational amplifiers for use in inverting applications. A unique feedforward amplifier design combines the characteristics of a low drift DC amplifier with those of a very fast AC amplifier. For optimum fast settling performance, this amplifier has an open loop gain roll-off of 6 dB per octave to beyond 100 MHz. Miniature thin-film hybrid construction permits an optimum combination of semiconductor devices and minimum lead lengths to realize the amplifier circuitry. Applications for the AM-500 series include fast integrators, sample-holds, fast waveform drivers, and fast D/A converter output amplifiers.

Output settling time is 200 nanoseconds max. to .01% for a 10 volt step change. Slew rate is 1000V/μsec. for positive output transitions and 1800V/μsec. for negative transitions. This high slew rate permits undistorted reproduction of a full load, 20V peak to peak sine-wave out to 16 MHz. Gain bandwidth product is 100 MHz minimum.

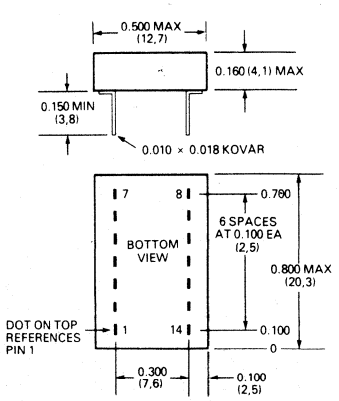
DC characteristics of the AM-500 series include a DC open loop gain of 10^6, 30 megohm input impedance, and 1 nanoampere bias current. Input offset voltage is ±0.5 mV and input offset voltage drift is 1μV/°C. Although these amplifiers do not operate differentially, a DC offset voltage in the range ±5V can be applied to the positive input terminal.

Power supply requirement is ±15VDC at 22 mA quiescent current. The amplifiers will operate over a supply range of ±10V to ±18V. Output current capability is ±50 mA with output short circuit protection. Four basic versions are available: AM-500GC and AM-500MC for 0° C to 70° C, AM-500MR for −25° C to +85° C, and AM-500MM for −55° C to +125° C. The device package is a 14 pin ceramic DIP.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	N.C.
2	N.C.
3	N.C.
4	-INPUT
5	+INPUT
6	-SUPPLY
7	N.C.
8	COMMON
9	N.C.
10	OUTPUT
11	+SUPPLY
12	N.C.
13	N.C.
14	N.C.

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SPECIFICATIONS, AM-500 SERIES

INPUT CHARACTERISTICS	
Input Common Mode Voltage Range[1]	±5V
Max. Input Voltage, no damage	±18V
Differential Input Impedance	30 Meg.
Input Bias Current	1nA typ., 4nA max.
Input Offset Current	0.5nA
Input Offset Voltage	0.5mV typ., 3mV max.
OUTPUT CHARACTERISTICS	
Output Voltage	± 10V min.
Output Current, S.C. protected	± 50mA
Stable Capacitive Load	100 pF
Output Impedance	25Ω
PERFORMANCE	
DC Open Loop Gain	10^6 volts/volt
Input Offset Volt. Drift, 0°C to 70°C	1μV/°C typ., 5μV/°C max.
-25°C to +85°C	2μV/°C typ., 7μV/°C max.
-55°C to +125°C	5μV/°C typ., 10μV/°C max.
Input Bias Current Drift, -55°C to +70°C	-20pA/°C
+70°C to +125°C	doubles every 10°C
Input Voltage Noise, .01 Hz to 1Hz[2]	5μV P-P
100Hz to 10kHz[2]	1μV RMS
1Hz to 10MHz[2]	20μV RMS
Power Supply Rejection Ratio	80 dB min.
DYNAMIC CHARACTERISTICS	
Gain Bandwidth Product	130MHz typ., 100 MHz min.
Slew Rate, positive going	1000V/μsec.
Slew Rate, negative going	1800V/μsec.
Full Power Frequency (20V P-P)	16MHz
Settling Time, 10V step to 1%[3]	70 nsec.
10V step to 0.1%[3]	100 nsec.
10V step to .01%[3]	200 nsec. max.
Overload Recovery Time	10μsec.
POWER REQUIREMENT	
Voltage, rated performance	+15VDC
Voltage, operating	+10V to ±18VDC
Quiescent Current	22 mA
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	
AM-500GC	0°C to 70°C
AM-500MC	0°C to 70°C
AM-500MR	-25°C to +85°C
AM-500MM	-55°C to +125°C
Storage Temperature Range	-55°C to +125°C
Package Type	14 pin ceramic
Pins	0.010X0.018" Kovar
Weight	0.09 oz. (2.5g)

NOTES:
1. DC only
2. -3dB single pole bandwidth
3. 1K input and feedback resistors, 2.4pF feedback capacitor

ORDERING INFORMATION

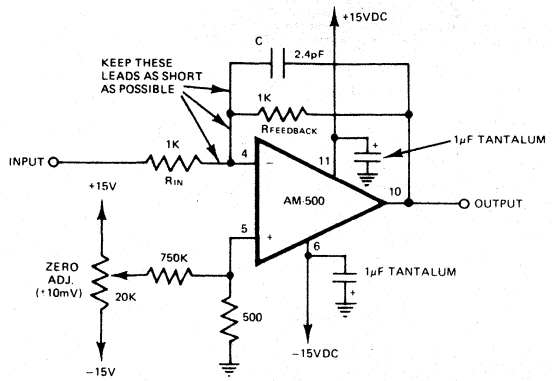
MODEL	OP. TEMP. RANGE	SEAL	PRICE (1-24)
AM-500GC	**0°C to 70°C**	**Epoxy**	**$ 72.50**
AM-500MC	**0°C to 70°C**	**Herm.**	**$ 93.50**
AM-500MR	**-25°C to +85°C**	**Herm.**	**$109.00**
AM-500MM	**-55°C to +125°C**	**Herm.**	**$157.00**

Socket: Standard 14 pin DIP socket. Not available from Datel-Intersil

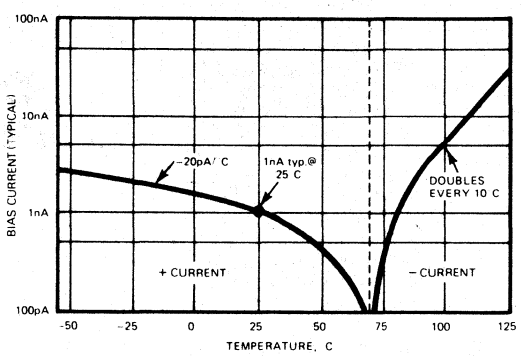
Trimming Potentiometer: TP 20K at $3.50

THE AM-500 AMPLIFIERS ARE COVERED BY GSA CONTRACT

CONNECTION FOR FAST SETTLING WITH GAIN OF –1



INPUT BIAS CURRENT VS. TEMPERATURE



TECHNICAL NOTES

1. The circuit design shows the connection of the AM-500 series for fast settling operation with a closed loop gain of -1. It can be used for fast settling at closed loop gains up to -10. The equivalent resistance seen by the summing junction should be 500 ohms or less. For gains larger than -1 use an input resistor of 500 ohms and pick a feedback resistor for the required closed loop gain (1K for -2, 1.5K for -3, etc.).
2. A small feedback capacitor should be used across the feedback resistor. Determine C in picofarads from the following formula: $C = \frac{1 + |G|}{816R}$ where G is closed loop gain and R is in kilohms.
3. Summing point leads must be kept as short as possible. Input and feedback resistors should be soldered close to the body of the resistor directly to the summing point (pin 4). Summing point capacitance to ground must be kept very low.
4. Low output impedance power supplies should be used with 1 μF tantalum bypassing capacitors at the amplifier supply terminals. There are internal .03 μF ceramic capacitors in the amplifier.
5. Although these amplifiers are inverting mode only, a DC voltage in the range of ±5V may be applied to the positive input terminal for offsetting the amplifier.

NEW

DATEL

Ultra-High Speed Wideband Operational Amplifier AM-1435

PRELIMINARY

FEATURES

- **70 nS Settling to 0.01%**
- **1 GHz Gain Bandwidth Product**
- **100 dB Open Loop Gain**
- **80 dB Minimum CMRR**
- **– 55°C to + 125°C Operation**

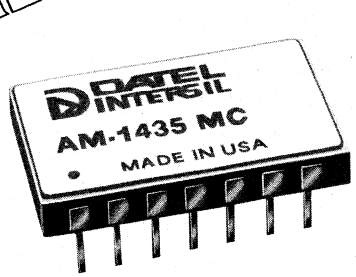
GENERAL DESCRIPTION

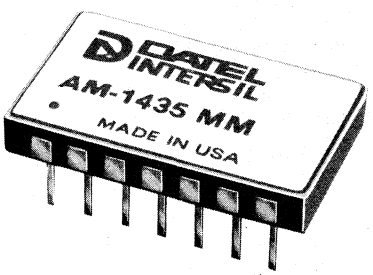
DATEL-INTERSIL's AM-1435 is an ultra-fast settling, wide-band operational amplifier. Utilizing precision thin-film hybrid construction and differential input operational amplifier design techniques, the AM-1435 achieves a settling time of only 70 nsec for a 10 volt step to 0.01% accuracy. High speed performance is optimized with high open-loop gain, flat frequency response beyond 10 kHz and a roll-off of 6 dB/octave to beyond 100 MHz. Gain bandwidth product is typically 1 GHz and slew rate is 300 V/μsec.

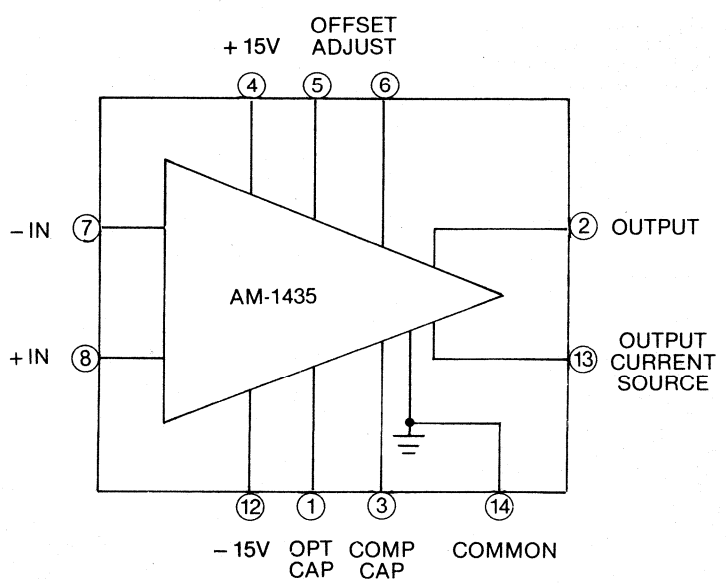
DC characteristics of the AM-1435 include a DC open loop gain of 100 dB, 1 MΩ input impedance, and an initial input offset voltage of only ± 2 mV. Input offset voltage drift is typically ± 5 μV/°C. Also featured is a minimum common mode rejection ratio of 80 dB and full power frequency of 8 MHz.

The AM-1435 is designed specifically for applications requiring high accuracy in the amplification of complex wide-band waveforms. Such applications would include radar and sonar signal processing, video instrumentation and ultra-fast, A/D, D/A converters and sample-hold amplifiers.

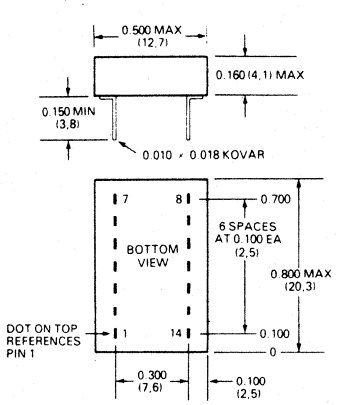
Power supply requirement is ± 15 VDC at 30 mA maximum quiescent current. Models are specified for operation over the commercial 0°C to ± 70°C, industrial, – 25°C to + 85°C and military – 55°C to + 125°C operating temperature ranges. The device package is a 14-pin, hermetically sealed, ceramic case. The AM-1435 is available fully screened to MIL-STD 883 level B.







MECHANICAL DIMENSIONS



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OPTIONAL CAP
2	OUTPUT
3	COMPENSATION CAP.
4	+ 15V SUPPLY
5	OFFSET ADJUST
6	OFFSET ADJUST
7	– INPUT
8	+ INPUT
9	N.C.
10	N.C.
11	N.C.
12	– 15V SUPPLY
13	OUTPUT CURRENT SOURCE
14	CASE/COMMON

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SPECIFICATIONS, AM-1435
(Typical at +25°C, ±15 VDC supplies, unless otherwise noted)

	MINIMUM	TYPICAL	MAXIMUM
INPUT CHARACTERISTICS			
Differential between Inputs			±4V
Common Mode Voltage Range	±7V	±8.5V	
Common Mode Rejection Ratio;			
DC	80 dB		
1 MHz	70 dB		
Input Impedance;			
common mode	1 MΩ || 2 pF		
differential mode	2.5 kΩ || 2 pF		
Input Offset Voltage[2]		±2 mV	5 mV
Input Bias Current		10 μA	20 μA
Input Offset Current		0.3 μA	
OUTPUT CHARACTERISTICS			
Output Voltage[3]		±7V	±5V
Output Current[3]		±14 mA	±10 mA
Stable Capacitive Load[4]			1000 pF
PERFORMANCE			
D.C. Open Loop Gain[3]	90 dB	100 dB	
Input Offset Voltage Drift		±5 μV/°C	±25 μV/°C
Input Bias Current Drift		50 nA/°C	100 nA/°C
Input Offset Current Drift		2 nA/°C	
Input Voltage Noise,			
0.01 Hz to 10 Hz		15 μV P-P	
100 Hz to 10 kHz		1.6 μV RMS	
10 Hz to 1 MHz		5.2 μV RMS	
Input Current Noise[5],			
0.01 Hz to 10 Hz		2.5 nA P-P	
100 Hz to 10 kHz		2.5 nA RMS	
10 Hz to 1 MHz		3.5 nA RMS	
Power Supply Rejection Ratio		0.15 mV/V ΔV_S	
DYNAMIC CHARACTERISTICS			
Gain Bandwidth Product	700 MHz	1000 MHz	
Unity Gain Bandwidth		150 MHz	
Full Power Frequency[6]	8 MHz	10 MHz	
Settling Time, 10V to 0.025%[7]		60 nS	75 nS[8]
10V to 0.01%		70 nS[8]	
5V to 1.0%		25 nS	
5V to 0.1%		40 nS	60 nS
1V to 1.0%		10 nS	
1V to 0.1%		20 nS	
Slew Rate[6]	250 V/μS	300 V/μS	
Overshoot			1%
Propagation Delay		5 nS	
Rise Time, 10V Step		40 nS	
Overload Recovery Time		50 nS	
POWER REQUIREMENT			
Rated Supply Voltage	±12V	±15V	±16V
Quiescent Current[9]			±30 mA
PHYSICAL ENVIRONMENTAL			
Operating Temperature Range:			
AM-1435MC		0°C TO +70°C	
AM-1435MR		−25°C TO +85°C	
AM-1435MM[10]		−55°C TO +125°C	
Storage Temperature Range		−65°C TO +150°C	
Package		14-pin, hermetically sealed ceramic DIP	

NOTES:
1. Specified for D.C. linear operation. Maximum common mode voltage range is typically ±10V.
2. Adjustable to zero.
3. R_L = 500Ω.
4. C_1 = 3 pF.
5. Referred to input.
6. C_1 = 0.5 pF.
7. Specified for AM-1435MR and AM-1435MM. Specification for AM-1435MC is 85 nS maximum.
8. C_f = 1 pF.
9. $\pm V_S$ = ±15V.
10. With 18°C/watt heat sink.

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for rated performance. The extensive use of a ground plane for all common connections is recommended. Lead length should be kept to a minimum with point to point connections wired directly to the amplifier pins. 1 μF tantalum bypass capacitors should be used at the V+ and V− pins.
2. Operation of the AM-1435MM over the +85°C to +125°C temperature range requires additional thermal dissipation to achieve rated performance, use of an 18°C/W heat sink is recommended.
3. No input protection is provided so as to maximize frequency response. As a result, several precautions must be observed: Do not apply positive supply voltage before the negative supply. Do not apply power to either input prior to power-up. If frequency response is not critical, installation of an external input protection circuit is recommended.
4. A 1 μF bypass capacitor connected to Pin 1 may be required to inhibit output oscillation when driving capacitive loads.
5. To ensure stable operation when the noise gain is less than 10, a 2 pF compensation capacitor must be connected between pins 3 and 7. The value of the compensation capacitor may be application sensitive.
6. The AM-1435 is a prime choice as a current to voltage converter due to its excellent E_{os} and I_{os} tempco's. Input bias currents are easily compensated by adding a resistor from pin 8 to ground, which is equal to the parallel combination of the feedback resistor and input impedance.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PRICE
AM-1435MC	0°C to +70°C	$
AM-1435MR	−25°C to +85°C	$
AM-1435MM	−55°C to +125°C	$

Trimming potentiometer TP1K
MIL-STD-883B screening also available.

Programmable Gain Instrumentation Amplifiers Models AM-542, AM-543

FEATURES

- 1 to 1024 Gains
- Digital Gain Selection
- $10^9\Omega$ Input Impedance
- 6 μsec Settling Time, AM-543
- 1 μV/°C Offset Drift, AM-542
- ± 3 to ± 18 VDC Analog Supply Range, AM-542
- 6 mV P-P Output Voltage Noise, AM-543

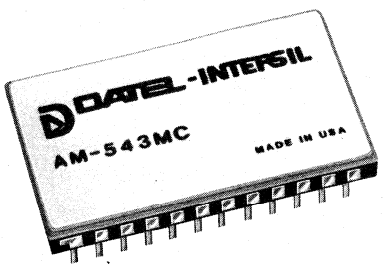
GENERAL DESCRIPTION

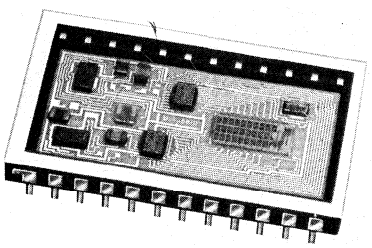
The AM-542 and AM-543 are high performance, digitally controlled, Programmable Gain Instrumentation Amplifiers. The AM-542 permits selection of gains from 1 to 1024 in 11 binary weighted steps, the AM-543 permits selection of gains from 1 to 128 in 8 binary weighted steps. Gain selection is accomplished by the input of a 4 bit word. One version is optimized for low drift with extremely low noise and the other is optimized for fast settling. Use of these devices in data acquisition applications yields a system with wide dynamic range and high resolution.

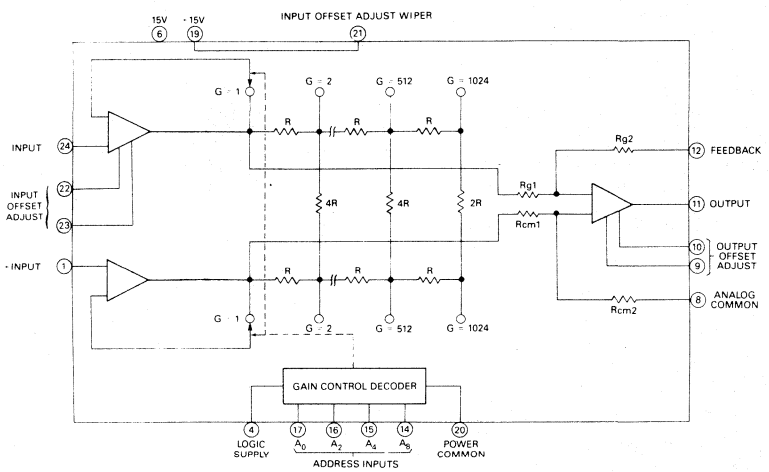
The AM-542 is optimized for low drift performance, having an input offset voltage drift specified at only 1 μV/°C, while the gain temperature coefficient is a maximum of only ± 5 ppm/°C. Other specifications include an input impedance of $10^9\Omega$, Common Mode Rejection of 90 dB minimum, and an output voltage range of ± 10.5V min. at 5 mA. The AM-542 operates from analog supply voltages from ± 3 VDC to ± 18 VDC with very low power dissipation.

The AM-543 is tailored for high speed applications; a 20V step settles to 0.01% in only 6 μsec maximum at unity gain. These devices also feature a slew rate of 13V/μsec, an input impedance of $10^{12}\Omega$, Common Mode Rejection of 80 dB minimum, and a gain temperature coefficient of ± 10 ppm/°C maximum. The AM-543 operates with analog supply voltages from ± 10 VDC to ± 16 VDC.

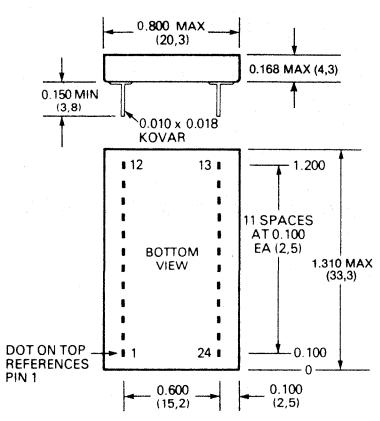
Both devices are packaged in a compact, hermetically sealed 24 pin ceramic DIP and are available for operation over the 0°C to +70°C, −25°C to +85°C, and −55°C to +125°C temperature ranges. High reliability screening in compliance with MIL-STD-883, Level B is also available. For details contact the factory.







MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+ INPUT
2	NC
3	NC
4	LOGIC SUPPLY
5	NC
6	−15 VDC
7	NC
8	ANALOG COMMON
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	FEEDBACK
13	NC
14	A_8
15	A_4
16	A_2
17	A_0
18	NC
19	+15 VDC
20	POWER COMMON
21	INPUT OFF. ADJ. WIPER
22	INPUT OFFSET ADJUST
23	INPUT OFFSET ADJUST
24	− INPUT

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SPECIFICATIONS, AM-542 AND AM-543
(Typical at +25°C, ± 15 VDC and +5 VDC supplies, unless otherwise noted)

	AM-542	AM-543
MAXIMUM RATINGS		
Positive Supply, Pin 19	+22V	+16V
Negative Supply, Pin 6	−22V	−16V
Input Voltage Range	±20V	±20V
No Damage	±VCC	±VCC
INPUT CHARACTERISTICS		
Input Offset Voltage, adj. to zero	±50 μV, max.	±50 μV
Input Bias Current, max.		
MC models	±50 nA	±50 pA
MR/MM models	±14 nA	±50 pA
Input Offset Current, max.		
MC models	±50 nA	±50 pA
MR/MM models	±14 nA	±50 pA
Input Impedance, Diff. Mode	$10^9\Omega$	$10^{12}\Omega$
Com. Mode	$2 \times 10^9\Omega$	$10^{12}\Omega$
Common Mode Volt. Range min.[1]	±11V	±10.25V
Digital Inputs, Logic "1", min.[2]	+2.4V @ 2 μA	+2.4V @ 2 μA
Digital Inputs, Logic "0", max.	+0.8V @ 50 μA	+0.8V @ 50 μA
OUTPUT CHARACTERISTICS		
Output Voltage Range, min.[3]	±10.5V	±11V
Output Current, min.	±5 mA	±1 mA
Output Offset Voltage, max.[4]	±1 mV	±12 mV
Output Voltage Noise, DC to 1 MHz, max.[5]	6 mV (P-P)	7 mV (P-P)
PERFORMANCE		
Gain Range	1 to 1024	1 to 128
Gain Accuracy, max.	±.02%[6]	±.05%
Gain Nonlinearity, max.	.005%[7]	.01%
Gain Temp. Coefficient, max.	±5 ppm/°C	±10 ppm/°C
Input Offset Temp. Drift,		
0 to +70°C	1 μV/°C	30 μV/G + 30 μV/°C
+70°C to +85°C	5 μV/°C	35 μV/G + 30 μV/°C
+85°C to +125°C	10 μV/°C	40 μV/G + 30 μV/°C
Power Supply Reject. Ratio, min.	80 dB	80 dB
Input Current Noise, max[8]	90 pA (P-P)	270 pA (P-P)
Common Mode Rejection Ratio,		
60 Hz, min[9]	86 dB	86 dB
DC, min[9]	90 dB	80 dB
Small Signal Bandwidth, (−3 dB)		
G = 1	500 kHz	7 MHz
G = 128	—	—
G = 1024	500 Hz	—
Slew Rate	0.14V/μsec	13V/μsec
Settling Time, 20V to 0.01%, max.		
G = 1	150 μsec	6 μsec
G = 16	200 μsec	10 μsec
G = 64	400 μsec	40 μsec
G = 128	400 μsec	100 μsec
G = 256	700 μsec	---
G = 512	1.4 msec	---
G = 1024	2.8 msec	---
POWER REQUIREMENTS		
Analog Supply, Rated Value	±15V @ 20 mA, max.	±15V @ 25 mA, max.
Analog Supply Range	±3V to ±18VDC	±10V to ±16 VDC
Logic Supply	+3V to +18V @ 5 nA max.	+3V to +18V @ 5 nA max.
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range		
MC	0 to +70°C	
MR	−25 to +85°C	
MM	−55 to +125°C	
Storage Temperature Range	−65 to +150°C	
Package Type	Hermatically Sealed 24 Pin DIP	

TECHNICAL NOTES

1. The AM-542 and AM-543 have an offset adjustment capability for each stage, input and output. The output trim should be sufficient to zero out offset errors on the lower gain ranges, adjustment should be made with a gain of 1 selected. For the higher gain ranges, the input offset zeroing circuit should be used to optimize accuracy. Adjustment of the input offset should be made with a gain of 1024 selected on the AM-542, and a gain of 128 selected for the AM-543.

2. Power supply inputs to the AM-542 and AM-543 are bypassed internally. However, for best performance both power supplies should be bypassed with 1 μF electrolytics in parallel with .01 μF ceramic capacitors as close as possible to the ± supply pins.

3. The digital inputs of the AM-542/543 are TTL/CMOS compatible. However, when interfacing with TTL logic, it is recommended that 10 kΩ pull-up resistors be used. When interfacing with CMOS logic, the logic supply pin (pin 4) should be connected to the system logic supply.

ORDERING INFORMATION

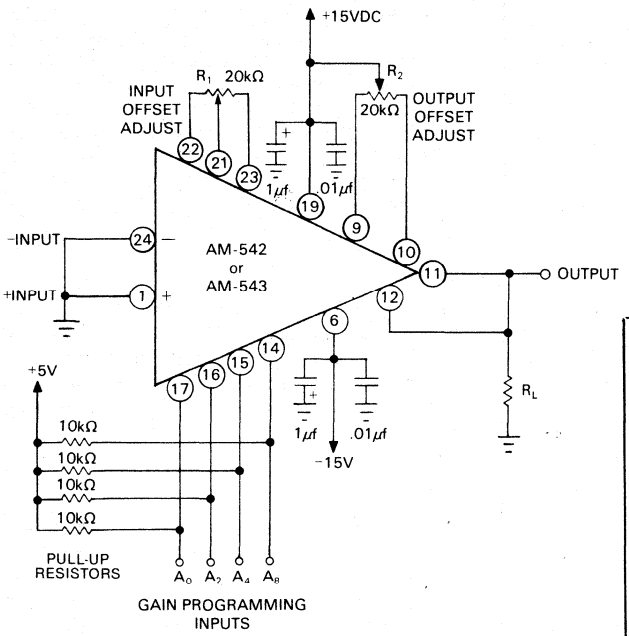
MODEL NO.	OPERATING TEMP. RANGE	PRICE (1-24)
AM-542MC	0°C to +70°C	
AM-542MR	−25°C to +85°C	
AM-542MM	−55°C to +125°C	
AM-543MC	0°C to +70°C	
AM-543MR	−25°C to +85°C	
AM-543MM	−55°C to +125°C	

NOTES:

1. As with any three amplifier instrumentation amplifier configuration, the voltage at either input ± ½ the output voltage must not exceed ± 12V (± 11 V - AM543) for linear operation.
2. Requires pull up resistor for TTL logic. Please refer to technical note 3.
3. AM-542, $R_L = 2\ k\Omega$. AM-543, $R_L = 10\ k\Omega$.
4. G - 1, adjustable to zero.
5. AM-542, $R_S = 5\ k\Omega$, G = 1024. AM-543, $R_S = 5\ k\Omega$, G = 128.
6. Maximum for AM-542MM/MR. Maximum for AM-542MC is ±.05%.
7. Maximum for AM-542MM/MR. Maximum for AM-542MC is .01%.
8. DC to 1 kHz
9. 1 kΩ source imbalance, G = 2.

CONNECTION AND APPLICATION

OFFSET ADJUSTMENT



The AM-542/543 are functionally laser trimmed to reduce initial offset voltage and offset voltage change due to gain change to a minimum level. However, for critical applications where zero offset is required, the following procedure can be followed to externally zero the offset.

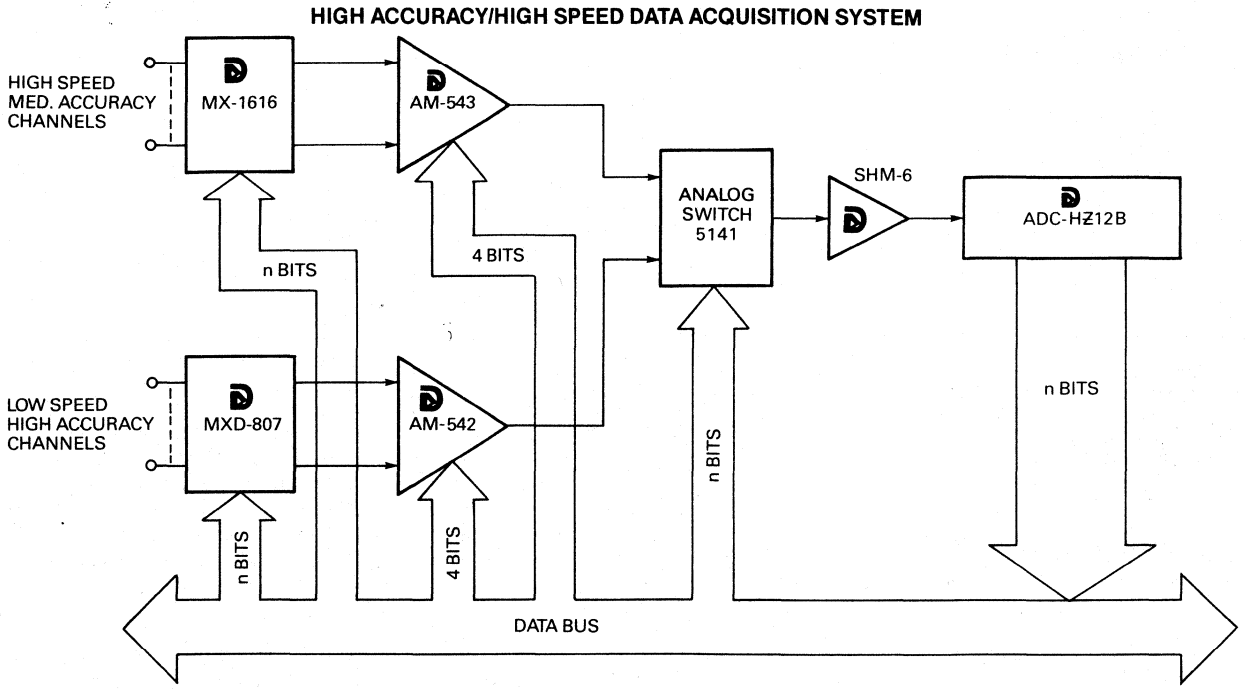
1. Allow the Amplifier to reach operating temperature.
2. Set R_1 and R_2 to mid-range.
3. Set gain to 1 V/V.
4. Adjust R_2 for zero output.
5. Set gain to 1024 (128-AM-543) V/V
6. Adjust R_1 for zero output.

This technique minimizes the offset voltage change over the maximum change in gain. Trimming may cause input offset temperature drift to increase slightly.

GAIN STATE TRUTH TABLE

DIGITAL INPUTS				GAIN	
A_8(PIN 14)	A_4(PIN 15)	A_2(PIN 16)	A_0(PIN 17)	AM-542	AM-543
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	4	4
0	0	1	1	8	8
0	1	0	0	16	16
0	1	0	1	32	32
0	1	1	0	64	64
0	1	1	1	128	128
1	0	0	0	256	—
1	0	0	1	512	—
1	0	1	0	1024	—

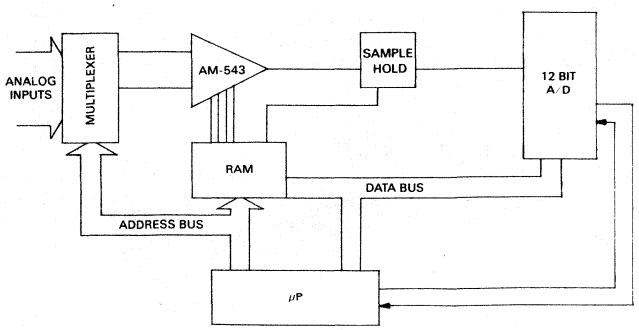
HIGH ACCURACY/HIGH SPEED DATA ACQUISITION SYSTEM



A system that uses the AM-542 with high gain, high accuracy, low to moderate speed transducers and the AM-543 with moderate gain, moderate to high speed transducers.

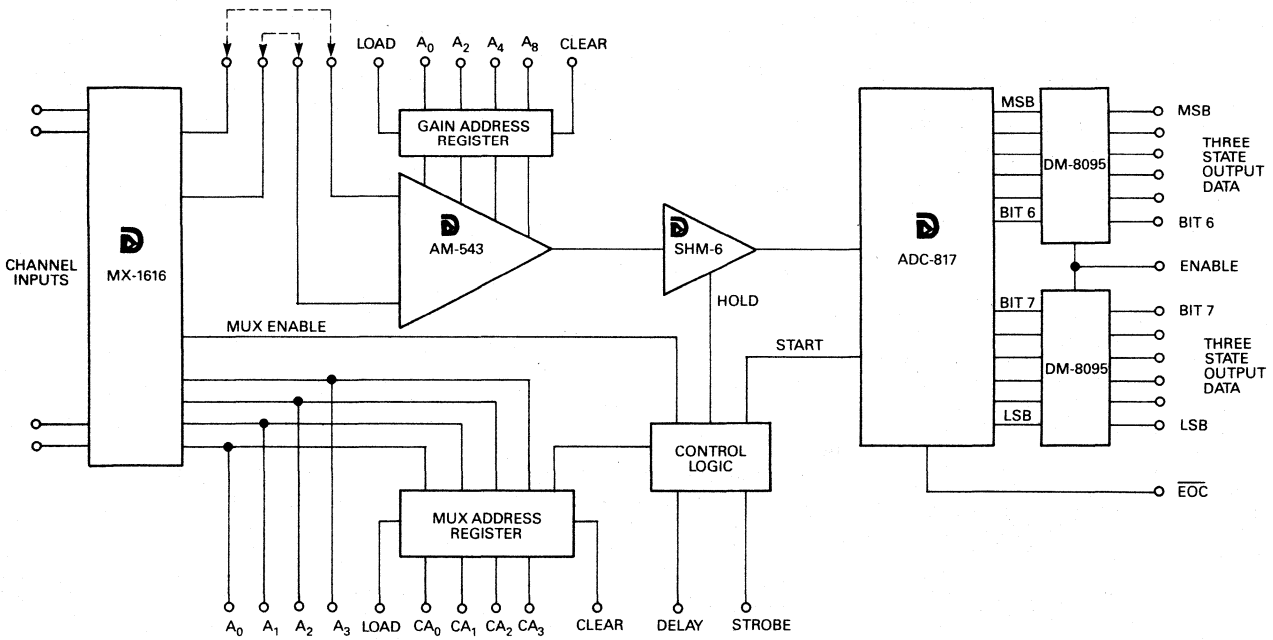
TYPICAL APPLICATIONS

MICROPROCESSOR BASED DATA ACQUISITION SYSTEM



A typical application of the AM-542/543 is in a microprocessor controlled data acquisition system. The microprocessor loads the RAM with the desired gain coding. This coding relates the selected gain ranges to a specific address. When the processor instructs the multiplexer to multiplex a particular analog input channel, this instruction is also received by the RAM, which puts out the appropriate gain code to the AM-542/543. This system allows acquisition of signals over a wide dynamic range at high resolution.

HIGH SPEED DATA ACQUISITION SYSTEM



A high speed data acquisition system with 8 differential inputs and 12 bit resolution that utilizes the AM-543. If the control logic is timed so that the Sample-Hold-ADC section is converting one analog value while the mux-amplifier section is allowed to settle to the next input value, throughput rates greater than 156 KHz can be achieved. The AM-543 is used with Datel-Intersil's ADC-817, a 12 bit hybrid A/D with a 2 μsec conversion rate, the SHM-6, a .01%, 1 μsec hybrid Sample-Hold, and the MX-1616, a low cost, high speed, monolithic analog multiplexer.

The system works as follows:

The μP selects a channel and initiates a conversion at G = 1 and then looks at the MSB of the conversion result. If the MSB = 1, the μP will store the value. If the MSB = 0, the μP will select G = 2. The μP will repeat the cycle of gain incrementing, comparison, and analog to digital conversion until the MSB = 1. The μP will then test for an output of all 1's, as this is the full scale output of the A/D. If the output is all 1's, the μP will decrement the gain by 1 step and perform the final conversion.

NEW

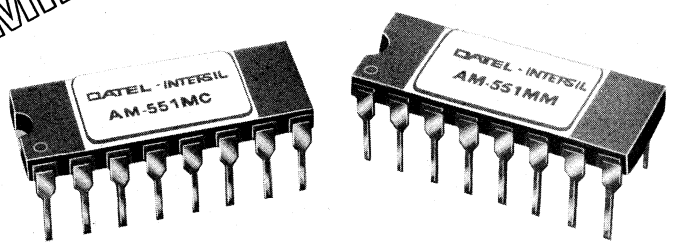
DATEL

Low Cost, Hybrid Programmable Gain Instrumentation Amplifier AM-551

PRELIMINARY

FEATURES

- 1 to 1000 Gain Range
- ±0.01% Max. Nonlinearity
- 2 μsec Settling Time
- 100 dB CMRR
- Low Cost



GENERAL DESCRIPTION

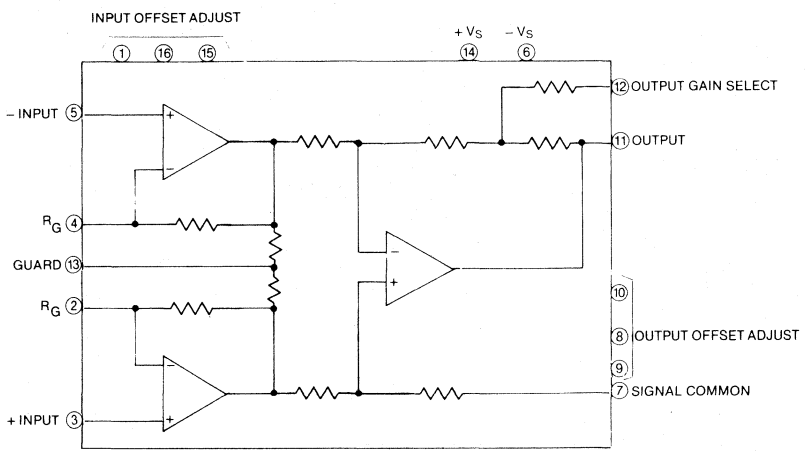
DATEL-INTERSIL's AM-551 is a low cost, high performance, programmable gain instrumentation amplifier manufactured with hybrid thin-film technology. Gain is adjustable over a range of 1 to 1000 by the addition of a single external resistor and a simple user-selectable pin-strapping option. Maximum gain nonlinearity is ±0.01%.

The AM-551 dynamic characteristics include a settling time of 2 μsec for a 20V output step to 0.01% accuracy. Slew rate is 23V/μsec and small signal bandwidth is 400 kHz. Other specifications include a common mode rejection ratio of 100 dB, a $10^{12}\Omega$ input impedance and a minimum output voltage swing of ± 11V. Maximum offset voltage drift is ± 15 μV/°C.

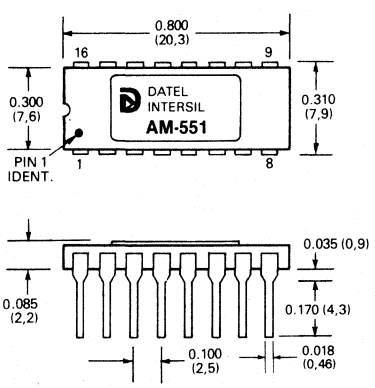
The AM-551 is a self-contained, functionally complete device, containing a high impedance variable gain voltage follower input stage followed by a differential output stage with user selectable gains of 1 or 10. High accuracy, ultra-low drift thin-film technology is used in the fabrication of all interconnected resistor networks.

The combination of high accuracy, speed, low cost, and rugged hybrid construction make the AM-551 an ideal choice for applications involving the remote amplification of low-level signals produced by thermocouples, strain gages and RTD's, high performance data acquisition systems and remote instrumentation systems.

Power requirement is ±15 VDC and all devices are cased in miniature, hermetically sealed, 16-pin ceramic packages. Models are available for operation over the commercial, 0°C to +70°C industrial, −25°C to +85°C, and military, −55°C to +125°C operating temperature ranges. High reliability screening in conformance with MIL-STD-883 level B is also available. For details contact the factory.



MECHANICAL DIMENSIONS INCHES (MM)



16-PIN CERAMIC DIP

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	INPUT OFFSET ADJUST
2	R_G (Gain Resistor)
3	+ INPUT
4	RG (Gain Resistor)
5	− INPUT
6	$-V_S$
7	SIGNAL COMMON
8	OUTPUT OFFSET ADJ. WIPER
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	OUTPUT GAIN SELECT
13	GUARD
14	$+V_S$
15	INPUT OFFSET ADJUST
16	INPUT OFFSET ADJ. WIPER

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SPECIFICATIONS, AM-551
(Typical at +25°C, ±15VDC supplies, unless otherwise noted)

MAXIMUM RATINGS	
Positive Supply, Pin 14	+18V
Negative Supply, Pin 6	−18V
Input Voltage Range	±18V
Differential Input Voltage Range	±30V
Output Short Circuit	Continuous
Power Dissipation	720 mW
INPUT CHARACTERISTICS	
Input Offset Voltage, unadjusted[1], max.	±1 mV × gain
Input Bias Current, max.	±100 pA
Input Offset Current, max.	±20 pA
Input Impedance, Diff. or Com. Mode	$10^{12}\Omega$
Common Mode Voltage Range, min.	±11V
OUTPUT CHARACTERISTICS	
Output Voltage Range, min.[2]	±11V
Output Current, min.	±5 mA
Output Impedance[3]	0.5Ω
PERFORMANCE	
Gain Range[4]	1 to 1000 V/V
Gain Equation[7]	$G = (1 + 20k/R_G)\ G_2$
Gain Accuracy, max.	±0.04%
Gain Nonlinearity, max.	±0.01%
Gain Tempco, max.[5]	50 ppm/°C
Offset Voltage Drift, max.	15 μV/°C
Input Bias Current Drift	Doubles for every 10°C
Input Voltage Noise, DC to 100 Hz	20 nV/√Hz
Power Supply Rejection Ratio, min.	82 dB
Common Mode Rejection Ratio[6]	
1 kHz	96 dB
100 Hz	98 dB
DC	100 dB
Slew Rate	23 V/μS
Small Signal Response, (−3 dB)	
G = 1	400 kHz
G = 10	150 kHz
G = 100	100 kHz
G = 1000	40 kHz
Settling Time, 20V to 0.01%	
G = 1	2.0 μS
G = 10	4.6 μS
G = 100	20 μS
G = 1000	200 μS
POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V
Supply Current, max.	27 mA
Power Supply Range	±5V to ±18V
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	
MC	0°C to +70°C
MR	−25°C to +85°C
MM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Type	16-Pin Ceramic DIP

1. Adjustable to zero.
2. R_L = 2 kΩ
3. At 1 kHz, for all gain ranges.
4. To 0.01% accuracy. Higher gains are achievable, however, performance will degrade.
5. Tempco of R_G = ±0 ppm/°C. For R_G = ∞, Gain Tempco = 5 ppm/°C
6. 1 kΩ Source Imbalance.
7. G_2 is the gain of the second stage of the AM-551. Connecting output gain select (Pin 12) to the output (Pin 11) sets the second stage gain at 1. Connecting output gain select (Pin 12) to signal common (Pin 7) sets the second stage gain at 10. R_G is the gain resistor for the first stage and is connected to R_G (Pins 2, 4).

TECHNICAL NOTES

1. A 25 kΩ trimpot may be used for both input and output offset adjusts. The trimpot is connected across the input offset adjust pins (Pins 1, 15) and the wiper is connected to Pin 16.

   For output offset adjust, the trimpot is connected across the output offset adjust pins (Pins 10, 9) with the wiper connected to Pin 8.
2. For unity gain, R_G is left open and the output gain select pin (Pin 12) is tied to the output pin (Pin 11). To avoid oscillation in the unity gain configuration, the connection between the output gain select pin and the output pin should be kept as short as possible.
3. Gain selection is accomplished in two stages. The input stage gain (G_1) is selected by an external gain resistor (R_G) connected across the (R_G) pins, (Pins 2, 4,), and is expressed as follows:

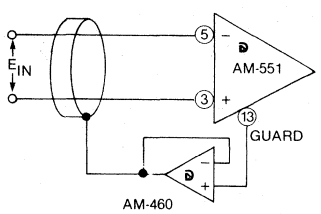
$$G_1 = 1 + \frac{20k}{R_G}$$

   The output stage gain (G_2) is selected by external pin-strapping: For $G_2 = 1$, connect the gain select pin (Pin 12) to the output pin (Pin 11). For $G_2 = 10$, connect the gain select pin (Pin 12) to the signal common pin (Pin 7).

   The total gain of the amplifier is as follows:

$$G_t = G_1 \times G_2 = \left(1 + \frac{20k}{R_G}\right) G_2$$

4. Both power supplies should be bypassed to ground with 0.1μF electrolytic capacitors.
5. A guard (pin 13) is provided to improve AC common mode rejection by compensating for unbalanced capacitance due to long input leads. Use of the guard function is recommended where input leads are longer than a few inches. In cases where the input leads are very long or where system bandwidth is very high, the addition of a buffer amplifier is recommended. The following diagram shows the typical guard drive connections to the AM-551 using DATEL-INTERSIL's AM-460.



Guard Drive Connection

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	PRICE (1-24)
AM-551MC	0°C to +70°C	$
AM-551MR	−25°C to +85°C	$
AM-551MM	−55°C to +125°C	$

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NEW

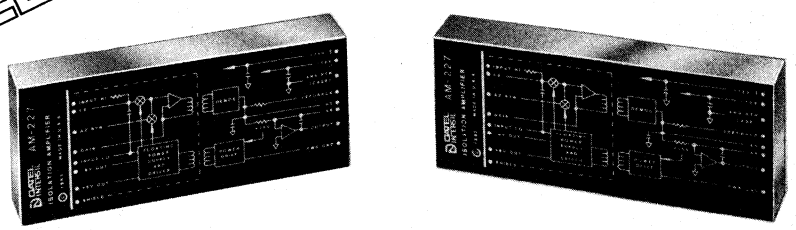
DATEL

Low Cost, Ultra-Stable Isolation Amplifier AM-227

PRELIMINARY

FEATURES

- **1000 VDC Isolation**
- **0.005% Nonlinearity**
- **166 dB min., CMRR**
- **0.2 μV/°C Offset Drift**
- **10 to 1000 Gain Range**



GENERAL DESCRIPTION

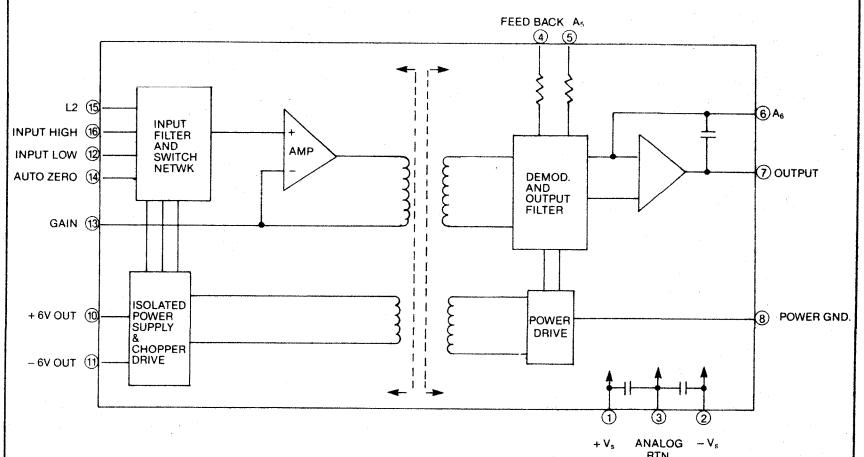
Datel-Intersil's AM-227 is a precision, low-cost, modular isolation amplifier designed specifically for applications involving the amplification of low-level, low frequency signals in the presence of high common mode interference. The ultra-low drift, high accuracy, and high CMRR make it possible to accurately amplify microvolt level signals with a user selectable gain range of 10 to 1000. Gain nonlinearity is specified as low as ±0.005% FSR maximum with gain selection accomplished through the addition of one external resistor.

The AM-227 offers excellent D.C. input characteristics including an unadjusted offset voltage of ± 150 μV, common mode rejection ratio of 166 dB minimum and common mode isolation voltage of 1000 VDC. Offset voltage drift is 0.5 μV/°C maximum and long term stability is typically as low as 2 μV/°C.

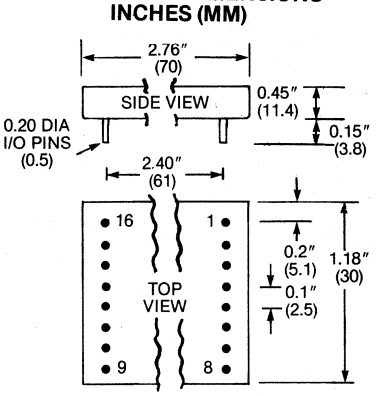
The AM-227 includes an input chopper-stabilized amplifier, power oscillator, demodulator, and 3 pole 60 dB/decade filtering. An output buffer amplifier provides ± 10V at ± 5 mA. The isolated ± 6V power outputs can be used in a simple open input indication network.

Its combination of high performance, low cost and small size make the AM-227 an excellent choice for applications involving thermocouple temperature measurements, remote data acquisition systems, strain gauge measurements, and precision telemetry systems.

Power requirement is ± 15 VDC. The AM-227 is packaged in a compact 2.8 × 1.2 × 0.45 inch, fully encapsulated module. Operation is specified over the industrial 0°C to +70°C temperature range.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V POWER IN	9	SHIELD
2	– 15V POWER IN	10	+6V OUT
3	ANALOG RTN	11	–6V OUT
4	FEEDBACK	12	INPUT LO
5	A5	13	GAIN
6	A6	14	AUT. ZER. RTN.
7	OUTPUT	15	L2
8	POWER GND	16	INPUT HIGH

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, AM-227
(Typical at +25°C, ±15 VDC supplies unless otherwise noted)

INPUT CHARACTERISTICS	
Linear Differential Input Voltage Range[1]	±10 mV to ±1V FS
Offset Voltage, R.T.I.[2], **G = 100**	±600 μV
G = 1000	±150 μV
Input Bias Current, max.	2 nA (0.5 nA typ.)
Input Resistance, Diff. Mode	100 MΩ
Input Impedance, Com. Mode	$10^{12}\Omega \| 80$pF
Diff. Mode	100 MΩ shunted by 22 kΩ in Series with 1.5 μF
Overload Input Impedance	22 kΩ
Common Mode Rejection Ratio, min.[3]	166 dB (176 dB typ.)
Common Mode Isolation Voltage, max.	1000 VDC, 750 VRMS
OUTPUT CHARACTERISTICS	
Output Voltage Range	±10V
Output Impedance, DC	0.1Ω
Output Load, max.	±5 mA and 500 pF
Output Short-Circuit Protection	Continuous to Ground
Output Chopper Noise[4]	1 mV P-P at approx. 10 kHz
PERFORMANCE	
Gain Range	10 to 1000
Gain Equation[6]	$G = 10^4/R_G$
Gain Nonlinearity, max., G = 10	±0.05% FSR
G = 50 – 500	±0.005% FSR
G = 1000	±0.01% FSR
Gain Tempco, max., G = 10 – 500	±20 ppm FSR/°C (±10 ppm FSR/°C typ.)
G = 1000	±30 ppm FSR/°C (±20 ppm FSR/°C typ.)
Input Offset Temp. Drift, R.T.I., max.	±0.5 μV/°C (0.2 μV/°C typ.)
Input Bias Current Temp. Drift	50 pA/°C
Warm-Up Drift[7], **R.T.I.**	<2μV
Long Term Drift, R.T.I.	1 μV/month, non-cumulative, 2 μV/year
Small Signal Bandwidth[8]	5Hz
Power Supply Sensitivity	±2 μV/% VV Supply
ISOLATED POWER SUPPLY OUTPUT	
Voltage, with respect to Input Low	±6 VDC nominal
Current, Full Load	±3 mA
Regulation, No load to Full Load	6%
Ripple	20 mV P-P @ 10 kHz
INPUT POWER REQUIREMENTS	
Positive Supply, No Load	±15V ±3% @ 5 mA
Negative Supply, No Load	–15V ±3% @ –3 mA
PHYSICAL ENVIRONMENTAL	
Operating Temperature Range[9]	0°C to +70°C
Storage Temperature Range	–55°C to +85°C
Relative Humidity	0 to 85%, non-condensing to +40°C
Package Size	1.2 x 2.8 x 0.5 in (30 x 70 x 12 mm)

NOTES:
1. Absolute maximum safe differential input voltage is: 120 V RMS, continuous.
2. Untrimmed, referred to input. Adjustable to zero.
3. At DC and from 50 to 800 Hz. G = 50 to 1000 with a 1 kΩ source imbalance.
4. 1 MHz bandwidth.
5. Non-inverting. Optimized for gains of 50 to 500.
6. See Technical Note 1.
7. 5 minutes.
8. 6 dB down at 5 Hz. See Technical Note 2 for information on the AM-227's internal filters.
9. It is possible to operate the AM-227 over the –25°C to +85°C temperature range with some degradation of performance.

TECHNICAL NOTES

1. The AM-227 gain may be set to any value from 10 to 1000 by connecting an external resistor (R_G) between the gain pin (Pin 13) and the input low pin (Pin 12). The gain is equal to $G = 10^4/R_G$ and untrimmed will be within ±3% of the calculated value. An RN55E resistor is recommended for temperature stability.

2. The AM-227 contains both input and output filters. The input filter is a one-pole RC (3 dB cut-off @ 5 Hz) and the output filter is a two-pole Butterworth (3 dB cut-off @ 5 Hz). Overall filtering is three-pole, 60 dB/decade roll-off (–60 dB @ 50 Hz).

3. For normal operation of the AM-227, connect the auto-zero pin (Pin 14) to the input low pin (Pin 12). A stable voltage source may be connected to the auto zero pin for applications requiring an input offset that exceeds the range of the offset adjust. Signals present on the input high pin (Pin 16) and auto zero pin (if used) are measured with respect to the input low pin. For optimum linearity, each signal must be within ±1V of input low.

4. The ±6V isolated power supply (Pins 10 & 11) outputs may be used for an open input indication network. This simple network consists of a resistor of approximately 180 MΩ connected between the input high pin (Pin 16) and either the +6V out pin (Pin 10) or the –6V out pin (Pin 11). This produces a bleeder current of approximately 20 nA through the input source circuitry. If the source is opened, this bleeder current will drive the AM-227 output into saturation.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	PRICE (1-9)
AM-227	0°C to +70°C	$

DATEL INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

NEW

DATEL

Four Channel, Isolated Signal Conditioning Modules SCM-100, SCM-101

FEATURES

- **Wide Input Span Range**
- **4 Channel Operation**
- **± 1000 VpK Isolation Voltage**
- **156 dB CMR**
- **± 0.02% Max. Nonlinearity**
- **± 1 μV/°C Input Offset Drift**
- **Low Cost**

GENERAL DESCRIPTION

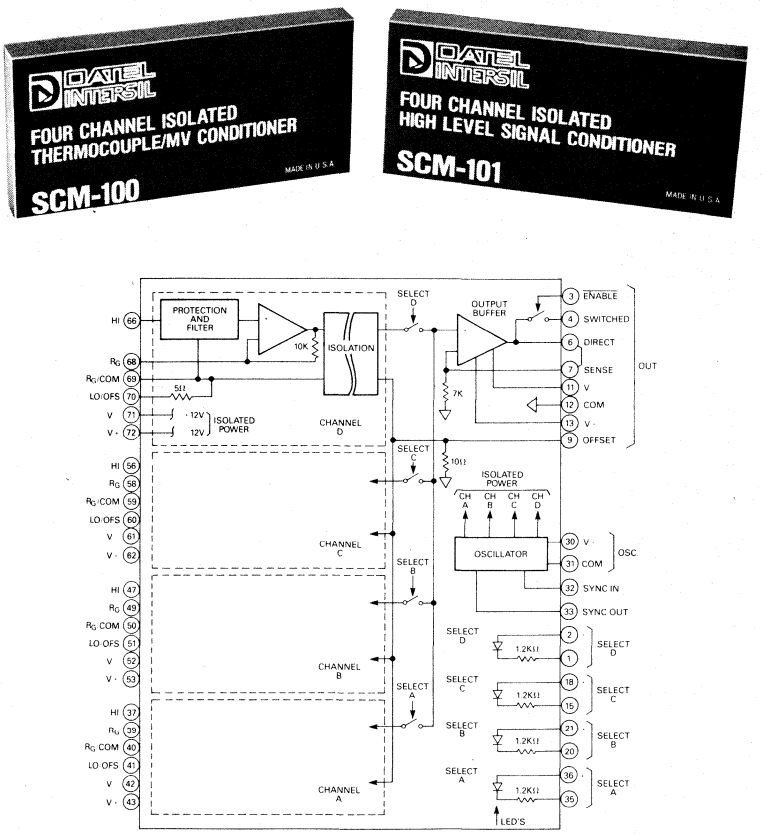
The SCM-100 and SCM-101 are low cost, high performance signal conditioning modules designed to interface with low-level thermocouple and high level analog input signals respectively. Each module is a functionally complete unit, consisting of four individually isolated input channels multiplexed into a single output amplifier. Common Mode isolation is ± 1000 Volts peak.

The SCM-100 is optimized for low level signal conditioning. An input span range of ± 5 mV to ± 100 mV and common mode rejection ratio of 156 dB minimum make this module an ideal choice for interfacing with thermocouples or strain gages, where low level signals require amplification in the presence of high common mode voltages. The SCM-100B features a maximum gain temperature coefficient of ± 25 ppm/°C and an input offset temperature drift of only ± 1 μV/°C maximum.

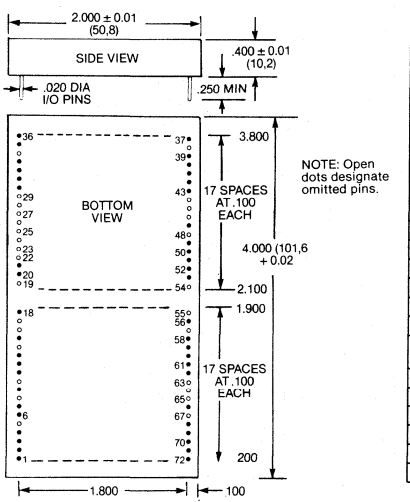
The SCM-101 is optimized for ± 50 mV to ± 5V or 4 to 20 mA input signals. Other specifications include a minimum common mode rejection ratio of 145 dB, a maximum gain temperature coefficient of ± 25 ppm of FS/°C and a maximum input offset voltage drift of ± 5 μV/°C.

All models feature a minimum channel scanning rate of 400 channels/second. Long term stability is specified at 1.5 μV/month and gain nonlinearity as low as ± 0.02% maximum. Their combination of functionally complete design, wide input range, high noise rejection, small size, and low cost make these devices an ideal choice for applications involving multi-channel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation.

Each device is packaged in a compact 2″ × 4″ × 0.4″ encapsulated module.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	– CHAN. D. SELECT	40	CHAN A RG/COMMON
2	+ CHAN D. SELECT	41	CHAN A LO/OFFSET
3	SWT. OUTPUT ENABLE	42	CHAN A (–) ISO. POWER
4	SWITCHED OUTPUT	43	CHAN A (+) ISO. POWER
6	DIRECT OUTPUT	47	CHAN B HI INPUT
7	OUTPUT SENSE	49	CHAN B RG
9	OUTPUT OFF ADJ	50	CHAN B RG/COMMON
11	OUTPUT POWER, – 15V	51	CHAN B LO/OFFSET
12	OUTPUT POWER, COMMON	52	CHAN B (–) ISO. POWER
13	OUTPUT POWER, + 15V	53	CHAN B (+) ISO. POWER
15	– CHAN C SELECT	56	CHAN C HI INPUT
18	+ CHAN C SELECT	58	CHAN RG
20	– CHAN B SELECT	59	CHAN C RG/COMMON
21	+ CHAN B SELECT	60	CHAN C LO/OFFSET
30	OSCILLATOR POWER, + Vs	61	CHAN C (–) ISO. POWER
31	OSCILLATOR POWER, COMMON	62	CHAN C (+) ISO. POWER
32	SYNC IN	66	CHAN D HI INPUT
33	SYNC OUT	68	CHAN D RG
35	– CHAN A SELECT	69	CHAN D RG/COMMON
36	+ CHAN A SELECT	70	CHAN D LO/OFFSET
37	CHAN A HI INPUT	71	CHAN D (–) ISO. POWER
39	CHAN A RG	72	CHAN D (+) ISO. POWER

DATEL-INTERSIL INC. 11 CABOT BOULEVARD MANSFIELD MA 02048/TEL (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SCM-100, SCM-101

Typical at +25°C ±15 VDC supplies, unless otherwise noted.

INPUT CHARACTERISTICS	SCM-100A	SCM-100B	SCM-101
Number of Channels	4	4	4
Input Span Range	±5 mV to ±100 mV	±5 mV to ±100 mV	±50 mV to ±5 V
Input Offset Voltage, max.[1]	±20 μV	±20 μV	±50 μV
Input Noise Voltage[2]	0.6 μV P-P	0.6 μV P-P	0.6 μV P-P
Input Bias Current, max.	+8 nA	+8 nA	+8 nA
Input Resistance			
Power On	100 MΩ	100 MΩ	100 MΩ
Power Off, min.	35 kΩ	35 kΩ	74 kΩ
Common Mode Voltage Range[3],			
ac, 60 Hz	750 Vrms	750 Vrms	750 Vrms
ac or dc, max.	±1000 V pk	±1000 V pk	±1000 V pk
Common Mode Rejection Ratio[4],			
min, G = 1000	156 dB	156 dB	------
G = 50	128 dB	128 dB	------
G = 100	------	------	145 dB
G = 1	------	------	110 dB
Normal Mode Input			
Without Damage 60 Hz	130 V rms	130 V rms	130 V rms
Normal Mode Rejection,			
min, G = 1000	55 dB	55 dB	------
G = 100	------	------	55 dB
Open Input Detection Time[5]			
G = 1000	6 nsec	6 nsec	------
G = 100	120 nsec	120 nsec	------
OUTPUT CHARACTERISTICS			
Output Voltage Swing[6]	±5V @ ±5 mA	±5V @ ±5 mA	±5V @ ±5 mA
Output Offset Voltage, max.[1]	±12 mV	±12 mV	±12 mV
Output Noise, dc — 100 kHz	0.8 mV P-P	0.8 mV P-P	0.8 mV P-P
Output Resistance			
Direct Output	0.1Ω	0.1Ω	0.1Ω
Switched Output	35Ω	35Ω	35Ω
PERFORMANCE			
Gain Equation	G = 1 + 10kΩ/R_G	G = 1 + 10kΩ/R_G	G = 1 + 10kΩ/R_G
Gain Nonlinearity[7],			
max, G = 1 to 100[8]	------	------	−0.2% min. to −0.55% max.
G = 50 to 300	±0.03%	±0.02%	------
Typ., G = 1000	±0.03%	±0.03%	------
Gain Temp. Coefficient, max.	±35 ppm/°C	±25 ppm/°C	±25 ppm/°C
Input Offset Temp. Drift, max.	±2.5 μV/°C	±1 μV/°C	±5 μV/°C
Input Offset Drift VS Time	±1.5 μV/month	±1.5 μV/month	±1.5 μV/month
Output Offset Temp. Drift, max.	±50 μV/°C	±50 μV/°C	±50 μV/°C
Total Offset Drift, RTI, max.	±(2.5 + 50/G) μV/°C	±(1 + 50/G) μV/°C	±(5 + 50/G) μV/°C
Channel Selection Time[9], max.	2.5 msec	2.5 msec	2.5 msec
Channel Scanning Speed, min.	400 chan/sec	400 chan/sec	400 chan/sec
Channel Select Input Reverse			
Voltage Rating, max.	3V	3V	3V
POWER REQUIREMENTS			
Analog Supply, rated value	±15 VDC ±10%		
Analog Supply Range, max.	±12 VDC to ±18 VDC		
Analog Supply Current, max.			
$\pm V_S$ = 15 VDC	±4 mA		
Oscillator Supply, rated value	+13.5 VDC to +24 VDC		
Oscillator Supply, absolute			
value max.	+26 VDC		
Oscillator Supply Current, max.			
$+V_{OS}$ = +15V	40 mA		
Power Supply Sensitivity, RTI			
Analog Supply	1 μV/V		
Oscillator Supply	1 μV/V		
PHYSICAL ENVIRONMENTAL			
Operating Temperature Range	0°C to +70°C		
Storage Temperature Range	−55°C to +85°C		
Relative Humidity[9]	0 to 85%		
Case Size	2" × 4" × 0.4" (50,8 × 101,6 × 10,2 mm)		

NOTES:
1. Adjustable to zero
2. R_S = 1 kΩ, 0.01 Hz to 100 Hz.
3. Channel to channel or channel to ground
4. $R_S \leq 100\Omega$, $f \geq 50$ Hz.
5. Response time can be reduced by addition of external resistors.
6. Short circuit protected.
7. Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line.
8. A negative gain error is purposely introduced to allow all channels to be matched at G = >1 by trimming the input gain. The gain is then set by the output gain adjustment.
9. To +0.01% full scale.

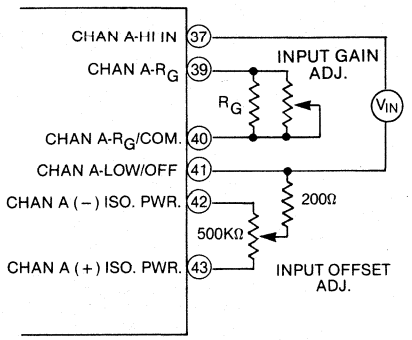
TECHNICAL NOTES

1. To minimize coupling between input and output, keep all leads associated with signals on the input as far as possible from leads associated with output signals. The use of a guard track on both sides of the board (see typical connection) may be helpful. The power supplies should be decoupled with tantalum capacitors mounted as close to the device as possible.
2. For lowest noise, the grounding scheme shown in the typical connection diagram should be used. To prevent power supply currents from flowing in the low lead of the signal output, the output signal common should be tied directly to the output power common pin (pin 12), with the power supply returns brought separately to pin 12.
3. When using an unregulated power source for the oscillator, a 0.1 μf capacitor should be connected directly from the output power common (pin 12) to the oscillator power common (pin 31). Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A one or two volt potential difference between the two power supply commons will not affect operation.
4. Channel selection is determined by the select inputs. Each select input consists of an LED in series with a resistor. Turning the LED on (± ≥2.5 mA) turns the channel on, and turning the LED off (± ≤50μA) turns the channel off. The easiest way to use the select inputs is to tie all the Select (+) inputs (pins 2, 18, 21 and 36) to +5V and drive the Select (−) inputs (pins 1, 15, 20 and 35) from TTL logic. Open-collector or totem-pole outputs can be used.

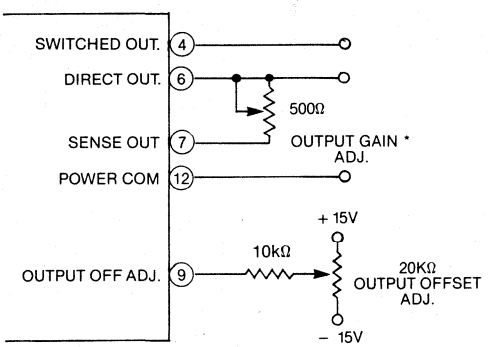
   With a +15V logic supply, a standard CMOS decoder or gate can supply enough current to drive the select inputs. At higher CMOS supply voltages, more current than the required 2.5 mA will flow into the select inputs. While this will not affect operation, it can be brought back to the minimum value if desired by putting a resistor in series with the decoder or gate output and the select (−) input. For 10V operation, a 2 kΩ resistor should be used and at 15V, a 2.9 kΩ.
5. The maximum reverse voltage applied to any select input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25 mA. Select inputs are isolated from all other circuits in the module and may be operated at up to ±50V with respect to output and power ground. Channels may be selected in any order with no restrictions on rate or duty cycle — except the 2.5 nS settling time for channel access. However, selecting two or more channels simultaneously for more than a few microseconds will result in very long settling times.
6. Output filtering is not required, in most applications, since the affect of the small carrier-related noise spikes on the output (<1mV P-P, 100 kHz B.W.) drops off rapidly as bandwidth decreases. To eliminate the carrier noise, a simple R-C filter (for example — 1 kΩ, 0.0047 μf) may be used at the output. Only one filter is required, even when using multiple modules, however, if the load to be driven has an input resistance of less than 10 MΩ, a buffer will be needed.
7. Output errors caused by differences in individual oscillator frequencies may occur in applications where multiple SCM-100/101's are used in close proximity or when system clock signals are present near the isolator. To eliminate these errors, multiple units may be synchronized by connecting the Sync Output (pin 33) of one module to the Sync Input (pin 32) of the adjacent module. The first module of a group may be synchronized to an external source via the SYNC IN (Pin 32). Sync wiring should be separated from analog signal runs to keep noise pickup at a minimum. (See External Syncronization) The frequency of the external Sync Source (if used) will have a slight effect on the gain and output offset of the device. Thus, any adjustments should be made with the modules synchronized.

TYPICAL CONNECTION AND CALIBRATION

INPUT OFFSET AND GAIN ADJUST



OUTPUT OFFSET AND GAIN ADJUST



TRIM POTS ARE 10 TURN.

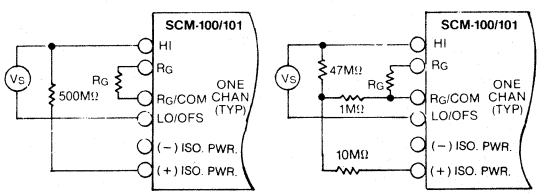
GAIN ADJUST RANGE SHOULD NOT EXCEED 10% TO MAINTAIN GAIN STABILITY

GAIN ADJUST — The gain of each channel is independently adjusted by an external gain resistor (R_G). A trimpot may be connected in parallel with R_G to trim out R_G's tolerance and the modules gain error. R_G should be chosen to give an untrimmed gain slightly less than the desired trimmed gain.

OFFSET ADJUST (optional) — The input offset of each channel may be fine adjusted with an external trimpot if required. This fine adjust has a limited range of ± 250 μV and can be used to adjust each channel for zero offset while operating at the desired gain. Since the range of this adjustment is so limited, it is recommended that the output offset be adjusted first. Output Offset Adjustment should be made as follows:

1. Select the desired channel.
2. Apply zero volts in and set for unity gain. (This can be done by disconnecting R_G.)
3. Set the OUTPUT OFFSET ADJUST for an output of 0V.

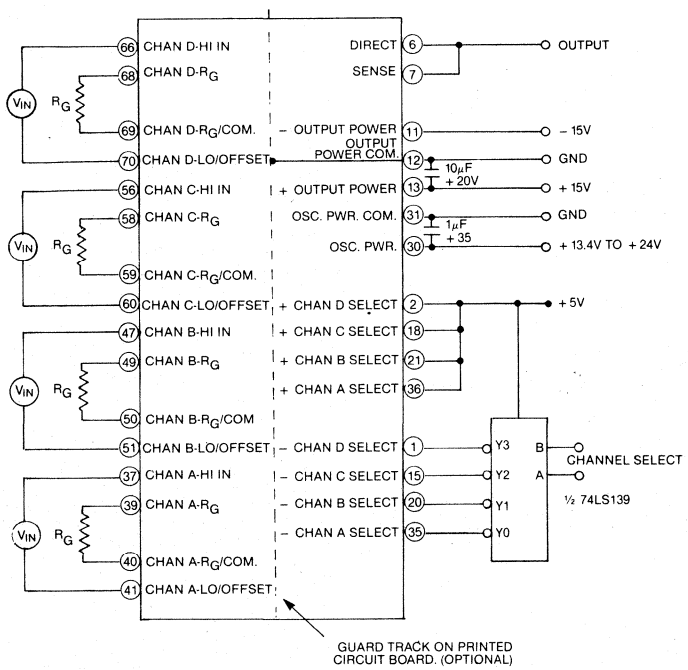
OPEN INPUT DETECTION



Since only a few nA of input bias current is available to charge the input filter, the response time for open input detection can be in the tens of seconds. Shorter response times and a positive overscale if required may be achieved with one of the above circuits which will augment or reverse the input bias current. Either circuit will supply a bias current of approximately 20 nA which may be used to aid or oppose the 3 nA supplied from the module. Circuit A has the advantage of simplicity, however, the high value resistor may not be readily available. Circuit B solves the problem at the expense of complexity. The component values may be varied to give an optimum trade of bias current for response time as required. The values shown will give a typical response time of 2 to 5 seconds.

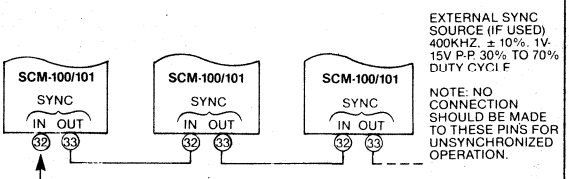
TYPICAL CONNECTION

SCM-100, SCM-101



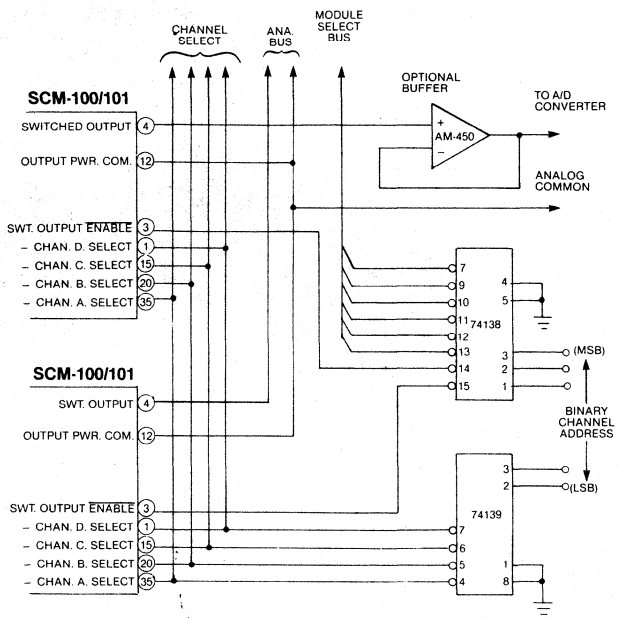
EXTERNAL SYNCHRONIZATION

(see Tech Note 7)



APPLICATIONS

EXPANSION TO 32 CHANNELS

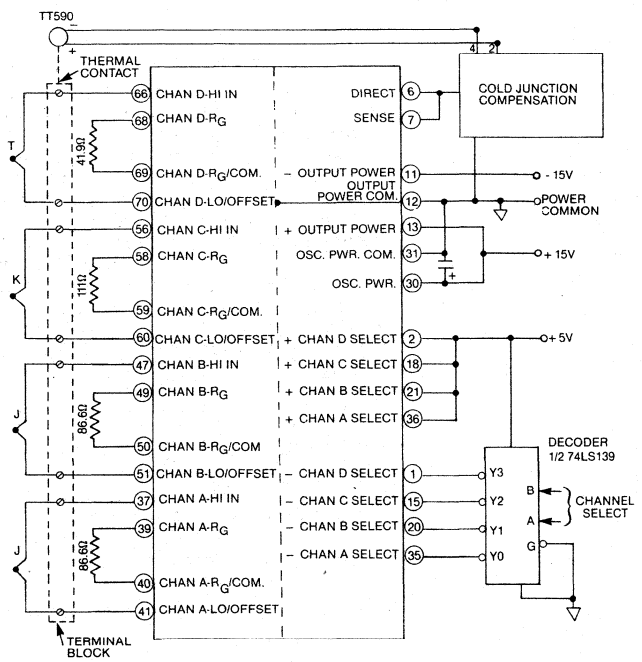


The SCM-100/101 are mainly used in Data Acquisition systems to maintain high system accuracy in electrically noisy industrial environments.

It is possible to operate up to sixteen modules in parallel giving 64 input channels. However, it will be necessary to divide the select inputs into several groups to avoid overloading the decoder.

The above diagram shows the SCM-100/101 expanded to 32 channels. The CHANNEL SELECT inputs are driven in parallel from a single 74139 decoder. Module selection is achieved by driving the enable inputs with a 74138 decoder. All + channel select pins are tied to +5V.

THERMOCOUPLE TEMPERATURE MEASUREMENT



In this application, the SCM-100 is set up as a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the module. Various thermocouple types are used, and the gain adjust pots on each channel have been selected to take the standard ANSI range for each thermocouple to a 5V output span. A universal cold junction compensator is used to compensate for the temperature of the reference junction which is formed where the thermocouple leads are terminated.

NEW

DATEL

Four Channel RTD, Strain Gage Signal Conditioning Modules SCM-102, SCM-103

PRELIMINARY

FEATURES

- **4 Channel Operation**
- **± 1 μV/°C Input Offset Drift**
- **± 0.01% Max. Nonlinearity**
- **3000 Chan./Sec Scanning Speed**
- **Low Cost**

GENERAL DESCRIPTION

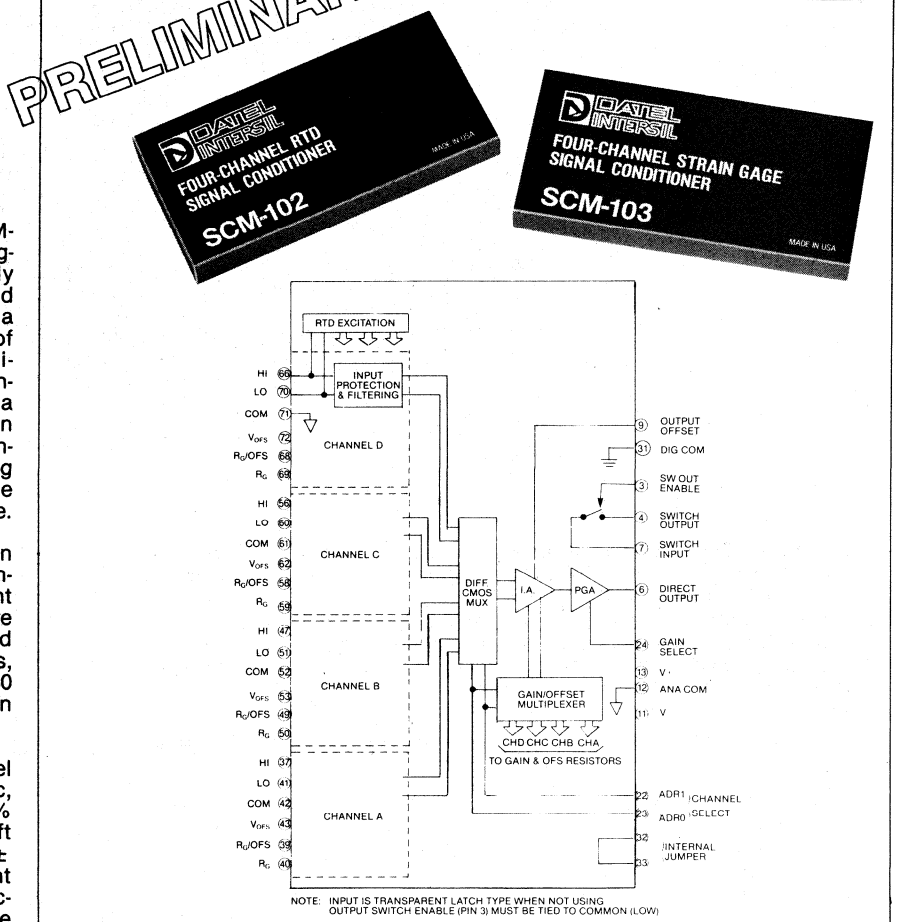
DATEL-INTERSIL's SCM-102 and SCM-103 are low-cost, high performance signal conditioning modules specifically designed to interface with RTD and strain gage sensors. Each module is a functionally complete unit consisting of four individual input channels multiplexed into a single low-drift instrumentation amplifier which is followed by a digitally controlled, programmable gain amplifier output stage. Each channel includes an input protection and filtering circuit to preserve signal integrity in the presence of series mode 50/60 Hz noise.

The SCM-102 is optimized to condition signals produced by RTD sensors and includes an internally selectable, constant current, excitation source and lead wire compensation. The SCM-103 is designed to interface with strain gage sensors, and features an input span range of ± 30 mV to ± 100 mV and a minimum common mode rejection ratio of 94 dB.

Both models feature a minimum channel scanning speed of 3000 channels/sec, 100 MΩ input resistance and ± 0.01% maximum nonlinearity. Total offset drift is ± 1 μV/°C, output voltage swing is ± 5V and the gain temperature coefficient is ± 25 ppm/°C. Gain and channel selection is accomplished by applying the proper binary code to the gain or channel select inputs. User selectable switched or direct outputs allow for the interconnection of multiple units when more than four channels is required.

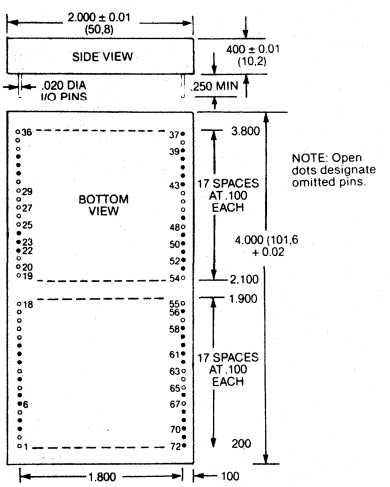
The low cost, functionally complete multichannel design of these modules make them an ideal choice for applications involving multi-channel data acquisition systems, computer interface systems and industrial process measurement and control.

Each device is packaged in a compact 2″ × 4″ × 0.4″ encapsulated module and operates over the industrial −25°C to +85°C temperature range.



NOTE: INPUT IS TRANSPARENT LATCH TYPE WHEN NOT USING OUTPUT SWITCH ENABLE (PIN 3) MUST BE TIED TO COMMON (LOW)

MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
3	SWT. OUTPUT ENABLE	43	CHAN A — Voff (+ 10V)
4	SWITCHED OUTPUT	47	CHAN B — HI INPUT
6	DIRECT OUTPUT	49	CHAN B — R_G/OFFSET
7	SWITCHED INPUT	50	CHAN B — R_G
9	OUTPUT OFFSET	51	CHAN B — LO INPUT
11	− 15V POWER	52	CHAN B — COMMON
12	ANALOG COMMON	53	CHAN B — Voff (+ 10V)
13	+ 15V POWER	56	CHAN C — HI INPUT
22	CHANNEL SELECT 1	58	CHAN C — R_G/OFFSET
23	CHANNEL SELECT 2	59	CHAN C — R_G
24	GAIN SELECT	60	CHAN C — LO INPUT
31	DIGITAL COMMON	61	CHAN C — COMMON
32	SYNC IN	62	CHAN C — Voff (+ 10V)
33	SYNC OUT	66	CHAN D — HI INPUT
37	CHAN A — HI INPUT	68	CHAN D — R_G/OFFSET
39	CHAN A — R_G/OFFSET	69	CHAN D — R_G
40	CHAN A — R_G	70	CHAN D — LO INPUT
41	CHAN A — LO INPUT	71	CHAN D — COMMON
42	CHAN A — COMMON	72	CHAN D — Voff (+ 10V)

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SPECIFICATIONS, SCM-102, SCM-103
Typical at +25°C, ±15 VDC Supplies, unless otherwise noted.

INPUT CHARACTERISTICS	SCM-102	SCM-103
Number of Channels	4	4
Input Span Range	25Ω to 175Ω and 0 to 350Ω	±30 mV to ±100 mV
Input Offset Voltage, Adj. to Zero	±150 μV	±150 μV
Channel to Channel Offset	±25 μV	±25 μV
Input Bias Current, max.	10 nA	10 nA
Input Noise Voltage, 0.01 Hz to 100 Hz[1]	1.5 μV P-P	1.5 μV P-P
Common Mode Voltage Range	———	6V
Common Mode Rejection Ratio, min[2]	———	94 dB
Normal Mode Rejection, 60 Hz	24 dB	24 dB
Maximum Safe Differential Input	130 V rms	130 V rms
Input Resistance	>100 MΩ	>100 MΩ
Load Resistance Effect	±0.03 deg/Ω	———
OUTPUT CHARACTERISTICS		
Output Voltage Swing	±5V @ 1mA	±5V @ 5 mA
Output Resistance;		
Direct Output	0.1Ω	0.1Ω
Switched Output	35Ω, +5%/°C	35Ω, +5%/°C
Maximum Switched Voltage	±9V[4]	±10V[3]
PERFORMANCE		
Gain Range[5], R_G = 945Ω	166.6 V/V or 50 V/V	166.6 V/V or 50 V/V
Gain Error, max., G = 50	±0.6%	±0.6%
G = 166.6	±0.8%	±0.8%
Gain Nonlinearity, max.	±0.01% of Span	±0.01% of Span
Transfer Function	Vout = [0.4 × 10^3 × (R_{RTD}) − 0.04] G	———
Gain Tempco[5]	±25 ppm/°C	±25 ppm/°C
Input Offset Temp.Drift,	0.015 deg./deg.	±1 μV/°C
Total Offset Temp. Drift, RTI	±1 μV/°C	±1 μV/°C
Channel Selection Time, max.	300 μsec	300 μsec
Channel Scanning Speed, min.	>3000 chan/sec	>3000 chan/sec
Input Settling Time, to 0.01% FS	0.4 sec.	0.4 sec.
Bandwidth	4 Hz	4 Hz
Sensor Excitation Level	0.4 mA ±1% (±1.7% max.)	———
Sensor Excitation Level Tempco	±10 ppm/°C	———
Power Supply Rejection	±0.02%/%V_S	±0.003%/%V_S
POWER REQUIREMENTS		
Analog Supply, Rated Value	±15 VDC ±5%	
Analog Supply Current, max., +15V	+35 mA	
−15V	−15 mA	
PHYSICAL ENVIRONMENTAL		
Specified Temperature Range	0°C to +70°C	
Operating Temperature Range	−25°C to +85°C	
Storage Temperature Range	−55°C to +85°C	
Case Size	2″ × 4″ × 0.4″ (50.8 × 101.6 × 10.2 mm)	

NOTES:
1. R_S = 1 kΩ
2. R_S − 1 kΩ, f = 60 Hz
3. R_L = 2 kΩ
4. No load
5. Gain range may be expanded by use of an external amplifier. Expanded gain range for both the SCM-102 and SCM-103 is 50 V/V to 1000 V/V.
6. Does not include effects of sensor excitation drift.
7. To 0.01% Full Scale.
8. Per channel.

TECHNICAL NOTES

1. Channel selection for the SCM-102/103 is accomplished by applying the proper binary code to the channel select inputs (Pins 22 and 23). Channels may be selected in any order, the only restriction being the 300 μsec channel selection settling time.
2. The SCM-102 and SCM-103 are precalibrated to provide gains of 50 V/V and 166.6 V/V. Gain selection is accomplished by applying the appropriate binary code to the gain select input (Pin 24). A logic high applied to Pin 24 gives a gain of 50 V/V while a logic low gives a gain of 166.6 V/V. A 200Ω potentiometer connected in series with an 845Ω resistor across the R_G pins of each channel will provide ±3% full scale span adjustment.
3. The gain range of the SCM-102 and SCM-103 may be expanded by the use of an external amplifier. A low-drift amplifier, such as DATEL-INTERSIL's AM-427 should be used to maintain signal integrity.
4. All unused inputs should be shorted to common.

ORDERING INFORMATION

MODEL NO.	INPUT	PRICE (1-9)
SCM-102	RTD	
SCM-103	Strain Gage	

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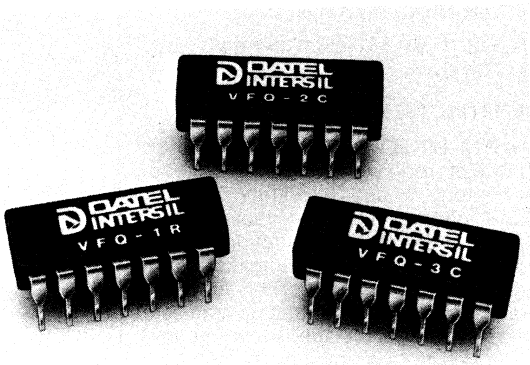
SPECIAL FUNCTION PRODUCTS

Special functions

DATEL-INTERSIL offers a line of products specifically designed to meet the needs of specialized applications. Included here is a complete family of low-cost voltage to frequency to voltage converters, a precision 2.455V bandgap voltage reference and a hybrid universal active filter.



MODEL	DESCRIPTION	NON-LINEARITY % OF F.S.	DRIFT	PACKAGE	TECH-NOLOGY	OPERATING TEMPERATURE RANGE (°C)	SEE PAGE
VFQ-1C	V/F, F/V Converter Operates to 100 kHz	0.05%	40 ppm/°C	14-pin DIP	Monolithic	0 to + 70	346
VFQ-1R		0.05%				− 25 to + 85	
VFQ-2C		0.01%				0 to + 70	
VFQ-3C		0.25%				0 to + 70	
VFV-10K	V/F, F/V Converters 10 kHz or 100 kHz Operation	0.005%	20 ppm/°C	2 × 2 × 0.375 in (51 × 51 × 10 mm)	Module	0 to + 70	—
VFV-100K		0.05%	100 ppm/°C				
VI-7660-1	CMOS voltage converter. Input Range of + 1.5V to + 100			TO-99	Monolithic	0° to + 70°C	350
VI-7660-2				8 Pin DIP			
VR-182A	2.455 V Precision Bandgap Voltage Reference	± 1.43%	100 ppm/°C	2-lead TO-18	Monolithic	0 to + 70	352
VR-182B			50 ppm/°C				
VR-182C			30 ppm/°C				
FLT-U2	Universal Active Filter	± 5%	0.01%/°C	16-pin DIP	Hybrid	0 to + 70	340
FLT-U2-M						− 55 to + 125	

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Microelectronic Universal Active Filter FLT-U2

FEATURES

- **State Variable Filter**
- **LP, BP, or HP Functions**
- **2 Pole Response**
- **Low Noise Op Amps**
- **−55°C to +125°C Operation**
- **Low Cost**

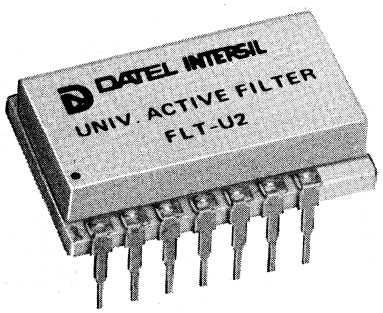
GENERAL DESCRIPTION

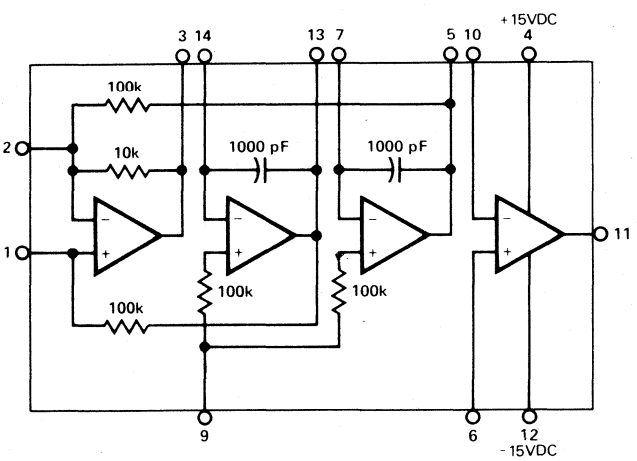
The FLT-U2 is a universal active filter manufactured with thick-film hybrid technology. It uses the state variable active filter principle to implement a second order transfer function. Three committed operational amplifiers are used for the second order function while a fourth uncommitted op amp can be used as a gain stage, summing amplifier, buffer amplifier, or to add another independent real pole.

Two-pole lowpass, bandpass, and highpass output functions are available simultaneously from three different outputs, and notch and allpass functions are available by combining these outputs in the uncommitted op amp. To realize higher order filters, several FLT-U2's can be cascaded. Q range is from 0.1 to 1,000 and resonant frequency range is 0.001 Hz to 200 kHz. Frequency stability is .01%/°C and resonant frequency accuracy is within ±5% of calculated values. Frequency tuning is done by two external resistors and Q tuning by a third external resistor. For resonant frequencies below 50 Hz two external tuning capacitors must be added. Exact tuning of the resonant frequency is done by varying one of the resistors around its calculated value.

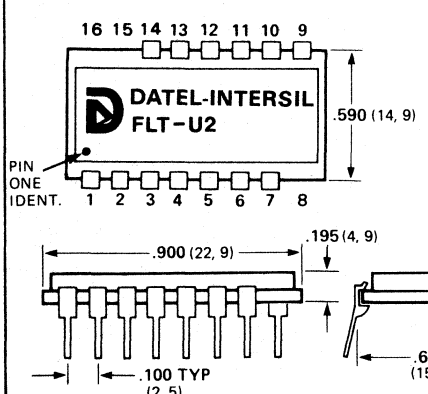
The internal op amps in the FLT-U2 have 3 MHz gain bandwidth products and a wideband input noise specification of only 10nV/√Hz. This results in considerably improved operation over most other competitive active filters which employ lower performance amplifiers. By proper selection of external components any of the popular filter types such as Butterworth, Bessel, Chebyshev, or Elliptic may be designed. Applications include audio, tone signalling, sonar, data acquisition, and feedback control systems.

Two models are available for operation over the commercial, 0°C to +70°C, and military, −55°C to +125°C, temperature ranges.

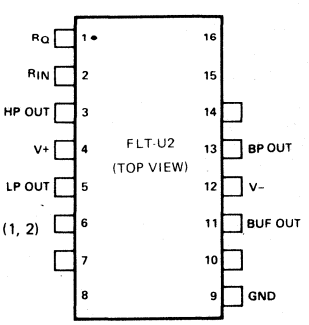




MECHANICAL DIMENSIONS INCHES (MM)



CONNECTIONS DIAGRAM



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SPECIFICATIONS, FLT-U2

Typical at 25°C, ±15V supplies, unless otherwise stated

FILTER CHARACTERISTICS

Frequency Range[1]	0.001 Hz to 200 kHz
Q Range[1]	0.1 to 1,000
f_0 Accuracy	±5%
f_0 Temperature Coefficient	0.01%/°C
Voltage Gain[1]	0.1 to 1,000

AMPLIFIER CHARACTERISTICS

Input Offset Voltage	0.5 mV typ., 6 mV max.
Input Bias Current	40 nA typ., 500 nA max.
Input Offset Current	5 nA typ., 200 nA max.
Input Impedance	5 Megohms
Input Com. Mode Voltage Range	±12V min.
Input Voltage Noise, wideband	10nV/$\sqrt{Hz}$
Output Voltage Range	±10V min.
Output Current	±5mA min.
Open Loop Voltage Gain	300,000
Common Mode Rejection Ratio	100 dB
Power Supply Rejection	10 μV/V
Unity Gain Bandwidth	3 MHz
Slew Rate	1 V/μsec.

POWER SUPPLY REQUIREMENT

Voltage, rated performance	±15 VDC
Voltage Range, operating	±5V to ±18V
Quiescent Current	11.5 mA max.

PHYSICAL-ENVIRONMENTAL

OPERATING TEMPERATURE RANGE	
FLT-U2	0°C to +70°C
FLT-U2M	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Case	Ceramic 16-pin DIP (double-spaced)

NOTE: 1. $f_0Q \leq 2 \times 10^6$

ORDERING INFORMATION

MODEL	OPERATING TEMP RANGE	PRICE (1-24)
FLT-U2	0°C to +70°C	
FLT-U2M	−55°C to +125°C	

TECHNICAL NOTES

1. The FLT-U2 has simultaneous lowpass, bandpass, and highpass output functions. The chosen output for a particular function will be at unity gain based on Tables II and III. This means that the other two unused outputs will be at other gain levels. The gain of the lowpass output is always 10 dB higher than the gain of the bandpass output and 20 dB higher than the gain of the highpass output.

2. When tuning the filter and checking it over its frequency range, the outputs should be checked with a scope to make sure there is no waveform clipping present, as this will affect the operation of the filter. In particular the lowpass output should be checked since its gain is the highest.

3. f_1, the center frequency for bandpass and the cutoff frequency for lowpass or highpass, should be checked at the bandpass output. Here the peaking frequency can easily be determined for high Q filters and the 0° or 180° phase frequency can easily be determined for low Q filters (depending on whether inverting or noninverting).

4. Tuning resistors should be 1% metal film resistors with 100 ppm/°C temperature stability or better for best performance. Likewise external tuning capacitors should be NPO ceramic or other stable capacitor types.

THEORY OF OPERATION

The FLT-U2 block diagram is shown in Figure 1. This is a second order state-variable filter using three operational amplifiers. Lowpass, bandpass, and highpass transfer functions are simultaneously produced at its three output terminals. These three transfer functions are characterized by the following second order equations:

$$H(s) = \frac{K_1}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad \text{LOWPASS}$$

$$H(s) = \frac{K_2 S}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad \text{BANDPASS}$$

$$H(s) = \frac{K_3 S^2}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad \text{HIGHPASS}$$

where K_1, K_2, and K_3 are arbitrary gain constants.

A second order system is characterized by the location of its poles in the s-plane as shown in Figure 2. The natural radian frequency of this system is ω_0. In Hertz this is $f_0 = \frac{\omega_0}{2\pi}$.

THEORY OF OPERATION, (Cont'd)

The resonant radian frequency of the circuit is different from the natural radian frequency and is:

$$\omega_1 = \omega_0 \sin \phi = \sqrt{\omega_0^2 - \sigma_1^2}$$

The damping factor d determines the amount of peaking in the filter frequency response and is defined as:

$$d = \cos \phi$$

The point at which the peaking becomes zero is called "critical damping" and is $d = \sqrt{2}/2$.

Q is found from d and is a measure of the sharpness of the resonance of the peaking:

$$Q = \frac{1}{2d}$$

$$\text{Also, } Q = \frac{f_0}{-3\text{ dB Bandwidth}} = \frac{\omega_0}{2\sigma_1}$$

For high Q filters the natural frequency and resonant frequency are approximately equal:

$$\omega_1 \simeq \omega_0 \text{ or } f_1 \simeq f_0$$

This is true since $\omega_1 = \omega_0 \sin \phi$ and $\sin \phi \simeq 1$ as the poles move close to the $j\omega$ axis in the s-plane.

For high Q's ($Q > 1$) we therefore have for the second order filter:

$f_0 \simeq$ Bandpass center frequency
$\simeq$ Lowpass corner frequency
$\simeq$ Highpass corner frequency

In the simplified tuning procedure which follows, the tuning is accomplished by independently setting the natural frequency and Q of the filter. This is done most simply by assuming unity gain for the output of the desired filter function. Unity gain means a gain of one (±) at DC for lowpass, at center frequency for bandpass, and at high frequency ($f >> f_0$) for highpass. Unity gain does not apply to all outputs simultaneously but only to the chosen output based on the component values given in the tables. Figure 3 shows the relative gains of the three simultaneous outputs assuming the bandpass gain is set to unity. Note that lowpass gain is always 10 dB higher than bandpass gain and highpass gain is always 10 dB lower than bandpass gain.

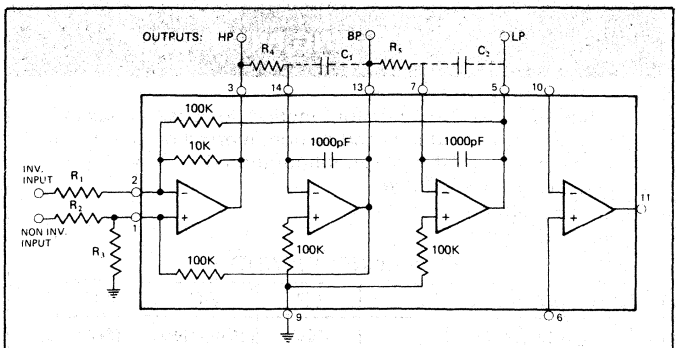


Figure 1.
FLT-U2 Block Diagram

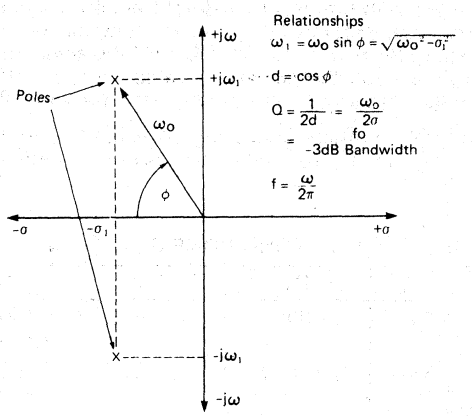


Figure 2.
S-Plane Diagram

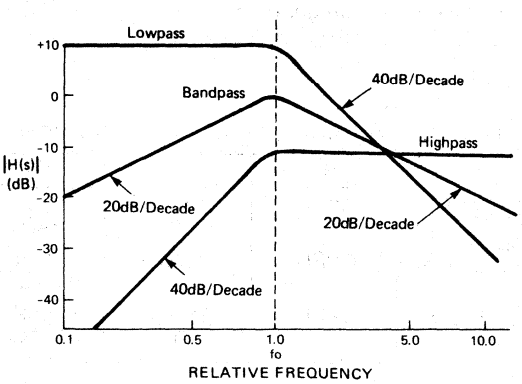


Figure 3.
Relative Gains of Simultaneous Outputs, Q=1

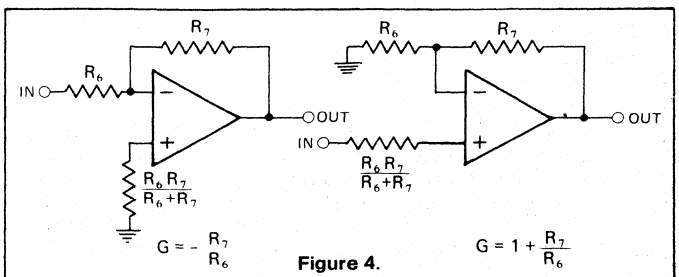


Figure 4.
Uncommitted Op Amp Gain Configurations

SIMPLIFIED TUNING PROCEDURE

1. Select the desired transfer function (lowpass, bandpass, or highpass) and inverted or noninverted output. From this determine the filter configuration (inverting or noninverting) using Table I.

TABLE I FILTER CONFIGURATION

	LP	BP	HP
INVERTING INPUT	INV.	NON-INV	INV
NONINVERTING INPUT	NON-INV.	INV	NON-INV

2. Starting with the desired natural frequency and Q (determined from the filter transfer function or s-plane diagram), compute f_0Q. For $f_0Q>10^4$ the actual realized Q will exceed the calculated value. At $f_0Q = 10^4$ the increase is about 1% and at $f_0Q = 10^5$ it is about 20%

3. **Inverting Configuration.** Using the value of Q from Step 2 find R_1 and R_3 from Table II. R_2 is open, or infinite.

TABLE II INVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	100K	OPEN	$\frac{100K}{3.80\ Q-1}$
BANDPASS	Q × 31.6K	OPEN	$\frac{100K}{3.48Q}$
HIGHPASS	10K	OPEN	$\frac{100K}{6.64Q-1}$

4. **Noninverting Configuration.** Using the value of Q from Step 2 find R_2 and R_3 from Table III. R_1 is open, or infinite.

TABLE III NONINVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	OPEN	$\frac{316K}{Q}$	$\frac{100K}{3.16Q-1}$
BANDPASS	OPEN	100K	$\frac{100K}{3.48Q-1}$
HIGHPASS	OPEN	$\frac{31.6K}{Q}$	$\frac{100K}{0.316Q-1}$

5. Using the value of f_0 from Step 2, set the natural frequency of the filter by finding R_4 and R_5 from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{f_0}$$

where R_4 and R_5 are in ohms and f_0 is in Hertz. The natural frequency varies as $\sqrt{R_4R_5}$ and therefore one value may be increased and the other decreased and the natural frequency will be constant if the geometric mean is constant. To maintain constant bandwidth at the bandpass output while varying center frequency, fix R_4 and vary R_5.

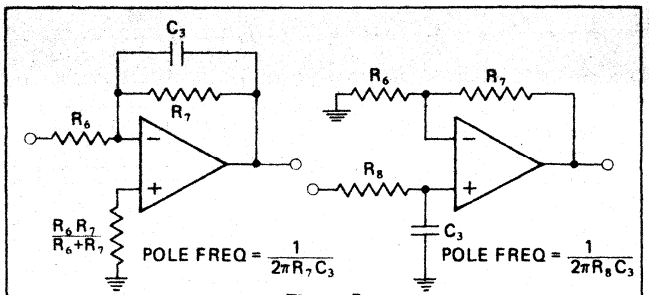


Figure 5.
Using the Uncommitted Op Amp to Add a Real Axis Pole

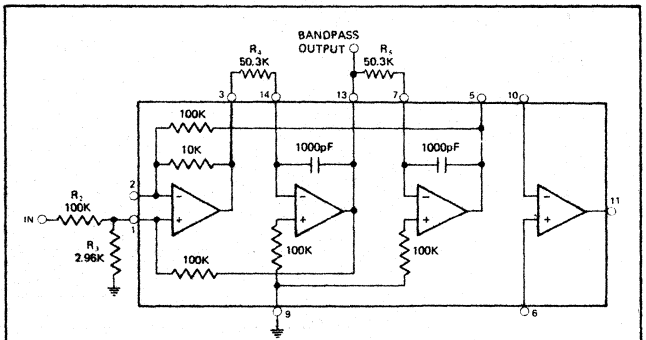


Figure 6.
Bandpass Filter Example

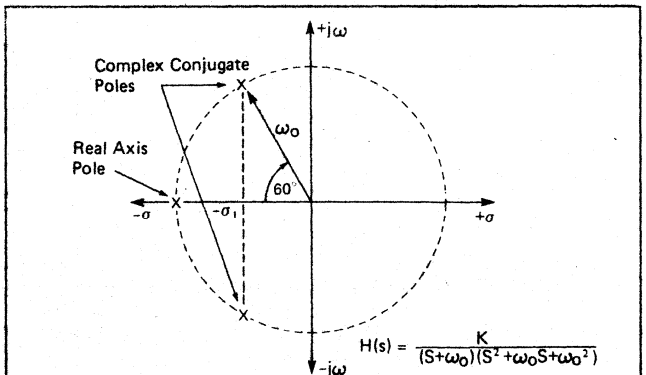


Figure 7.
S-Plane Diagram of 3-Pole Butterworth Lowpass Filter

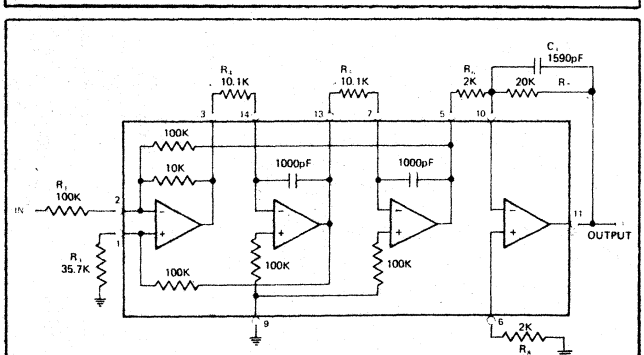


Figure 8.
Three Pole Butterworth Low Pass Filter Example

SIMPLIFIED TUNING PROCEDURE,(Cont'd)

6. For f_0 <50 Hz the internal 1000pF capacitors should be shunted with external capacitors across pins 5 & 7 and 13 & 14. If equal value capacitors are used, R_4 and R_5 are then computed from:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0 C} \text{ (C in pF)}$$

For unequal value capacitors this becomes:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0 \sqrt{C_1 C_2}} \text{ } (C_1C_2 \text{ in pF})$$

In both cases the capacitance is the sum of the external values and the internal 1000 pF values.

7. This procedure is based on unity gain output for the desired function. For additional gain, the fourth uncommitted operational amplifier should be used as an inverting or noninverting gain stage following the selected output. See Figure 4. A third pole on the real axis of the s-plane may also be added to the transfer function by adding a capacitor to the gain stage as shown in Figure 5.

FILTER DESIGN EXAMPLES

Bandpass Filter With 1kHz Center Frequency Q = 10, and Inverted Output

1. From Table I the noninverting configuration is chosen to realize an inverted bandpass output. $f_0Q = 10^4$ which means the realized Q will be about 1% higher than calculated.

2. From Table III, using Q = 10, we find:

R_1 = open
R_2 = 100K ohms
$R_3 = \frac{100K}{3.48Q-1} = \frac{100K}{33.8} = 2.96K$ ohms

3. Using f_0 of 1 kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{1000} = 50.3K \text{ ohms}$$

4. This completes the filter design which is shown in Figure 6. To choose the nearest 1% standard value resistors either 49.9K or 51.1K ohms could be used; likewise one value of 49.9K and one of 51.1K could be used giving the geometric mean of $\sqrt{R_4R_5} = \sqrt{49.9K \times 51.1K} = 50.5K$ which is even closer. But due to the filter ±5% frequency tolerance it may be better to hold R_4 constant while varying R_5 to tune it exactly.

Three-Pole Noninverting Butterworth Low Pass Filter With DC Gain Of 10 And Cutoff Frequency Of 5 kHz.

The s-plane diagram of the 3-pole Butterworth filter is shown in Figure 7. We will use a second order filter to realize the two complex conjugate poles and the uncommitted op amp to provide the third real axis pole and a DC gain of 10.

1. From Table I, the noninverting filter configuration would normally be used to give a noninverting low pass output.

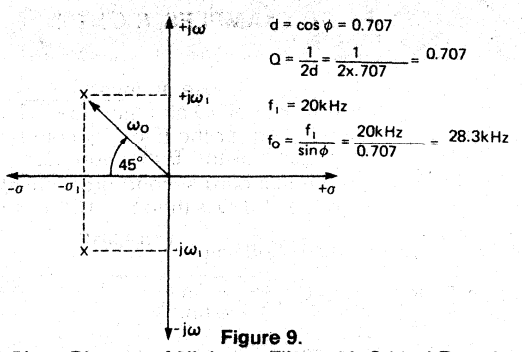


Figure 9.
S-Plane Diagram of Highpass Filter with Critical Damping

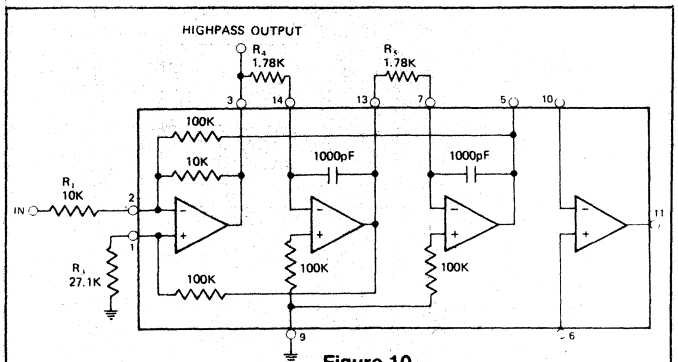


Figure 10.
Highpass Filter Example

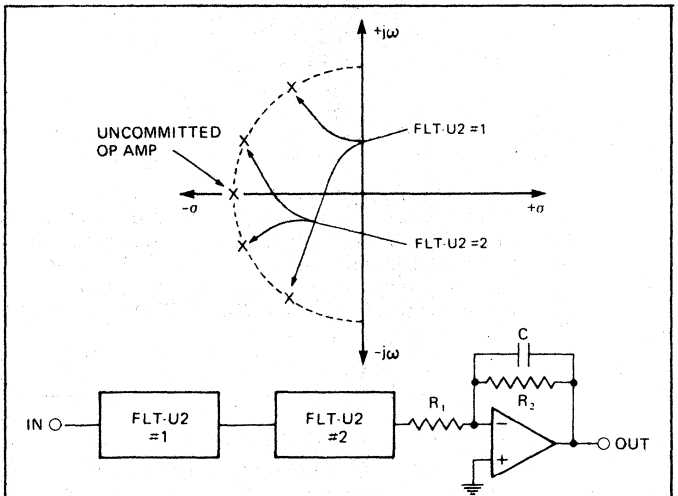


Figure 11.
Realization of a Complex Multipole Filter

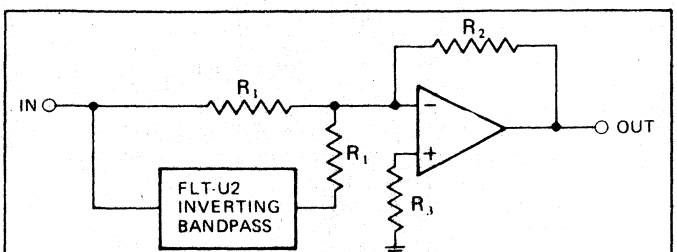


Figure 12.
Realization of Notch Filter

FILTER DESIGN EXAMPLES, (CONT'D)

In this case, however, we choose an inverting uncommitted op amp with a gain of 10 and therefore we use the inverting configuration for the filter. By comparing the second order portion of the Butterworth function $S^2 + \omega_0 S + \omega_0^2$ to the standard second order function $S^2 + \frac{\omega_0}{Q} S + \omega_0^2$ we find $Q = 1$. $f_0 Q$ is then 5×10^3 so that Q will not exceed its specified value.

2. From Table II, using Q = 1, we find:

$$R_1 = 100K \text{ ohms}$$
$$R_2 = \text{open}$$
$$R_3 = \frac{100K}{3.80Q-1} = 35.7K \text{ ohms}$$

3. Using f_0 of 5 kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{5000} = 10.1K \text{ ohms}$$

4. For the uncommitted output amplifier, a gain of −10 is required. This defines $R_7/R_6 = 10$ and we arbitrarily choose $R_6 = 2K$, $R_7 = 20$ K ohms.

5. The final step is to realize the real axis pole of the Butterworth filter. This pole is at 5 kHz and is set by using capacitor C_3 across the feedback resistor R_7:

$$C_3 = \frac{1}{2\pi f R_7} = \frac{1}{6.28 \times 5 \times 10^3 \times 20 \times 10^3} = 1590 \text{ pF}$$

6. This completes the 3-pole Butterworth filter which is shown in Figure 8.

Highpass Filter with Gain of −1, 20 kHz Cutoff Frequency, and Critical Damping

1. From Table I the inverting configuration must be used to realize a highpass gain of −1. An s-plane diagram of this function is shown in Figure 9. Critical damping requires the pole positions to be on a line 45° with respect to the real axis and this results in no frequency peaking. The damping factor d is:

$$d = \cos\phi = \cos 45^\circ = 0.707$$

and

$$Q = \frac{1}{2d} = \frac{1}{2(.707)} = 0.707$$

Because this is a low Q system the natural frequency will not be the same as the highpass cutoff frequency f_1. From Figure 9:

$$f_0 = \frac{f_1}{\cos\phi} = \frac{20 \text{ kHz}}{0.707} = 28.3 \text{ kHz}$$

Then $f_0 Q = 0.707 \times 28.3 \times 10^3 = 2 \times 10^4$ and the Q will exceed its desired value by slightly over 1%.

2. From Table II, using Q = 0.707 we find:

$$R_1 = 10K \text{ ohms}$$
$$R_2 = \text{open}$$
$$R_3 = \frac{100K}{6.64Q-1} = \frac{100K}{3.69} = 27.1K \text{ ohms}$$

3. Using $f_0 = 28.3$ kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{28.3 \times 10^3} = 1.78K \text{ ohms}$$

4. This completes the highpass filter design which is shown in Figure 10. When using this filter, care should be exercised so that clipping does not occur in the filter due to excessive input levels. If clipping occurs, the filter will not operate properly. Clipping will first occur at the lowpass output around f_0 since its gain is 20 dB higher than the highpass output. The signal level should be reduced so that clipping does not occur anywhere in the frequency range used. If higher signal level is required, the highpass output should be amplified by a gain stage using the uncommitted op amp.

ADVANCED FILTERS

All of the common filter types can be realized by using cascaded FLT-U2 stages. This includes multi-pole Butterworth, Bessel, Chebyshev, and Elliptic types. The basic procedure is to implement each pole pair with a single FLT-U2 and cascade enough units to realize all poles. A real axis pole is implemented by an uncommitted op amp. stage. Each stage should be separately tuned with an oscillator and scope and then the stages connected together and checked. See Figure 11.

A notch filter can be constructed in several ways. The first way is to use the FLT-U2 as an inverting bandpass filter and sum the output of the filter with the input signal by means of the uncommitted op amp. This produces a net subtraction at the center frequency of the bandpass which produces a null at the output of the amplifier. (See Figure 12.) Likewise lowpass and highpass outputs (which are always in phase) can be subtracted from each other with an external op amp. The highpass output must have some gain added to it, however, so that its gain is equal to that of the lowpass output. A third method is to use two separate FLT-U2's, one as a two-pole lowpass filter and the other as a two-pole highpass filter. Again the outputs are subtracted in an op amp. This method permits independent tuning of the two sections to get the best null response.

Further discussion of filter designs is beyond the scope of this data sheet and the user is referred to the various texts on filter design, some of which are listed below.

Estep, G.J., *The State Variable Active Filter Configuration Handbook*, 2nd Edition, Agoura, Ca., 1974.

Reference Data for Radio Engineers, Howard W. Sams & Co. Inc., 5th Edition.

Christian, E., and Eisenmann, E., *Filter Design Tables and Graphs*. McGraw-Hill Book Co., 1974.

Low Cost, Monolithic V/F Converters Models VFQ-1, VFQ-2, VFQ-3

FEATURES

- **10 kHz to 100 kHz FS**
- **0.01% Max. Linearity at 10 kHz (VFQ-2)**
- **Single or Dual Supply Operation**
- **Open Collector Output**
- **Pulse and Square Wave Outputs**
- **Operates as V/F or F/V**

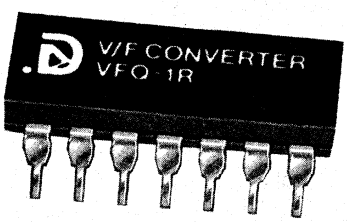
GENERAL DESCRIPTION

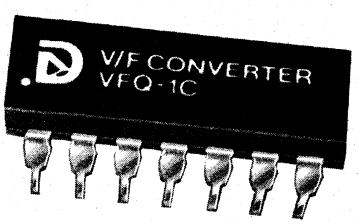
Datel-Intersil's VFQ series is a family of low cost monolithic voltage to frequency converters combining bipolar and CMOS technologies. These devices accept a positive analog input current and produce an output pulse train with a frequency linearly proportional to an input current. The full scale output pulse rate can be set from 10 kHz to 100 kHz by means of two external capacitors.

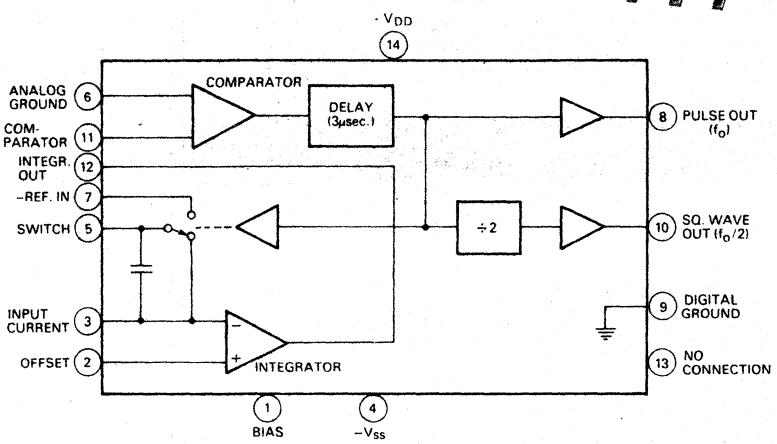
Linearities are specified for both 10 kHz and 100 kHz full scale outputs. The maximum linearity, at 10 kHz, of the VFQ-1 is 0.05%, while the VFQ-2 has a maximum of 0.01%, and the VFQ-3 has a 0.25% maximum. The linearity holds over the full output range of zero to full scale.

The internal circuitry of these converters includes an operational integrator, a comparator, digital delay circuit, single-pole double-throw electronic switch, a start circuit, a divide by two circuit, and two output driver circuits. Operation is based on the well-known charge balancing integrator principle. The two outputs are open collector NPN which can sink up to 10 mA and give a Logic HI output up to + 18 volts. In normal operation these devices require only five external components and a reference. If the zeroing adjustment is used, a trimming potentiometer and two more resistors are required. The VFQ series can be operated from dual ±4 to ±7.5V supplies or from a single + 10V to + 15V supply. They may also be operated as frequency to voltage converters.

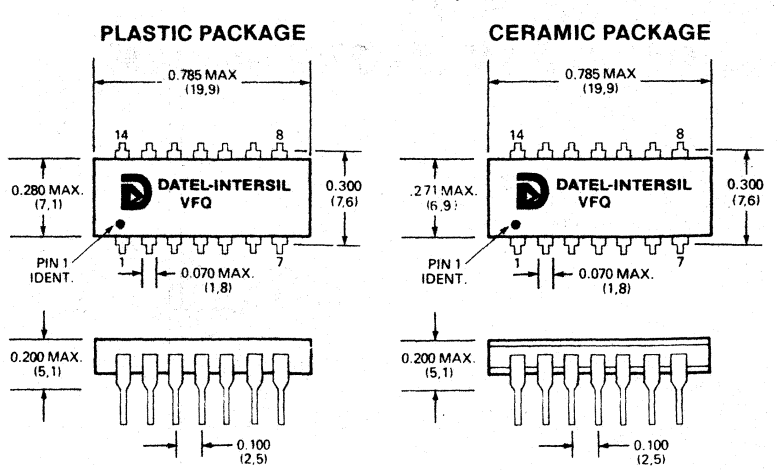
Each model is available in a 14 pin Plastic DIP for 0°C to + 70°C operation, with the VFQ-1 also available in a 14 pin Ceramic DIP for – 25°C to + 85°C operation.







MECHANICAL DIMENSIONS INCHES (MM)



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/ TEL.(617)339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, VFQ SERIES
(Typical at 25°C, ± 5V supplies, – 5V ref., unless otherwise noted.)

	VFQ-1	VFQ-2	VFQ-3
MAXIMUM RATINGS			
Supply Voltage, pin 4 to pin 14	18 Volts	*	*
Input Current, pin 3	± 10 mA	*	*
Output Voltage, pins 8 to 10	+ 25 Volts	*	*
Reference (pin 7) to $-V_{SS}$	± 1.5 Volts	*	*
INPUTS			
Input Current Range	0 to 10μA	*	*
Input Current Overrange, max.	+ 50 μA	*	*
Input Offset Voltage, max.[1]	± 50 mV	± 50 mV	± 100 mV
Reference Input	Negative Voltage Within ± 1.5V of negative supply		
OUTPUTS			
Type Outputs	Open Collector NPN		
Pulse Output, pin 8	Negative Going, 3 μsec pulses at f_o		
Square Wave Output, pin 10	Square Wave at $f_o/2$		
Output Logic Levels	V_{OUT}("0") ≤ + 0.4V @ – 10mA V_{OUT}("1") = $+V_{DD}$		
PERFORMANCE			
Linearity, 10 kHz Full Scale, max.	0.05%	0.01%	0.25%
Linearity, 100 kHz Full Scale, max.	0.25%	0.08%	0.5%
Gain Tempco, max.	40 ppm/°C	40 ppm/°C	100 ppm/°C
Zero Tempco, max.	50 μV/°C	50 μV/°C	100 μV/°C
Full Scale Accuracy, before trim	± 10%	*	*
Output Settling Time, 0.01%	2 Pulses of New Frequency		
SPECIFICATIONS AS F/V			
Nonlinearity, max.[2]	0.05%	0.02%	0.25%
Input Frequency Range	10 Hz to 100kHz	*	*
Input Voltage, minimum	± 0.4V	*	*
Input Voltage, maximum	– 2V to $+V_{DD}$	*	*
Input Pulse Width, Negative pulse, min.	0.5 μsec	*	*
Input Pulse Width, Positive pulse, min.	5.0 μsec	*	*
Output Voltage Range[3]	0V to ($+V_{DD}$ – 1)	*	*
Output Load, min.	2 kΩ		
POWER REQUIREMENT			
Positive Supply (pin 14)	+ 4.0V to + 7.5V		
Negative Supply (pin 4)	– 4.0V to – 7.5V		
Quiescent Current, max.[4]			
VFQ-1C, 2C	± 4 mA		
VFQ-1R	± 6 mA		
VFQ-3C	± 10 mA		
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range:			
Suffix C	0°C to + 70°C		
Suffix R	– 25°C to + 85°C		
Storage Temperature Range	– 65°C to + 150°C		
Package, C Suffix	14 pin Plastic DIP		
Package, R Suffix	14 pin Ceramic DIP		

*Specifications same as VFQ-1.

NOTES:
1. Before Trimming, $I_{IN} = 0$.
2. 10 Hz to 100 kHz
3. $R_L \geq 2\ k\Omega$
4. $V_{IN} = -0.1V$

TECHNICAL NOTES

1. To calibrate the VFQ as a V/F converter, connect as shown in the diagrams. Connect a precision voltage source (such as Datel-Intersil DVC-8500) to the input resistor. Connect a 5 digit counter, with time base set to one second, to the output (pin 8).
   Zero. Set the voltage reference to + 0.01V and adjust the zero adjust potentiometer for an output frequency of 10 Hz (for 10 kHz FS) or 100 Hz (for 100 kHz FS).
   Gain. Assuming the 10V FS input, set the voltage reference to + 10.000V and trim the value of R1 to give an output frequency of 10,000 Hz (for 10kHz FS) or 100,000 Hz (for 100 kHz FS).
2. The two outputs (pins 8 and 10) are open collector NPN transistors for easy interfacing to a variety of standard logic circuits. A pull-up resistor must be used as shown in the diagrams. The resistor may be tied to any voltage up to + 18V, which can be separate from + Vdd.
3. Note that the negative reference voltage must be within ± 1.5V of the negative supply (– Vss). For a given full scale output frequency the value of C_2 is dependent on the negative reference voltage.
4. Note the min-max waveform requirements for the input when using the VFQ as a frequency to voltage converter. See "Input Waveform Limits" diagram. The minimum ± 0.4V must be observed as well as the minimum widths for both positive and negative going portions of the waveform. If the input waveform exceeds the maximum amplitude limits, an input resistor and back-to-back clamping diodes should be used as shown in the connection diagram.
5. For F/V operation, the input signal must cross through zero in order to trip the comparator. In order to overcome the hysteresis the amplitude must be greater than ± 200mV. If only a unipolar input signal (F_{in}) is available, it is recommended that either an offset circuit using resistors be used or that the signal be coupled in via a capacitor.

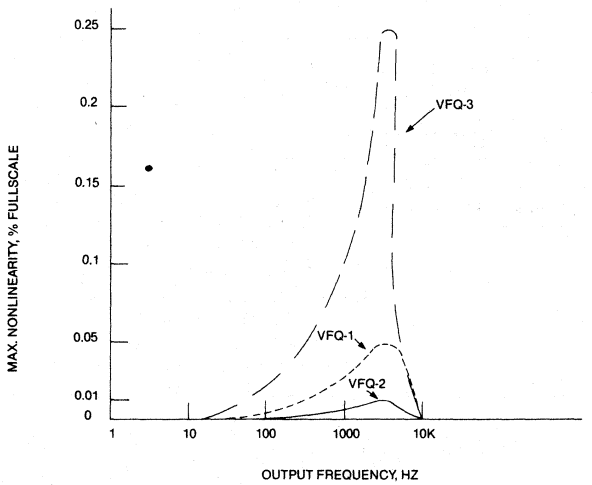
ORDERING INFORMATION

MODEL	TEMP. RANGE	LINEARITY	PRICE
VFQ-1C	0°C to + 70°C	0.05%	
VFQ-1R	– 25°C to + 85°C	0.05%	
VFQ-2C	0°C to + 70°C	0.01%	
VFQ-3C	0°C to + 70°C	0.25%	

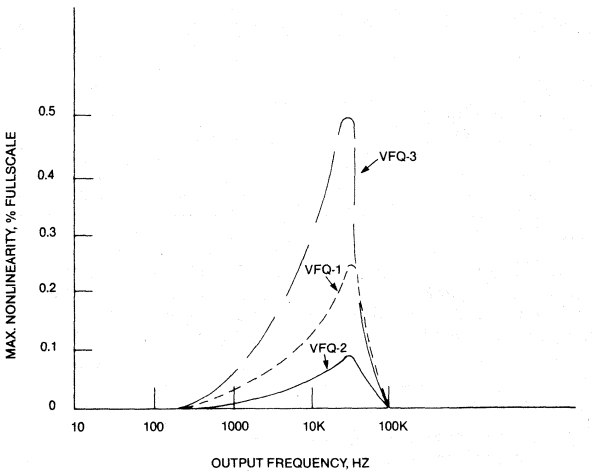
TRIMMING POTENTIOMETER: TP50K

PERFORMANCE CHARACTERISTICS

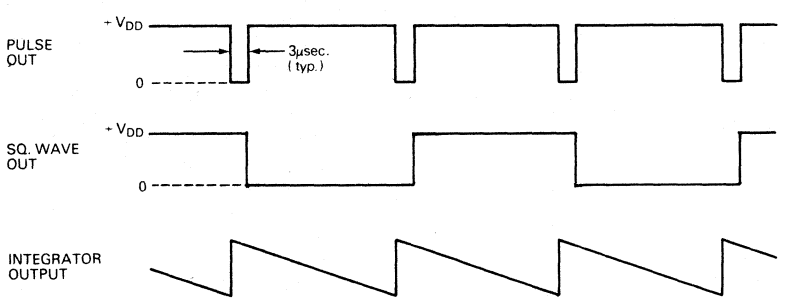
MAX. NONLINEARITY - 10 KHZ FULLSCALE

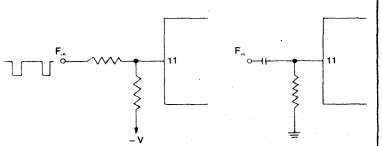


MAX. NONLINEARITY - 100 KHZ FULLSCALE



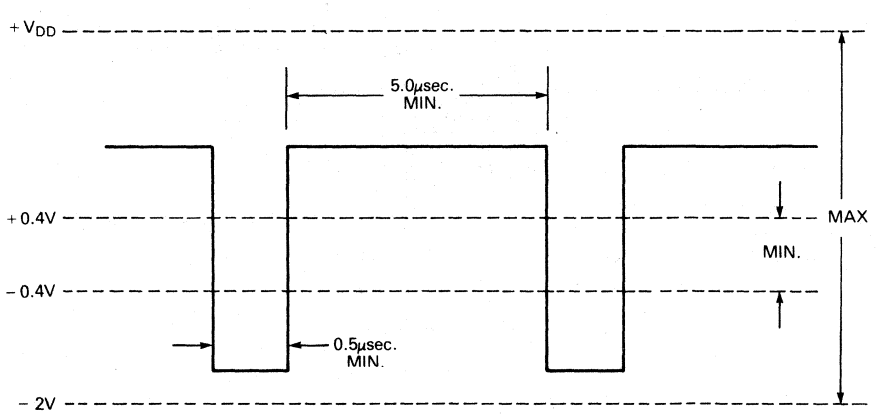
OUTPUT WAVEFORMS





NOTE:
For F/V operation, if only a unipolar input signal is available, an offset circuit using resistors should be used or the signal should be capacitor coupled.

INPUT WAVEFORM LIMITS (F/V CONVERTER)



VFQ FORMULAS

$$f_{OUT} = \frac{V_{IN}}{R_1} \times \frac{1}{V_{REF}\ C_2}$$

$$R_1 = \frac{V_{IN}\ (max.)}{10\mu A}$$

$82K \leq R_2 \leq 120K$

$3C_2 \leq C_1 \leq 10\ C_2$

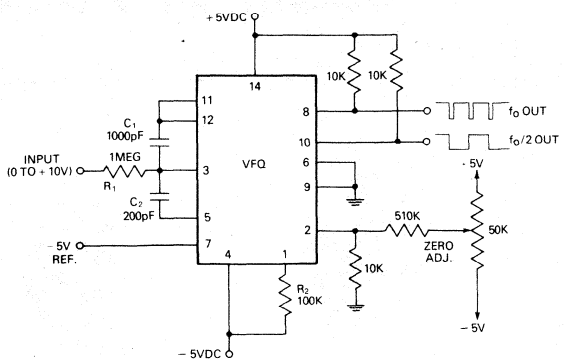
C_1 (optimum) $= 4\ C_2$

F/V CONVERTER
$V_{OUT} = F_{IN}(V_{REF} \times C_2 \times R_1)$

OUTPUT TIME CONSTANT:
$T = R_1\ C_1$

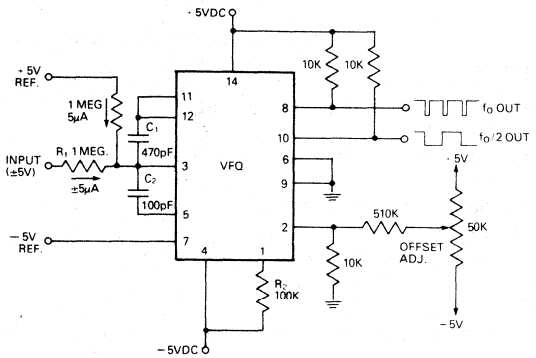
APPLICATIONS DIAGRAMS

NORMAL CONNECTION—10 kHz FULL SCALE

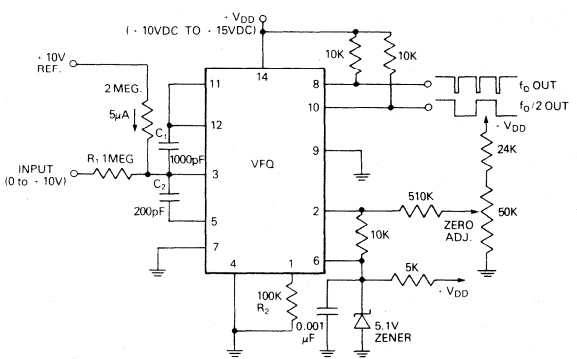


NOTE: FOR 100kHz FULL SCALE, C_1 = 100pF AND C_2 = 20 pF

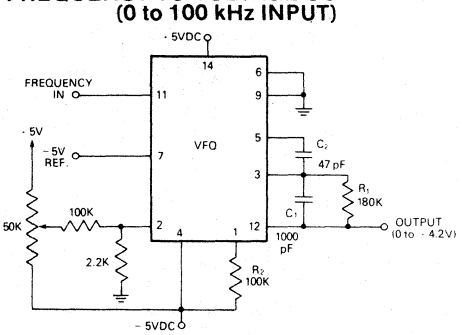
BIPOLAR OPERATION (0 to 20 kHz)



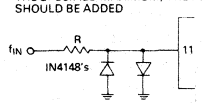
SINGLE SUPPLY OPERATION



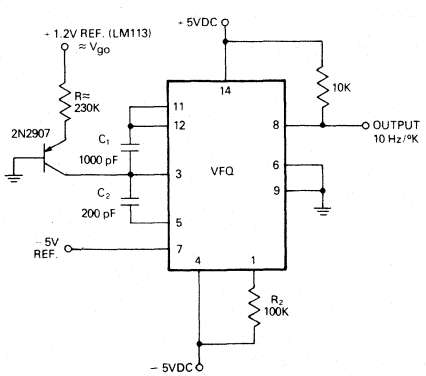
FREQUENCY TO VOLTAGE CONVERTER (0 to 100 kHz INPUT)



NOTE: IF THE AMPLITUDE OF THE INPUT WAVEFORM EXCEEDS THE SPECIFIED MAXIMUM, THE FOLLOWING INPUT CIRCUIT SHOULD BE ADDED



TEMPERATURE TO FREQUENCY CONVERTER



NOTES:

1. V_{go} IS THE EXTRAPOLATED ENERGY-BAND-GAP VOLTAGE FOR SILICON AT 0°K.
2. R IS A STABLE METAL FILM RESISTOR (50 PPM/°C OR BETTER) ITS EXACT VALUE SHOULD BE FOUND BY ADJUSTING IT TO GIVE AN OUTPUT FREQUENCY OF 10 X °K IN HZ FOR A KNOWN TEMPERATURE SUCH AS 300°K. IT WILL THEN BE CORRECTLY CALIBRATED FOR ALL OTHER TEMPERATURES.
3. WHEN PROPERLY IMPLEMENTED THIS CONVERTER IS ACCURATE TO 1°K.

Monolithic Voltage Converter Model VI-7660

FEATURES

- **Easy +5V supply conversion to ±5V supplies**
- **Simple voltage multiplication (V_{OUT} = (−) nV_{IN})**
- **99.9% typical voltage conversion efficiency (RL = ∞)**
- **98% typical power efficiency**
- **Wide operating voltage range 1.5V to 10.0V**
- **Requires only 2 non-critical passive components**

GENERAL DESCRIPTION

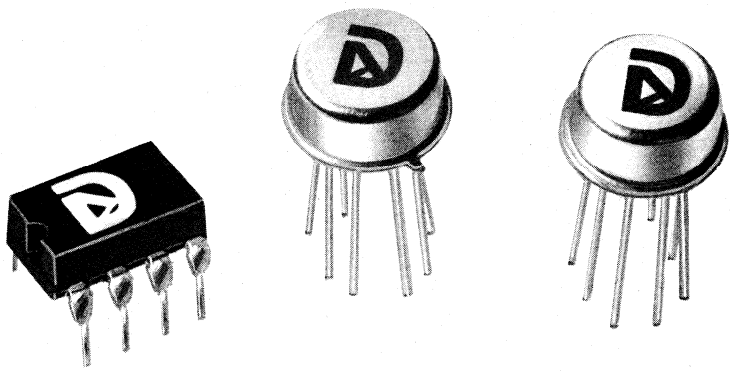
The VI-7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The VI-7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for $V_{SUPPLY} > 6.5V$.

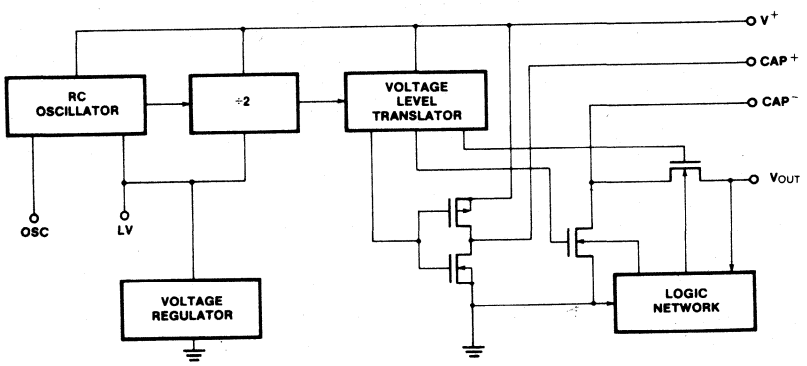
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

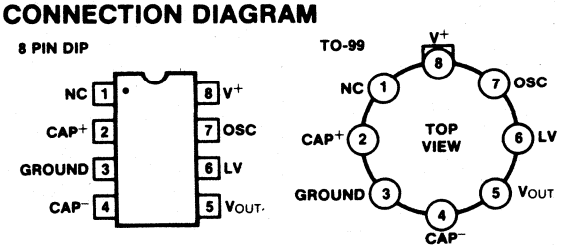
The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the VI-7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The VI-7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.





CONNECTION DIAGRAM



Note: 1. Pin 1 is designated by dot or notch for DIP.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PACKAGE	PRICE (1-24)
VI-7660-I	0 to +70°C	Plastic	
VI-7660-2	0 to +70°C	TO-99	

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
LV and OSC Input Voltage
(Note 1) ..... −0.3V to (V^+ + 0.3V) for V^+ < 5.5V
(V^+ − 5.5V) to (V^+ + 0.3V) for V^+ > 5.5V
Current into LV (Note 1) ..... 20μA for V^+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ... Continuous Power Dissipation (Note 2)
VI-7660-2 ..... 500mW
VI-7660-I 300mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature
(Soldering, 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

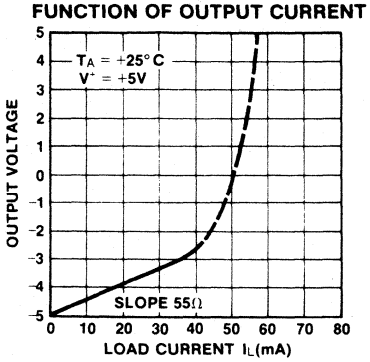
OPERATING CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$,

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I^+	Supply Current		170	500	μA	$R_L = \infty$
V^+_{H1}	Supply Voltage Range - Hi (Dx out of circuit)	3.0		6.5	V	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV = No Connection
V^+_{L1}	Supply Voltage Range - Lo (Dx out of circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground
V^+_{H2}	Supply Voltage Range - Hi (Dx in circuit)	3.0		10.0	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = No Connection
V^+_{L2}	Supply Voltage Range - Lo (Dx in circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground
R_{OUT}	Output Source Resistance		55	100	Ω	I_{OUT} = 20mA, T_A = 25°C
				120	Ω	I_{OUT} = 20mA, −20°C ≤ T_A ≤ +70°C
				300	Ω	V^+ = 2V, I_{OUT} = 3mA, LV = Ground, −20°C ≤ T_A ≤ +70°C
f_{OSC}	Oscillator Frequency		10		kHz	
P_{Ef}	Power Efficiency	95	98		%	R_L = 5kΩ
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	97	99.9		%	$R_L = \infty$
Z_{OSC}	Oscillator Impedance		1.0		MΩ	V^+ = 2 Volts
			100		kΩ	V^+ = 5 Volts

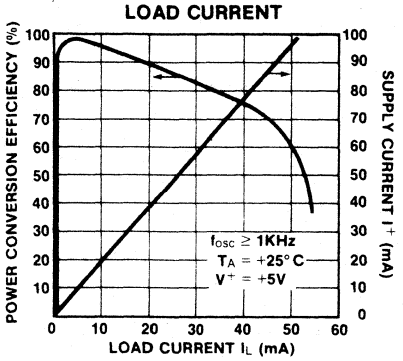
Notes: **1.** Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the V I-7660.
2. Derate linearly above 50°C by 5.5mW/°C.

TYPICAL PERFORMANCE CHARACTERISTICS

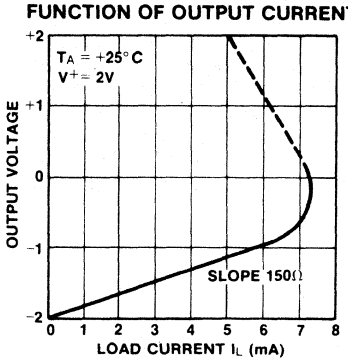
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



Precision Bandgap Voltage References VR-182 Series

FEATURES

- **2.455V Output**
- **Tempcos to 30 ppm/°C**
- **2 to 120 mA Ref. Current**
- **±1.4% Tolerance**
- **2-Terminal**
- **Low Cost**

GENERAL DESCRIPTION

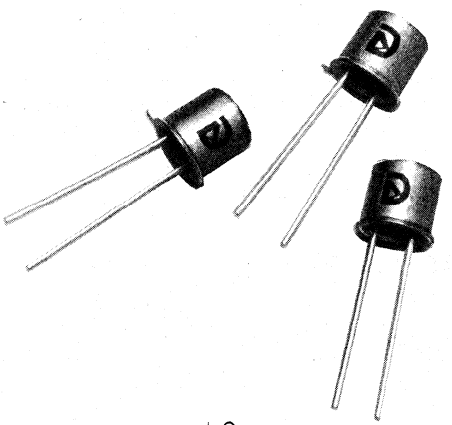
The VR-182 series precision references are two-terminal monolithic bandgap devices which feature 2.455 volts output with tight tolerance and low tempcos. Temperature coefficients are 100, 50, and 30 ppm/°C respectively for Models VR-182A, VR-182B, and VR-182C.

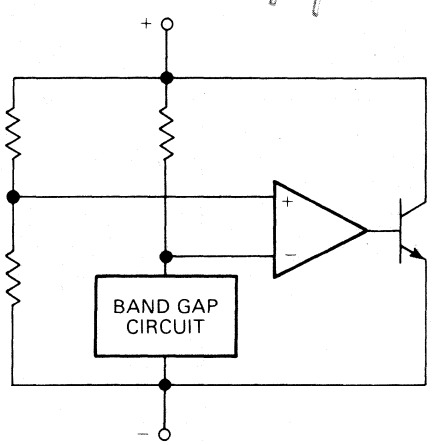
An active regulator around the bandgap circuit results in 0.1 ohm typical dynamic impedance with a wide 2 to 120 mA reference current range. Furthermore, the dynamic impedance is flat to 4 KHz rising to only 1.2 ohms at 50 KHz. Other specifications include ±1.43% voltage tolerance, 10 μV RMS output voltage noise, and 10 ppm per 1000 hours long term stability.

These low cost references are easy to use and are ideal for use with monolithic A/D and D/A converters which do not have internal references. They are also useful in voltage regulator circuits, switching power supplies, comparator circuits, and other analog signal processing applications.

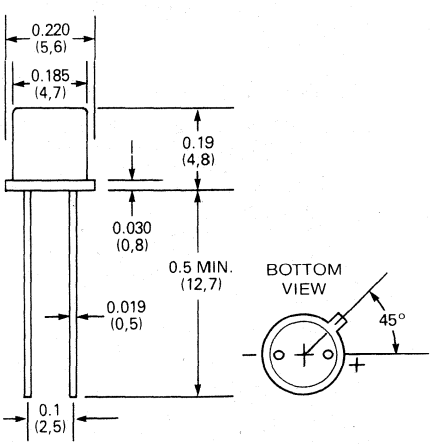
The low 2.455 reference voltage allows these references to be used with 5V logic supplies and other power supply voltages as low as 3.5V. In many cases they give improved performance over higher priced Zener diode references which require higher supply voltages and have much higher dynamic impedances.

The VR-182 devices are supplied in a two-lead hermetically sealed TO-18 package and operate over the 0°C to 70°C temperature range.

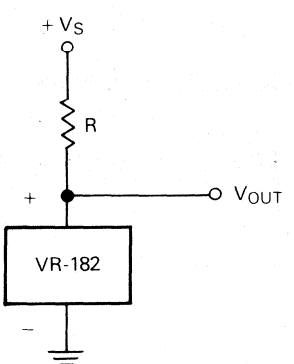




MECHANICAL DIMENSIONS
INCHES (MM)



CONNECTION



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SPECIFICATIONS, VR-182 SERIES
Typical at 25°C, I_{REF} = 2 mA unless otherwise noted.

MAXIMUM RATINGS
- **Reference Current** . . . . . 120 mA*
- **Dissipation** . . . . . 300 mW

OUTPUT
- **Output Voltage** 2.455V
- **Output Voltage Tolerance, %** . . . . ±1.43%
- **Output Voltage Tolerance, mV** . . . ±35 mV

PERFORMANCE
- **Reference Current Range** . . . . . 2 to 120 mA*
- **Temperature Coefficient, ppm/°C**
  - **VR-182A** . . . . . 60 typ., 100 max.
  - **VR-182B** . . . . . 35 typ., 50 max.
  - **VR-182C** . . . . . 23 typ., 30 max.
- **Dynamic Impedance, DC** . . . . . 0.1 typ., 0.2 ohm max.
- **Dynamic Impedance, 50 KHz** . . . 1.2 ohms
- **Noise Voltage, 1 Hz to 10 Hz** . . . . 10 μV RMS
- **Long Term Stability** . . . . . ±10 ppm/1000 hours

PHYSICAL-ENVIRONMENTAL
- **Operating Temperature Range** . . 0°C to 70°C
- **Storage Temperature Range** . . . . −55°C to +150°C
- **Package Type** 2-lead TO-18

*Derate the 120 mA by 1 mA/°C above 25°C

APPLICATION

VR-182 series voltage references are recommended for use with the following Datel products:

A/D Converters	D/A Converters
ADC-EK Series	DAC-08B
ADC-ET Series	DAC-IC8B
	DAC-IC10B

Application Equation: $R = \frac{V_S - 2.455}{I_L + I_R}$

V_S = Supply Voltage
I_R = Reference Current
I_L = Load Current

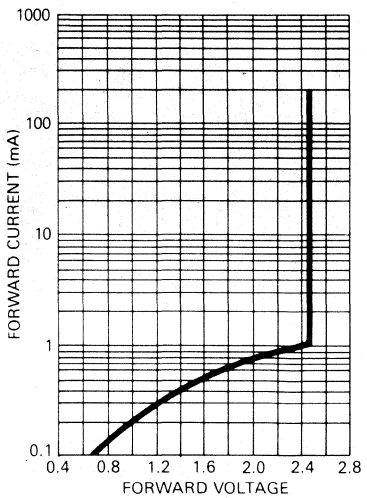
ORDERING INFORMATION

MODEL	TEMPCO/MAX	PRICE (1-24)
VR-182A	100 ppm/°C	
VR-182B	50 ppm/°C	
VR-182C	30 ppm/°C	

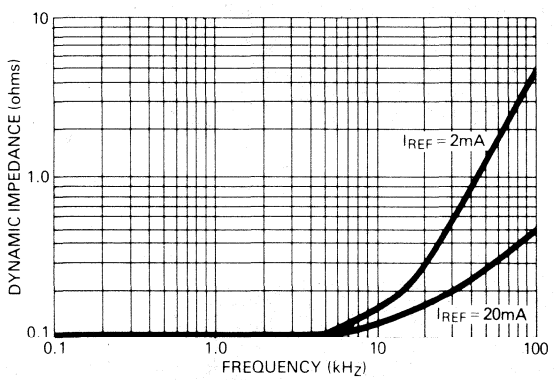
THESE REFERENCES ARE COVERED BY GSA CONTRACT

PERFORMANCE

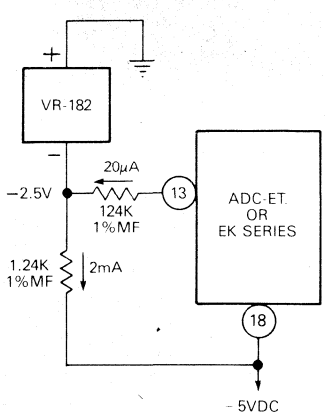
FORWARD CHARACTERISTIC

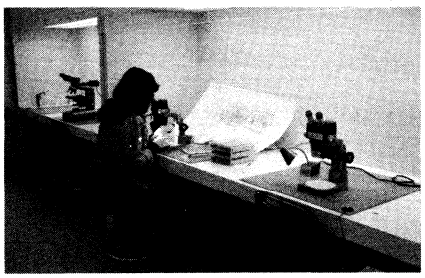


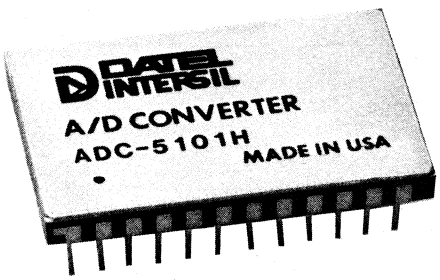
DYNAMIC IMPEDANCE

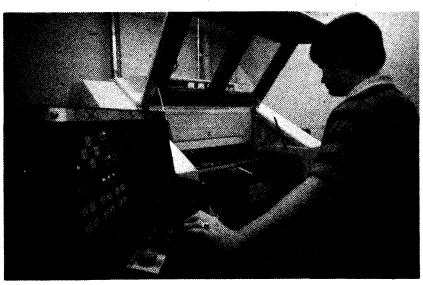


CONNECTION TO DATEL ADC-EK OR ADC-ET SERIES AID CONVERTERS

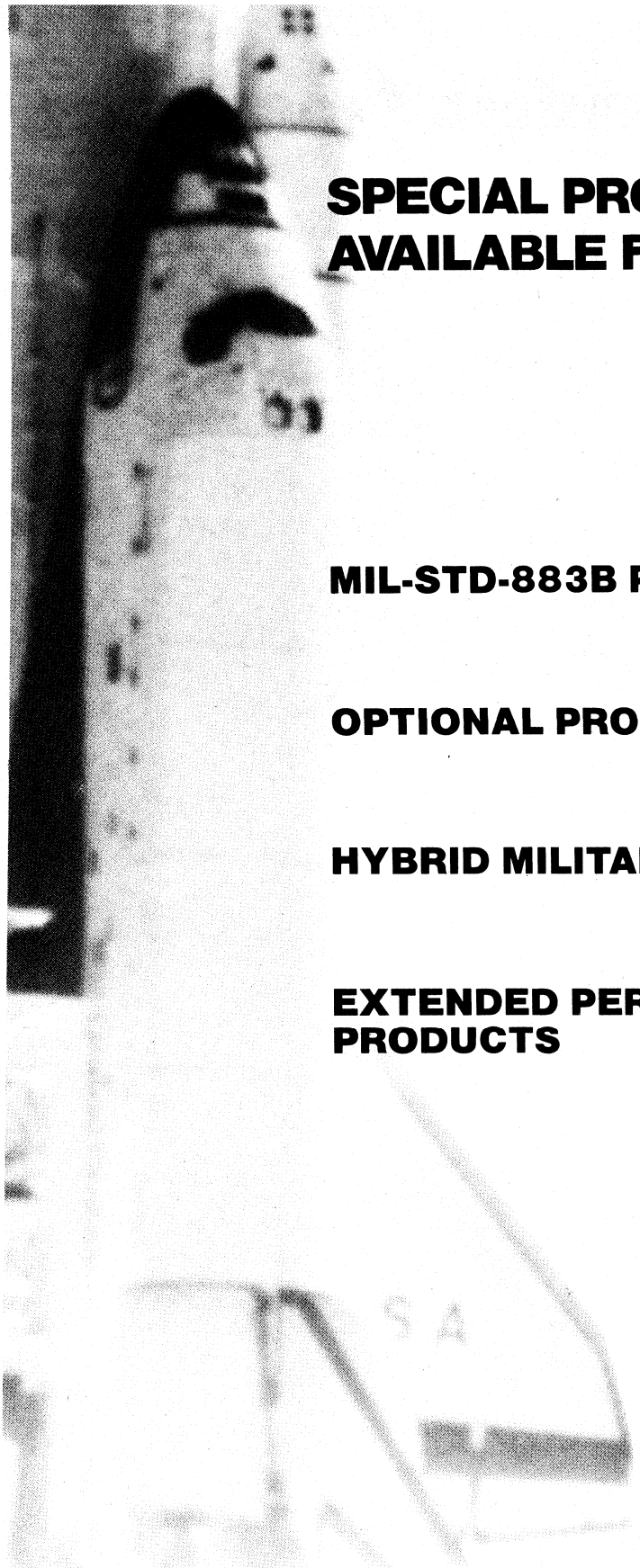





DATEL INTERSIL
A/D CONVERTER
ADC-5101H
MADE IN USA



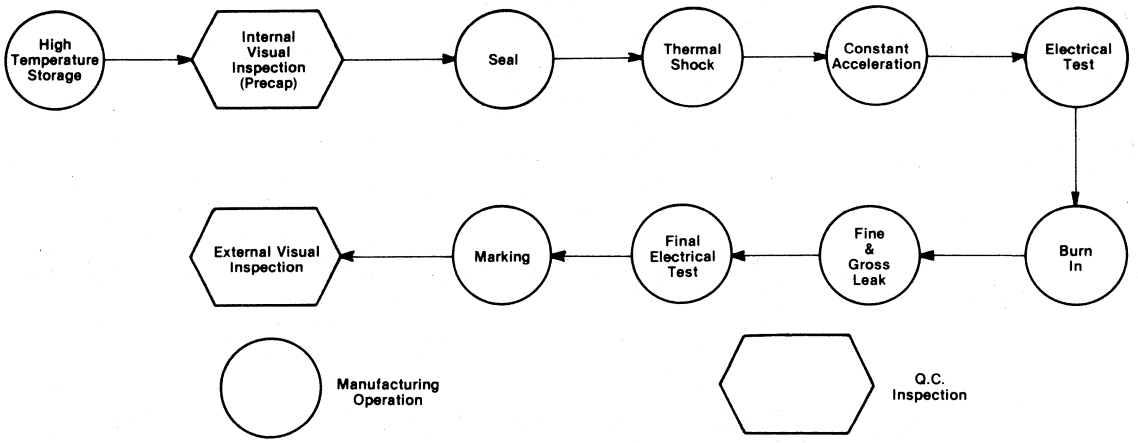

DATEL INTERSIL
A/D CONVERTER
ADC-5101H-QL
MADE IN USA



SPECIAL PROCESSING AVAILABLE FROM DATEL

MIL-STD-883B Standard Processing

Military and Aerospace programs require high reliability devices subjected to rigorous screening procedures. To meet this need Datel-Intersil has developed its QL program, a high level of screening, strictly in accordance with MIL-STD-883, method 5008, Class B. All devices in this program are hermetically sealed and designated with the suffix "QL". The following flow diagram and chart briefly summarize the test procedures followed by the QL program in conformance with MIL-STD-883B. For more complete information, contact your nearest sales office for Datel-Intersil's brochure "HIGH RELIABILITY HYBRID MICROCIRCUITS FOR DATA ACQUISITION".



TEST	METHOD	PURPOSE
HIGH TEMPERATURE STORAGE	Method 1008, Test condition C, 24 hrs @ +150 °C	Eliminates device failure due to storage at elevated temperatures.
INTERNAL VISUAL (PRECAP)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical or thermal stress.
SEAL, FINE AND GROSS	Method 1014, test condition A (fine), 5×10^{-7} cc/sec., test condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
THERMAL SHOCK[1]	Method 5011, test condition A, 15 cycles @ 0 °C to +100 °C.	Determines resistance of device to sudden exposure to extreme temperate changes. Removes potential failures due to thermal stress on bonds, etc.
TEMPERATURE CYCLING	Method 1010, test condition C, −65°C to +150°C	
CONSTANT ACCELERATION	Method 2001, test condition A, Y_1 AXIS, 5 Kg.	Eliminates potential failures due to structural or mechanical weaknesses not detected in shock or vibration tests.
BURN-IN TEST	Method 1015, test condition B, 160 hrs @ +125 °C.	Stresses device at or above maximum rated operating temperature in order to eliminate infant mortality failures.
FINAL ELECTRICAL TESTS	Performed at +25 °C, and at maximum & minimum operating temperatures.	Verifies that device still meets specified data sheet parameters.
EXTERNAL VISUAL	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

1. Per MIL-STD-883B, Thermal shock may be substituted for temperature cycling.

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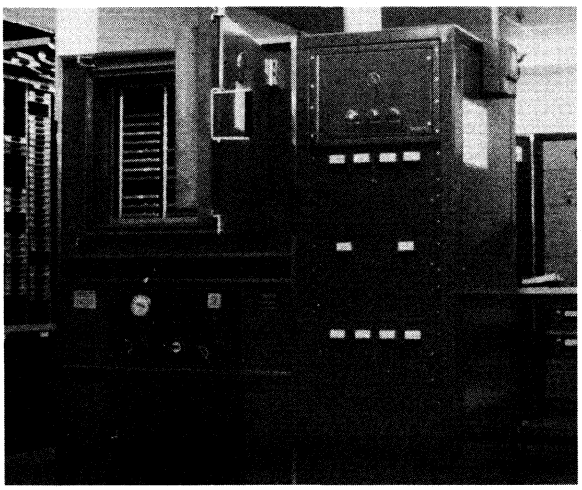
Optional Processing

In addition to the 100% screening tests described, the following sample testing is available per MIL-STD-883B, Method 5008 and referenced sampling plans for product qualification:

- In-process, wire-bond strength testing per MIL-STD-883B Method 2011.
- Group A electrical test per MIL-STD-883B Method 5008 Table I.
- Group B tests per MIL-STD-883B Method 5008 Table II including:
  1. Physical dimensions per MIL-STD-883B Method 2016.
  2. Particle impact-noise detection per MIL-STD-883B Method 2020.
  3. Resistance to solvents per MIL-STD-883B Method 2015.
  4. Die shear strength per MIL-STD-883B Method 2019.
  5. Solderability per MIL-STD-883B Method 2003.
- Group C tests per MIL-STD-883B Method 5008 Table III including:
  1. Temperature cycling per MIL-STD-883B Method 1010.
  2. Constant acceleration per MIL-STD-883B Method 2001.
  3. Seal testing per MIL-STD-883B Method 1014.
  4. Operating-life test per MIL-STD-883B Method 1005.
- Group D package related tests per MIL-STD-883B Method 5008 Table IV including:
  1. Internal water-vapor content per MIL-STD-883B Method 1018.
  2. Seal testing per MIL-STD-883B Method 1014.
  3. Physical dimensions per MIL-STD-883B Method 2016.
  4. Lead integrity per MIL-STD-883B Method 2004.
  5. Thermal shock per MIL-STD-883B Method 1011.
  6. Temperature cycling per MIL-STD-883B Method 1010.
  7. Moisture resistance per MIL-STD-883B Method 1004.
  8. Mechanical shock per MIL-STD-883B Method 2002.
  9. Particle impact-noise detection per MIL-STD-883B Method 2020.
  10. Constant acceleration per MIL-STD-883B Method 2001.
  11. Salt atmosphere per MIL-STD-883B.
  12. Solderability per MIL-STD-883B Method 2003.

Datel-Intersil offers all of the above qualification testing for Class B "QL" products per customer request. In addition, we manufacture, test and qualify to customer-prepared documents requiring higher-level screening or qualification testing (i.e., product x-ray, scanning-electron microscopy, etc.). This testing is done either within Datel-Intersil's own facilities or at MIL-M-38510 certified outside testing laboratories. Datel-Intersil's Microelectronics Division is always ready to meet customer requirements for in-house source inspection, facility surveys, test audits, and whatever other vendor qualifications may be desired.



Datel-Intersil's microelectronic facility provides complete screening to MIL-STD-883 Class B, including 100% burn-in.

Hybrid military products

Datel-Intersil is a recognized industry leader in the design and manufacture of thin film hybrid data conversion products which meet the most demanding reliability requirements for military and aerospace applications per MIL-specifications. Datel-Intersil's data conversion products are currently used in a wide number of military and aerospace flight systems and in high reliability ground support and test systems. Datel-Intersil's modern 120,000 square foot manufacturing facility in Mansfield, Massachusetts includes the most automated and advanced manufacturing, test and calibration equipment available in the industry. This capability, supported by a Quality Assurance Program with full emphasis on product quality assurance and reliability, provides an experienced and reliable source for data converter products to the screening and qualification requirements of Methods 5004, 5005, and 5008 of MIL-STD-883B in compliance with MIL-M-38510 (specified by Datel-Intersil as "Q.L." devices).

The Quality Assurance operation at Datel-Intersil monitors all areas of manufacturing and test, controls manufacturing and screening standards, maintains lot traceability procedures, and sets material standards to assure product quality. All purchased and internally manufactured components are procured or manufactured to precise specification control drawings. All components are 100% electrically tested and 100% visually inspected either by the vendors or internally within Datel-Intersil's facilities. Assembly and test processes and work stations are carefully monitored by Quality Assurance using fully documented procedures to guarantee high standards of workmanship and quality in all of Datel-Intersil's products.

Datel-Intersil products with the suffix "Q.L." are fully screened in accordance with Methods 5004 and 5008 of MIL-STD-883B as amended by MIL-M-38510. The following list briefly summarizes Datel-Intersil's hybrid military products.

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
ADC-HC12BMM	12 bits	300 μsec	± ½ LSB	– 55 to + 125
ADC-HC12BMM-QL	12 bits	300 μsec	± ½ LSB	– 55 to + 125
ADC-HS12BMM	12 bits	9 μsec	± ½ LSB	– 55 to + 100
ADC-HS12BMM-QL	12 bits	9 μsec	± ½ LSB	– 55 to + 100
ADC-HX12BMM	12 bits	20 μsec	± ½ LSB	– 55 to + 100
ADC-HX12BMM-QL	12 bits	20 μsec	± ½ LSB	– 55 to + 100
ADC-HZ12BMM	12 bits	8 μsec	± ½ LSB	– 55 to + 100
ADC-HZ12BMM-QL	12 bits	8 μsec	± ½ LSB	– 55 to + 100
ADC-810MM	12 bits	2 μsec	± ½ LSB	– 55 to + 125
ADC-810MM-QL	12 bits	2 μsec	± ½ LSB	– 55 to + 125
ADC-815MM	8 bits	700 nsec	± ½ LSB	– 55 to + 125
ADC-815MM-QL	8 bits	700 nsec	± ½ LSB	– 55 to + 125
ADC-816MM	10 bits	800 nsec	± ½ LSB	– 55 to + 125
ADC-816MM-QL	10 bits	800 nsec	± ½ LSB	– 55 to + 125
ADC-817MM	12 bits	2 μsec	± ½ LSB	– 55 to + 125
ADC-817MM-QL	12 bits	2 μsec	± ½ LSB	– 55 to + 125
ADC-825MM	8 bits	1 μsec	± ½ LSB	– 55 to + 125
ADC-825MM-QL	8 bits	1 μsec	± ½ LSB	– 55 to + 125
ADC-826MM	10 bits	1.4 μsec	± ½ LSB	– 55 to + 125
ADC-826MM-QL	10 bits	1.4 μsec	± ½ LSB	– 55 to + 125
ADC-827MM	12 bits	3 μsec	± ½ LSB	– 55 to + 125
ADC-827MM-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125
ADC-5101H	8 bits	900 nsec	± ½ LSB	– 55 to + 125
ADC-5101H-QL	8 bits	900 nsec	± ½ LSB	– 55 to + 125
ADC-5210H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5210H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5211H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5211H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5212H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5212H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5213H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5213H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5214H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5214H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5215H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5215H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5216H	12 bits	13 μsec	± ½ LSB	– 55 to + 125
ADC-5216H-QL	12 bits	13 μsec	± ½ LSB	– 55 to + 125

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DIGITAL-TO-ANALOG CONVERTERS

MODEL NO.	RESOLUTION	OUTPUT SETTLING TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
DAC-HA10BM	10 bits	1.3 μsec	± ½ LSB	– 55 to + 125
DAC-HA10BM-QL	10 bits	1.3 μsec	± ½ LSB	– 55 to + 125
DAC-HA12BM	12 bits	5 μsec	± ½ LSB	– 55 to + 125
DAC-HA12BM-QL	12 bits	5 μsec	± ½ LSB	– 55 to + 125
DAC-HA14BM	14 bits	7 μsec	± 1 LSB	– 55 to + 125
DAC-HA14BM-QL	14 bits	7 μsec	± 1 LSB	– 55 to + 125
DAC-HF8BMM	8 bits	25 nsec	± ½ LSB	– 55 to + 125
DAC-HF8BMM-QL	8 bits	25 nsec	± ½ LSB	– 55 to + 125
DAC-HF10BMM	10 bits	25 nsec	± ½ LSB	– 55 to + 125
DAC-HF10BMM-QL	10 bits	25 nsec	± ½ LSB	– 55 to + 125
DAC-HF12BMM	12 bits	50 nsec	± ½ LSB	– 55 to + 125
DAC-HF12BMM-QL	12 bits	50 nsec	± ½ LSB	– 55 to + 125
DAC-HK12BMM	12 bits	3 μsec	± ½ LSB	– 55 to + 125
DAC-HK12BMM-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125
DAC-HP16BMM	16 bits	15 μsec	± 2 LSB	– 55 to + 125
DAC-HP16BMM-QL	16 bits	15 μsec	± 2 LSB	– 55 to + 125
DAC-HZ12BMM	12 bits	3 μsec	± ½ LSB	– 55 to + 125
DAC-HZ12BMM-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125
DAC-87-CBI-I	12 bits	300 nsec	± ½ LSB	– 55 to + 125
DAC-87-CBI-I-QL	12 bits	300 nsec	± ½ LSB	– 55 to + 125
DAC-87-CBI-V	12 bits	3 μsec	± ½ LSB	– 55 to + 125
DAC-87-CBI-V-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125
DAC-87-CCD-I	3 digits	300 nsec	± ¼ LSB	– 55 to + 125
DAC-87-CCD-I-QL	3 digits	300 nsec	± ¼ LSB	– 55 to + 125
DAC-87-CCD-V	3 digits	3 μsec	± ¼ LSB	– 55 to + 125
DAC-87-CCD-V-QL	3 digits	3 μsec	± ¼ LSB	– 55 to + 125

SAMPLE-HOLD AMPLIFIERS

MODEL NO.	ACCURACY	ACQUISITION TIME	HOLD MODE DROOP	OPERATING TEMP. RANGE (°C)
SHM-6MM	0.01%	1 μsec	10μV/μsec	– 55 to + 125
SHM-6MM-QL	0.01%	1 μsec	10μV/μsec	– 55 to + 125
SHM-9MM	0.01%	6 μsec	0.2 mv/ms	– 55 to + 125
SHM-9MM-QL	0.01%	6 μsec	0.2 mv/ms	– 55 to + 125
SHM-HUMM	0.10%	25 nsec	50μV/μsec	– 55 to + 100
SHM-HUMM-QL	0.10%	25 nsec	50μV/μsec	– 55 to + 100

OPERATIONAL AMPLIFIERS

MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-500MM	3 mV	130 MHz	± 10V @ 50 mA	– 55 to + 125
AM-500MM-QL	3 mV	130 MHz	± 10V @ 50 mA	– 55 to + 125

DIGITALLY PROGRAMMABLE INSTRUMENTATION AMPLIFIERS

MODEL NO.	GAIN RANGE	SETTLING TIME	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-542MM	1 to 1024	150 μsec	± 10.5V @ 5 mA	– 55 to + 125
AM-542MM-QL	1 to 1024	150 μsec	± 10.5V @ 5 mA	– 55 to + 125
AM-543MM	1 to 128	6 μsec	± 11V @ 1mA	– 55 to + 125
AM-543MM-QL	1 to 128	6 μsec	± 11V @ 1 mA	– 55 to + 125

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT RATE	OPERATING TEMP. RANGE (°C)
HDAS-8MM	12 bits	8 Differential	50 kHz	– 55 to + 125
HDAS-8MM-QL	12 bits	8 Differential	50 kHz	– 55 to + 125
HDAS-16MM	12 bits	16 Single-Ended	50 kHz	– 55 to + 125
HDAS-16MM-QL	12 bits	16 Single-Ended	50 kHz	– 55 to + 125

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Extended performance products

Discrete modular products are normally specified for operation over the commercial operating temperature range of 0°C to +70°C. While this temperature range is satisfactory for most applications encountered in industrial environments or research laboratories, there are some applications which may require a wider temperature range and/or the additional reliability of hermetically sealed semiconductor components.

Datel-Intersil, through its Extended Performance Program, offers versions of the discrete modular products listed below selected in accordance with the following suffix designations:

EX = Extended operating temperature range of −25°C to +85°C.

EXX-HS = Extended operating temperature range of −55°C to +85°C with all hermetically sealed semiconductor components.

In addition to the extended performance options, Datel-Intersil also offers standard burn-in options for these modules and for all hybrid products. Burn-in options are indicated by the following add-on suffixes:

MODULES

BU01	96 hours at +25°C
BU02	96 hours at +85°C
BU03	168 hours at +25°C
BU04	168 hours at +85°C
BU05	96 hours at +70°C
BU06	168 hours at +70°C

HYBRIDS

B1	96 hours at +25°C
B2	96 hours at +85°C
B3	96 hours at +100°C
B4	96 hours at +125°C
B5	168 hours at +25°C
B6	168 hours at +85°C
B7	168 hours at +100°C
B8	168 hours at +125°C

MODEL/SERIES	EX	EXX-HS
ADC-E	YES	—
ADC-ECONOVERTER	YES	YES
ADC-EH	YES	YES
ADC-G	YES	YES
ADC-MA	YES	YES
ADC-UH	YES	YES
ADC-89A	YES	YES
ADC-149	YES	YES
ADC-876	YES	YES
ADC-881	YES	YES
DAC-DG12B	YES	YES
DAC-HI	YES	YES
DAC-HR	YES	YES

MODEL/SERIES	EX	EXX-HS
SHM-2	YES	YES
SHM-2E	YES	YES
SHM-5	YES	YES
SHM-UH	YES	YES
SHM-UH3	YES	YES
MDAS-16/8D	YES	YES
DAS-250	YES	YES
AM-100	YES	—
AM-101	YES	—
AM-102	YES	—
AM-103	YES	—
AM-201	YES	—
AM-303	YES	—
VFV-10	YES	YES
VFV-100	YES	—

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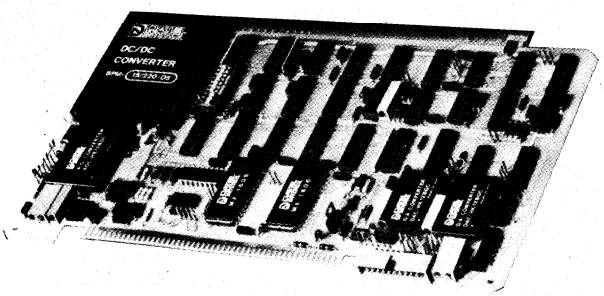
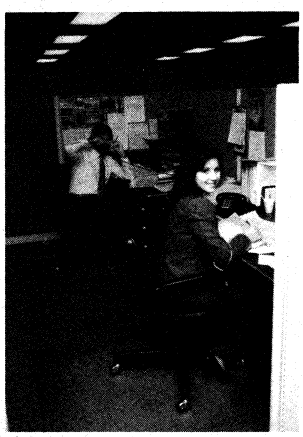
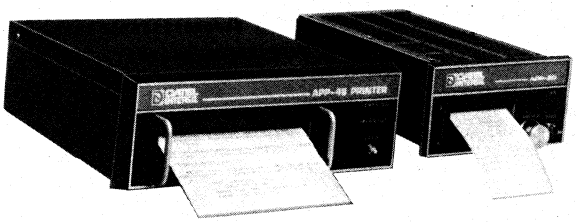

DC/DC
CONVERTER



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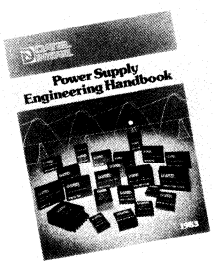
ADDITIONAL PRODUCTS FROM DATEL . . .

DATA ACQUISITION SYSTEMS, MODULES, HYBRIDS, ICS

DATEL

Your COMPLETE Source for A/D Converters, D/A Converters, Sample-Hold, MUX, Data Acquisition Systems, Data Loggers, Digital Panel Meters, Thermal Printers, Power Supplies, DC/DC Converters, Computer I/O Boards . . . *and much more*



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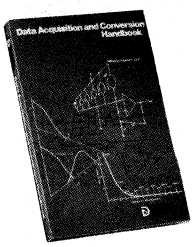

BE AN EXPERT ON DATA ACQUISITION REQUEST ORDERING DETAILS

DATEL INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

DVC-8500 Miniature Digital Voltage Calibrator

The DVC-8500 provides a precisely regulated DC voltage output over a ±20.0005 VDC range selected from front panel thumbwheel switches and an offset vernier control. The thumbwheel switches select voltages down to ±1 mV resolution and the vernier makes a further adjustment of ±1.5 mV which may be used for amplifier adjustments, setting comparator limits and A/D-D/A converter bit decision levels. The output amplifier delivers up to 25 mA regulated to within the accuracy specifications which are ±25 ppm of setting, ±500 μV. Outputs beyond 25 mA trip the overload LED indicator and the output is short-circuit protected by current limiting at 70 mA. Outputs are taken either from front panel banana jacks or rear panel PC board connection. Sense inputs are included on the rear panel for output accuracy delivered at a remote load. The DVC-8500 is powered by a choice of 100, 115, or 230 VAC. The instrument includes a benchtop tilt-up stand which may be removed for panel mounting.

Quick Specifications

Output voltage range	0 to ±19.999 VDC, cascaded with continuous verner control ±1.5 mVDC
Resolution of setting	1 mV increments
Output current	0 to 25 mA (rated accuracy)
	greater than 25 mA (LED front panel overload lamp)
	70 mA (short-circuit current limit)
Accuracy at +25°C	within ±25 ppm of setting, ±500 μV (typical)
Output temperature coefficient	Zero: within ±5 μV/°C (typical)
	Setting: within ±4 ppm of setting/°C (typical)
Operating temperature range	0 to +50°C
Warm-up time	5 minutes to rated accuracy
Output noise	25 μV p-p wideband
Power supply	100, 115 or 230 VAC, 47 to 440 Hz, 10 watts
AC transformer isolation	1000 MΩ, 300 VRMS min.
Case dimensions	5.59"W x 2.11"H x 5.78"D (142.0 x 53.6 x 146.8 mm)
Bezel dimensions	5.86"W x 2.25"H x 0.50" THK (148.7 x 57.0 x 12.7 mm)
Mounting cutout	5.62"W x 2.16"H (142.7 x 54.8 mm)
Weight	2.25 pounds (1.0 kg)

Ordering Guide

MODEL	POWER VOLTAGE
DVC-8500A	115 VAC
DVC-8500E	230 VAC
DVC-8500J	100 VAC

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

Quick selection: Digital panel meters

MODEL	NUMBER OF DIGITS	DISPLAY TYPE	DISPLAY HEIGHT	INPUT TYPE	FULL SCALE INPUT RANGE	DATA OUTPUTS	USER-INSTALLED FEATURES
DM-3100N	3½	Red LED	0.56"	Balanced differential	± 1.999 VDC	NO	Input attenuator, shunt, offset
DM-3100B			0.56"	Balanced differential transformer-isolated			Input attenuator, shunt
DM-3100L			0.56"	Balanced differential			Input attenuator, shunt
DM-31			0.56"	Balanced differential			Input attenuator, shunt
DM-3101			0.6"	Balanced differential			" & offset pot
DM-3103			0.6"	Balanced differential			" (no offset)
DM-3104			0.6"	Balanced differential, transformer-isolated			"
DM-LX3		Black LCD	0.75"	Balanced differential			Input attenuator, shunt
DM-3100U1			0.5"	Balanced differential			Input attenuator, shunt, offset
DM-3100U2 DM-3100U3			0.5"	Balanced differential transformer-isolated			Input attenuator, shunt, offset
DM-3100X			0.5"	Balanced differential			Input attenuator, shunt
DM-4101L	4½	Red LED	0.56"	Balanced differential	± 1.9999 VDC	4-wire multiplexed BCD	Input attenuator, shunt
DM-4101N			0.3"	Balanced differential		NO	Input attenuator, shunt
DM-4200			0.3"	Balanced differential		4-wire multiplexed BCD	Input attenuator, shunt
DM-4105		Black LCD	0.5"	Balanced differential		4-wire multiplexed BCD	Input attenuator, shunt
DM-4101D		Red LED	0.3"	Balanced differential 100 MΩ, 5 pA		3-state shared μP-bus BCD	Input attenuator, shunt

Other Panel Instruments

MODEL	NUMBER OF DIGITS	FUNCTION	DESCRIPTION
PC-6	6 LED digits, 0.3"H	Programmable counter/timer	5 functions: 1. unit counter to 10 MHz, 2. frequency meter to 10 MHz
DVC-8500	4½	Digital voltage calibrator	Front digit setting levers, 1 mV resolution, ± 20,000 mVDC range
DBM-20	20 LED bars, 0.2"H	Digital bar meter with analog (linear) display	Adjustable input range, + 0.1 VDC to + 2.4 VDC, unipolar single-ended
DM-4104	4½ LED digits, 0.3"H	Microbussable BCD latched slave display	Accepts multiplexed bus BCD data in 4, 8, 12, 16 or full parallel inputs
DM-4102, 4103, 4106	4½ digits, LED or LCD	Slave display mates to DM-4200, DM-4101L, DM-4105 master DPMs	Requires multiplexed BCD TTL data, up to 25 feet remote

Datel-Intersil's leadership in low cost, instrumentation-grade miniature digital panel meters is the result of nearly a decade of product refinement and experience with OEM customers and end users. Datel-Intersil's product philosophy is to supply DPMs as a fully-specified panel-mounting component at very low cost while retaining outstanding performance specifications. Despite their miniature size, these DPMs are easily customized to other voltage, current or resistance ranges, offset inputs, ratiometric drift-correction and inputs from specific sensors, or transducers. Two miniature case styles are offered to give either minimal front panel height or large displays. Both self-illuminated LED and battery powered LCD displays are offered in 3-1/2 and 4-1/2-digit resolution with standard ±2 VDC input ranges. Both regulated 5 VDC and 115/230 VAC power options are offered and LCD DPMs will accept 6 to 15 VDC battery operation. Several models also include BCD data outputs for data loggers, printers and computer busses. In addition to analog-input/decimal display instruments, other functions offered include a linear bar display (DBM-20), precision DC voltage output (DVC-8500), digital pulse measurement (PC-6) and remote slave repeaters (DM-4102,3,6 and DM-4104).

POWER REQ'D	CASE SIZE	FRONT PANEL CUTOUT	NOTES
+5 VDC reg. at 0.28 A	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	User-adaptable to 4-20 mA input
115/230 VAC, pin-selectable	3.00"W x 2.15"D x 1.76"H	3.062"W x 1.812"H	Miniature AC-powered
+5 VDC reg. at 0.28 A	3.00"W x 2.15"D x 1.76"H	3.062"W x 1.812"H	Short panel depth
+5 VDC reg. at 0.28 A	No case, single board 3.5" x 2" x 0.5"	2.375"W x 1.156"H	Ultra low-cost single board, shallow depth
+5V/.28A	Low profile	2.562"W × 0.97"H	Bright DM-3100N
+5V/.28A	Short depth	3.062"W × 1.812"H	Bright DM-3100L
115/230 VAC, pin-selectable	Short depth	3.062"W × 1.812"H	Bright DM-3100B
5-6 VDC at 3.5 mA	No case, single board 4" x 2" x 0.5"	2.88"W x 1.13"H	Large display, battery-powered single board, shallow depth
5 V at 15 mA or 9-15 V at 6 mA	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	User-adaptable to 4-20 mA input
115 VAC (U2) 230 VAC (U3)	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	Miniature AC-powered
5 V at 15 mA or 9-15 V at 6 mA	3.00"W x 2.15"D x 1.76"H	3.062"W x 1.812"H	Battery-powered
+5 VDC at 0.35 A	3.00"W x 2.15"D x 1.76"H	3.062"W x 1.812"H	Low-cost differential DM-4100L 4½ digit, large display
+5 VDC at 0.25 A	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	Pin-for-pin replacement to DM-4100N in most applications
+5 VDC at 0.25 A	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	Miniature 4½ digit differential w/BCD
5-6 VDC at 5 mA	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	Battery-powered differential 4½ digits
+5 VDC reg. at 450 mA	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	Latched data out strobed in 4, 8, 12, 16 bits

DESCRIPTION	POWER REQ'D	CASE SIZE	FRONT PANEL CUTOUT	NOTES
3. sub-second period counter, 4. frequency ratio counter, 5. dual-channel sub-second interval timer	+5 VDC at 0.35 A regulated	3.00"W x 2.15"D x 1.76"H	3.062"W x 1.812"H	Data code or switch programmable, 10 MHz int. timebase
±1.5 mV vernier, 25 mA out with overload light	115 VAC or 230 VAC	5.59"W x 2.11"H x 5.78"D	5.62"W x 2.16"H	Miniature alum. case with tilt stand
May be user-wired to 2 internal DIP-relay pads for controller applications	+5 VDC at 0.25 A regulated	2.53"W x 3.34"D x 0.94"H	2.562"W x 0.97"H	Choice of horiz-ontal or vertical mounting
Individual 4-bit digit latches allow asynchronous data loading	+5 VDC at 0.45 A regulated	2.53"W x 3.34"D 0.94"H	2.562"W x 0.97"H	Ideal DPM remote repeater or slave display
12-wire interface, suitable for many competitive DPMs	+5 VDC regulated	Short depth and low profile	3.062" x 1.812" or 2.562" x 0.97"	Low cost remote slaves

SineTrac computer A/D-D/A boards

MODEL SERIES	COMPATIBLE COMPUTER BUS	COMPUTER MANU-FACTURER	NO. OF A/D CHANNELS AND RESOLUTION	A/D THROUGHPUT PERIOD	CURRENT LOOP I/O
ST-732	MULTIBUS iSBC-80 Series BLC-80 Series 8-bit CPU's	Intel Corp. Nat'l Semi. Corp.	32S or 16D, jumper-selected, 12 binary bits	Approx. 43 μs, sample-to-sample, High Level	16 diff. 4-20 mA inputs (user-added resistors) and 2 4-20 mA loop outputs.
ST-711			32S or 16D, jumper-selected, 12 binary bits	Approx. 43 μs, sample-to-sample, High Level	16 diff. 4-20 mA inputs (user-added resistors)
ST-724			None	None	4 channels of 4-20 mA loop outputs
ST-728	MULTIBUS iSBC-80 series, 8 or 16 bit data transfer, 16 or 20 bit addressing		None	None	4 or 8 output channels, 4-20 mA
ST-711RLY	MULTIBUS iSBC-80 series BLC-80 series 8 bit CPU's		8D or 16D, 12 binary bits	33 ms sample-to-sample	8 or 16 diff. loop inputs (user-added resistors)
ST-716	MULTIBUS iSBC-80 8/16 data, 16/20 addr		None	None	None
ST-6800 Series	M6800 EXORciser (Can be modified for Rockwell System 65)	Motorola Corp	32S or 16D, 12 binary bits	Approx. 36 μs, sample-to-sample	8 diff. 4-20 mA inputs (user-added resistors)
ST-6800DA Series			None	———	None
ST-6832 Series			32S or 16D, 12 binary bits	Approx. 45 μs, sample-to-sample, high level	16 diff. 4-20 mA inputs (user-added resistors) and 2 4-20 mA loop outputs
ST-LSI-DA Half Quad Series	LSI-11/2 PDP-11/03	Digital Equip. Corp.	None	———	None
ST-LSI2 Half Quad Series			16S or 8D, jumper-selected, 12 binary bits	Approx. 45 μs sample-to-sample, high level	8 diff 4-20 mA inputs (user-added resistors)

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LOW LEVEL INPUTS, PROG. GAIN INST. AMPLIFIER	NO. OF D/A CHANNELS AND RESOLUTION	INTERRUPTS	PACER/ START EXT. TRIG. CLOCK	DC/DC POWER CON-VERTER	NOTES
X1 to X1000, resistor selected, X1, 2, 4, 8 software selected, cascadable, non-isolated	2 with 4-20 mA loops, 12 binary bits	INTA, INTB or 8 MULTIBUS select-able from pacer clock	10-stage int./ext. binary divider, software selected, RC or xtal timebase	Included	Exact replace-ment for iSBC-732
X1 to X1000, resistor selected, X1, 2, 4, 8 software selected, cascadable, non-isolated	None	INTA, INTB or 8 MULTIBUS select-able from pacer clock	10-stage int./ext. binary divider, software selected, RC or xtal timebase	Included	Exact replace-ment for iSBC-711
None	4 loop outputs, 12 binary bits	———	———	Included	Exact replace-, ment for iSBC-724
None	4 or 8 loop outputs, 12 binary bits	None	None	Optional	Runs on iRMX-80 software
X1 to X1000, resistor sel-ected, X1, 2, 5, 10 software selected, cascadable, isolated 250 VRMS, CMR 126 dB, flying cap. mux.	None	INTA, INTB or 8 MULTIBUS select-able from pacer clock	10-stage int./ext. binary divider, software selected, RC or xtal timebase	Included	Runs on iRMX-80 software
None	8 channels, 14 binary bits	None	None	Optional	High resolution D/A
None, use ST-6832	2 optional, 12 binary bits	External event triggered	———	Optional	
———	4 or 8, 12 binary bits	———	———	Optional	
X1 to X1000 resistor select-ed, X1, 2, 4, 8 software-selected, cascadable, non-isolated	2 optional, 12 binary bits	pulls IRQ line; sets EOS/EOC bit in pollable register	16-frequency int./ ext. binary divider, software selected, RC or xtal timebase	Optional	Industrialized A/D-D/A board
———	4 channels, 12 binary bits	———	———	Optional	
X1, 2, 4, 8 or X1, 2, 5, 10 software-selected, non-isolated	None	———	———	Included	

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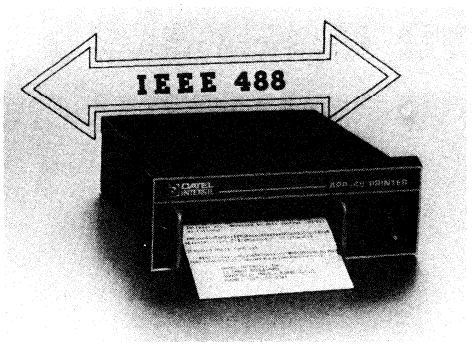
Panel-mount thermal printers

MODEL	NUMBER OF COLUMNS	PRINTING FORMAT	CHARACTER HEIGHT	CHARACTER SET	PRINTING SPEED	PAPER WIDTH	DATA INPUT INTERFACE
DPP-Q7	7 columns (6 plus polarity)	7-segment thermal	0.155 in. (4 mm)	0 to 9 dec. or 0 to F hexadecimal	4 lines/sec	1.75 inches (44, 5 mm)	TTL full parallel BCD, pos/neg true
APP-20A1, E1, V1	20 columns	5 x 7 matrix, dot-line thermal	0.110 in. (0.165 in. programmable)	alphanumeric 96-char. ASCII	1.1 line/sec, 66 lines/min	2.31 in. (58, 6 mm)	TTL bit-parallel byte/char.-serial selectable pos/neg true
APP-20A21, E21, V21	20 columns	5 x 7 matrix, dot-line thermal	0.110 in. 4 heights programmable	alphanumeric 96-char. ASCII	1.05 line/sec, 63 lines/min	2.31 in. (58, 6 mm)	Full serial isolated 20 mA TTY loop or RS-232-C
APP-M20 Series	20 columns	5 x 7 matrix, dot-line thermal	0.110 in. (0.165 in. programmable)	alphanumeric 96-char. ASCII	1.05 line/sec, 63 lines/min	2.31 in. (58, 6 mm)	Byte parallel (1), RS-232-C/20 mA serial (2) or IEEE-488 (3)
APP-20A3, E3, V3	20 columns	5 x 7 matrix, dot-line thermal	0.110 in. (0.165 in. programmable)	alphanumeric 96-char. ASCII	1.05 line/sec, 63 lines/min	2.31 in. (58 6 mm)	IEEE-488-1978 byte parallel interface bus
APP-48A1	48 columns	5 x 7 matrix, dot-line thermal	0.110 in. (2, 8 mm)	alphanumeric 96-char. ASCII plus second set special char.	1.2 lines/sec 72 lines/min	5 inches (127 mm)	TTL bit-parallel, byte/char.-serial, selectable pos/neg true (Centronics compatible)
APP-48A2	48 columns	5 x 7 matrix, dot-line thermal	0.110 in. (2, 8 mm)	alphanumeric 96-char. ASCII plus second set special char.	1.2 lines/sec 72 lines/min	5 inches (127 mm)	Full serial isolated 20 mA TTY loop or RS-232-C
APP-48A3	48 columns	5 x 7 matrix, dot-line thermal	0.110 in. (2, 8 mm)	alphanumeric 96-char. ASCII plus second set special char.	1.2 lines/sec 72 lines/min	5 inches (127 mm)	IEEE-488-1978 byte parallel interface bus
APP-TR Series	7, 20 or 48 columns	Companion take up reel/rewind accessory for DPP-Q7 (APP-TR1), APP-20 (APP-TR2), APP-48 (APP-TR5)					

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

Datel's evolution in miniature thermal panel printers has progressed since 1975 with the development of a complete line of printers containing data and mechanism electronics and built-in power supplies. Current models include a 7-column numeric printer (DPP-Q7), a 20-column alphanumeric (APP-20) and 48-column alphanumeric (APP-48). Data interfaces offered include a full parallel BCD TTL (DPP-Q7 only), 8-bit byte-parallel (APP-20 and 48), IEEE-488 byte parallel (APP-20 and 48) and full serial RS-232-C/isolated 20 mA loop (APP-20 and 48). Power supply options include 100 VAC, 115/230 VAC (VDE-compliance) and +12 VDC. Ruggedized slide mount printers (APP-M20 and M48 series) are also included for vehicle applications.



INPUT REGISTER	DATA LOADING RATE	HOUSING SIZE	POWER SUPPLY	SPECIAL FEATURES
1-line, 7 digits	Latched, 1 μs strobe	4.44"W x 2.76"H x 8.00"D	115/230 VAC selectable, 40 W max, 5 VDC/10 A spec. order	
1-line, 20 characters	1 char. per 500 μs; 900 ms wait while printing	4.44"W x 2.76"H x 8.00"D	115/230 VAC selectable, optional VDE 230 V, optional +12 VDC at 1 A	Selectable inverting (text) or non-inverting (lister) printout. Selectable TALL characters
1 line, 20 characters	75 to 9600 baud, 900 ms wait while printing	4.44"W x 2.76"H x 8.00"D	115/230 VAC selectable, optional VDE 230 V optional +12 VDC at 1 A	Same as above plus selectable small paper-saver characters
1 line, 20 characters	See specific interface above	4.44"W x 2.76"H x 8.00"D	115/230 VAC selectable, 40 W max, optional +12 VDC at 1 A	Includes vehicle mounting slides, printout lamps, ruggedized electronics for mobile applications
1-line, 20 characters	1 char. per 400 μs; 900 ms wait while printing	4.44"W x 2.76"H x 8.00"D	115/230 VAC selectable, optional VDE 230 V, optional +12 VDC at 1 A	Selectable inverting (text) or non-inverting (lister) printout. 5-bit my listen address (MLA)
1-line, 48 characters	Approx. 1 char. per 120 μs; 750 ms wait while printing	8.20"W x 2.84"H x 8.14"D	115/230 VAC selectable, optional +12 VDC at 2 A	Selectable inverting (text) or non-inverting (lister) printout. 2nd char. set European letters, math & currency symbols, etc.
1-line, 48 characters	110 to 9600 baud, 750 ms wait while printing	8.20"W x 2.84"H x 8.14"D	115/230 VAC selectable, optional +12 VDC at 2 A	Selectable inverting (text) or non-inverting (lister) printout. 2nd char. set European letters, math & currency symbols, etc.
1-line, 48 characters	Approx. 1 char. per 400 μs; 750 ms wait while printing	8.20"W x 2.84"H x 8.14"D	115/230 VAC selectable, optional +12 VDC at 2 A	Same as above plus 5-bit My Listen Address (MLA)
Panel-mount, 3.25" High			Choice of 100, 115, 230 VAC or 12 VDC	

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

Line operated power modules

This broad line of regulated DC power supplies features models with single, dual or triple outputs designed for either PCB or chassis mounting.

New products include four compact modular switching supplies and a series of plug-in power adapters consisting of 3 single-output regulated supplies: 5 VDC at 500 mA, 9 VDC at 200 mA and 12 VDC at 200 mA.

Single output, line operated power modules

MODEL NO.	OUTPUT VOLTAGE	RATED OUTPUT CURRENT	LINE/LOAD REGULATION	OUTPUT IMPEDANCE	MODULE SIZE (IN)	COMMENTS
UPM-5/250	5 VDC	250 mA	0.05%/0.1%	0.05 Ω	3.5 x 2.5 x 0.875	Single output, voltage regulated supplies. Tempcos are 0.02%/°C; output ripple is 1 or 2 mV RMS; and output accuracy is within ±1 or ±2%. Available with 115 VAC, 100 VAC or 220 VAC input.
UPM-5/500	5 VDC	500 mA	0.05%/0.1%	0.05 Ω	3.5 x 2.5 x 0.875	
UPM-5/1000	5 VDC	1 A	0.05%0.1%	0.01 Ω	3.5 x 2.5 x 1.25	
UPM-5/1000B	5 VDC	1 A	0.25%/0.25%	0.01 Ω	3.5 x 2.5 x 1.25	
UPM-5/2	5 VDC	2 A	0.05%/0.1%	0.005 Ω	3.5 x 2.5 x 1.56	
UPM-6/150A	6 VDC	150 mA	0.05%/0.1%	0.05 Ω	3.5 x 2.5 x 0.875	
UPM-9/100A	9 VDC	100 mA	0.05%/0.1%	0.01 Ω	3.5 x 2.5 x 0.875	
UPM-12/100A	12 VDC	100 mA	0.02%/0.05%	0.01 Ω	3.5 x 2.5 x 0.875	
UPM-15/100A	15 VDC	100 mA	0.02%/0.05%	0.01 Ω	3.5 x 2.5 x 0.875	

Dual output, line operated power modules

BPM-5/250	±5 VDC	±250 mA	0.05%/0.1%	0.05 Ω	3.5 x 2.5 x 0.875	Dual output, voltage regulated power supplies. Tempcos are 0.02%/°C; output ripple is 1 or 2 mV RMS; and output accuracy is within ±1%. Available with 115 VAC, 100 VAC or 220 VAC input.
BPM-5/500	±5 VDC	±500 mA	0.05%/0.1%	0.03 Ω	3.5 x 2.5 x 1.25	
BPM-12/60	±12 VDC	±60 mA	0.02%/0.05%	0.2 Ω	3.5 x 2.5 x 0.875	
BPM-12/100	±12 VDC	±100 mA	0.02%/0.05%	0.1 Ω	3.5 x 2.5 x 0.875	
BPM-12/200	±12 VDC	±200 mA	0.02%/0.05%	0.05 Ω	3.5 x 2.5 x 1.25	
BPM-12/300	±12 VDC	±300 mA	0.02%/0.05%	0.05 Ω	3.5 x 2.5 x 1.56	
BPM-15/60	±15 VDC	±60 mA	0.02%/0.05%	0.2 Ω	3.5 x 2.5 x 0.875	
BPM-15/100	±15 VDC	±100 mA	0.02%/0.05%	0.1 Ω	3.5 x 2.5 x 0.875	
BPM-15/200	±15 VDC	±200 mA	0.02%/0.05%	0.05 Ω	3.5 x 2.5 x 1.25	
BPM-15/300	±15 VDC	±300 mA	0.02%/0.05%	0.03 Ω	3.5 x 2.5 x 1.56	

Modular switching supplies

USM-5/3	5 VDC	3 A	0.05%/0.1%	0.001 Ω	3.5 x 2.5 x·1.56	PC and chassis mount supplies. Tempcos 0.02%/°C; efficiency 80%. Available with 90-130 VAC or 180-260 VAC input specifications.
USC-5/3	5 VDC	3 A	0.05%/0.1%	0.001 Ω	3.5 x 2.5 x 1.56	
USM-5/5	5 VDC	5 A	0.05%/0.1%	0.002 Ω	3.5 x 2.5 x 1.56	
USC-5/5	5 VDC	5 A	0.05%/0.1%	0.002 Ω	3.5 x 2.5 x 1.56	

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Chassis mounting modules

MODEL NO.	OUTPUT VOLTAGE	RATED OUTPUT CURRENT	LINE/LOAD REGULATION	OUTPUT IMPEDANCE	MODULE SIZE (IN)	COMMENTS
UCM-5/250	5 VDC	250 mA	0.05%/0.1%	0.05 Ω	3.5 x 2.5 x 0.875	I/O connections made to terminal strip on top of modules. Tempcos are 0.02%/°C; output ripple is 1 or 2 mV RMS; and output accuracy is within ± 1 or ± 2%. Available with 115 VAC, 100 VAC or 220 VAC input specifications.
UCM-5/500	5 VDC	500 mA	0.05%/0.01%	0.05 Ω	3.5 x 2.5 x 0.875	
UCM-5/1000	5 VDC	1-A	0.05%/0.1%	0.01 Ω	3.5 x 2.5 x 1.25	
UCM-5/1000B	5 VDC	1 A	0.25%/0.25%	0.01 Ω	3.5 x 2.5 x 1.25	
UCM-5/2	5 VDC	2 A	0.05%/0.1%	0.005 Ω	3.5 x 2.5 x 1.56	
BCM-15/60	± 15 VDC	60 mA	0.02%/0.05%	0.2 Ω	3.5 x 2.5 x 0.875	
BCM-15/100	± 15 VDC	100 mA	0.02%/0.05%	0.1 Ω	3.5 x 2.5 x 0.875	
BCM-15/200	± 15 VDC	200 mA	0.02%/0.05%	0.05 Ω	3.5 x 2.5 x 1.25	
BCM-15/300	± 15 VDC	300 mA	0.02%/0.05%	0.05 Ω	3.5 x 2.5 x 1.56	

Triple output modules

TPM-12/100 -5/500	± 12 VDC/ 5 VDC	± 100 mA/ 500 mA	0.02%/0.05% 0.05%/0.1%	0.1/0.05 Ω	3.5 x 2.5 x 1.56	Tempcos are 0.02%/°C; output accuracy is within ± 1%; and output ripple is 1 or 2 mV RMS. Available with 115 VAC, 100 VAC or 220 VAC input specifications.
TPM-15/100 -5/500	± 15 VDC/ 5 VDC	± 100 mA/ 500 mA	0.02%/0.05% 0.05%/0.1□	0.1/0.05 Ω	3.5 x 2.5 x 1.56	
TPM-12/200 -5/500	± 12 VDC/ 5 VDC	± 200 mA/ 500 mA	0.02%/0.05% 0.05%/0.1%	0.1/0.05 Ω	3.5 x 2.5 x 1.56	
TPM-15/200 -5/500	± 15 VDC/ 5 VDC	± 200 mA/ 500 mA	0.02%/0.05% 0.05%/0.1%	0.1/0.05 Ω	3.5 x 2.5 x 1.56	
TPM-12/150 -5/1000	± 12 VDC/ 5 VDC	± 150 mA/ 1000 mA	0.02%/0.05% 0.05%/0.1%	0.1/0.05 Ω	3.5 x 2.5 x 1.56	
TPM-15/150 -5/1000	± 15 VDC/ 5 VDC	± 150 mA/ 1000 mA	0.02%/0.05% 0.05%/0.1%	0.1/0.05 Ω	3.5 x 2.5 x 1.56	

High voltage, dual output modules

BPM-120/25	± 120 VDC	± 25 mA	0.05%/0.2%	5.0 Ω	3.5 x 2.5 x 1.56	Tempcos 0.02%/°C; output accuracy is within ± 1%; and output ripple is 10 mV RMS. Available with 100, 115 or 220 VAC input specifications.
BPM-150/20	± 150 VDC	± 20 mA	0.05%/0.2%	5.0 Ω	3.5 x 2.5 x 1.56	
BPM-180/16	± 180 VDC	± 16 mA	0.05%/0.2%	5.0 Ω	3.5 x 2.5 x 1.56	

Plug-in power adapters

MODEL NO.	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	LINE/LOAD REGULATION	OUTPUT RIPPLE	COMMENTS
UPA-5/500	115 VAC ± 10%	+ 4.8 to + 5.3 VDC	500 mA	0.3%/0.3%	8 mV RMS	Packaged in flame retardant 2.06 x 2.18 x 1.71 (in.) molded case.
UPA-9/200	115 VAC ± 10%	+ 8.7 to + 9.3 VDC	200 mA	0.3%/0.3%	8 mV RMS	
UPA-12/200	115 VAC ± 10%	+ 11.5 to + 12.5 VDC	200 mA	0.3%/0.3%	8 mV RMS	

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DC-DC converters

This broad line of DC-DC converters features 33 one-watt models with single and dual output voltages. Input voltages are 5, 12, 24, 28 and 48 with single outputs of 5, 12, 15, 24, and 28 and dual outputs of ± 12, ± 15, and ± 18V. Output voltage accuracies are ± 1% with 0.02%/°C temperature coefficients. Other features include low output ripple, 100 megohm isolation, and output current limiting.

1 watt series

MODEL NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	EFFIC. (FULL LOAD)	LINE/LOAD REGULATION	COMMENTS
UPM-5/200-D5	+5 V	200 mA	5 VDC ± 10%	40%	0.05%/0.1%	1 watt series of DC-DC converters. Case size is 1.5 x 2.0 x 0.375 (in). Tempco is 0.02%/°C; output impedance is 0.07 Ω or 0.02 Ω and output noise and ripple is 2 mV RMS (20mv P-P). Output voltage accuracy is within ± 1% and the operating temperature range is −25°C to +71°C.
UPM-5/200-D12	+5 V	200 mA	12 VDC ± 10%	50%	0.05%/0.1%	
UPM-5/200-D28	+5 V	200 mA	28 VDC ± 10%	50%	0.05%/0.1%	
UPM-12/80-D5	+12 V	80 mA	5 VDC ± 10%	50%	0.05%/0.05%	
UPM-12/80-D28	+12 V	80 mA	28 VDC ± 10%	55%	0.05%/0.05%	
UPM-24/40-D5	+24 V	40 mA	5 VDC ± 10%	50%	0.05%/0.05%	
UPM-24/40-D12	+24 V	40 mA	12 VDC ± 10%	55%	0.05%/0.05%	
UPM-28/25-D5	+28 V	25 mA	5 VDC ± 10%	50%	0.05%/0.05%	
UPM-28/25-D12	+28 V	25 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/25-D5	± 12 V	25 mA	5 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/25-D12	± 12 V	25 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/25-D28	± 12 V	25 mA	28 VDC ± 10%	55%	0.05%/0.05%	
BPM-15/25-D5	± 15 V	25 mA	5 VDC ± 10%	50%	0.05%/0.05%	
BPM-15/25-D12	± 15 V	25 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-15/25-D28	± 15 V	25 mA	28 VDC ± 10%	55%	0.05%/0.05%	
BPM-18/25-D5	± 18 V	25 mA	5 VDC ± 10%	50%	0.05%/0.05%	
BPM-18/25-D12	± 18 V	25 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-18/25-D28	± 18 V	25 mA	28 VDC ± 10%	55%	0.05%/0.05%	

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DC-DC converters

This complete line of DC-DC converters features 33 three-watt models with single and dual output voltages. Input voltages are 5, 12, 24, 28 and 48 with single outputs of 5, 12, 15, 24 and 28 and dual outputs of ±12, ±15 and ±18V. Output voltage accuracies are ±1% with 0.02%/°C temperagure coefficients. Other features include low output ripple, 100 megohm isolation, and output current limiting.

3 watt series

MODEL NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	EFFIC. (FULL LOAD)	LINE/LOAD REGULATION	COMMENTS
UPM-5/500-D5	+5 V	500 mA	5 VDC ±10%	40%	0.05%/0.1%	3 watt series of DC-DC converters. Case size is 2.0 x 2.0 x 0.432 (in). Tempco is 0.02%/°C; output impedance is 0.01 Ω or 0.2 Ω, and output noise and ripple is 2 mV RMS (20mv P-P). Output voltage accuracy is within ±1% and the operating temperature range is −25°C to +71°C.
UPM-5/500-D12	+5 V	500 mA	12 VDC ±10%	45%	0.05%/0.1%	
UPM-5/500-D28	+5 V	500 mA	28 VDC ±10%	45%	0.05%/0.1%	
UPM-12/250-D5	+12 V	250 mA	5 VDC ±10%	50%	0.05%/0.05%	
UPM-12/250-D28	+12 V	250 mA	28 VDC ±10%	55%	0.05%/0.05%	
UPM-24/125-D5	+24 V	125 mA	5 VDC ±10%	50%	0.05%/0.05%	
UPM-24/125-D12	+24 V	125 mA	12 VDC ±10%	55%	0.05%/0.05%	
UPM-28/100-D5	+28 V	100 mA	5 VDC ±10%	50%	0.05%/0.05%	
UPM-28/100-D12	+28 V	100 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-12/100-D5	±12 V	100 mA	5 VDC ±10%	50%	0.05%/0.05%	
BPM-12/100-D12	±12 V	100 mA	12 VDC ±10%	50%	0.05%/0.05%	
BPM-12/100-D28	±12 V	100 mA	28 VDC ±10%	55%	0.05%/0.05%	
BPM-15/100-D5	±15 V	100 mA	5 VDC ±10%	45%	0.05%/0.05%	
BPM-15/100-D12	±15 V	100 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-15/100-D28	±15 V	100 mA	28 VDC ±10%	55%	0.05%/0.05%	
BPM-18/100-D5	±18 V	100 mA	5 VDC ±10%	50%	0.05%/0.05%	
BPM-18/100-D12	±18 V	100 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-18/100-D28	±18 V	100 mA	28 VDC ±10%	55%	0.05%/0.05%	

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DC-DC Converters

Datel-Intersil offers a line of miniature, aluminum cased 4.5 watt DC-DC converters. Specifications include voltage accuracy of ± 1%, line regulation of 0.05% max., load regulation of 0.05% max. and tempco of 0.005%/°C. For convenient heat sinking, two 2-56 studs are provided on the bottom of the case. Datel-Intersil's complete line of 5 watt DC-DC converters features 32 different models with both single and dual outputs. Features include low output ripple, 100 megohm isolation, and output current limiting protection.

4.5 watt series

MODEL NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	EFFIC. (FULL LOAD)	LINE/LOAD REGULATION	COMMENTS
BPM-15/150-D5	± 15 V	150 mA	5 VDC ± 5%	51%	0.05%/0.05%	4.5 watt DC-DC converters. Case size (aluminum) 2.0 x 2.0 x 0.4 (in.)
BPM-15/150-D24	± 15 V	150 mA	24 VDC ± 14.5%	54%	0.05%/0.05%	
BPM-15/150-D28	± 15 V	150 mA	28 VDC ± 14%	54%	0.05%/0.05%	

5 watt series

UPM-5/1000-D5	+ 5 V	1.0 A	5 VDC ± 10%	50%	0.05%/0.1%	5 watt series DC-DC converters. Case size is 2.0 x 2.0 x 0.75 (in.) Tempcos are 0.02%/°C, output impedance ranges from 0.005 Ω to 0.03 Ω and output noise and ripple is 5 mV RMS (50mv P-P). Output voltage accuracy is ± 1%, and operating temperature range is − 25°C to + 71°C.
UPM-5/1000-D12	+ 5 V	1.0 A	12 VDC ± 10%	50%	0.05%/0.1%	
UPM-5/1000-D24	+ 5 V	1.0 A	24 VDC ± 10%	50%	0.05%/0.1%	
UPM-5/1000-D28	+ 5 V	1.0 A	28 VDC ± 10%	50%	0.05%/0.1%	
UPM-5/1000-D48	+ 5 V	1.0 A	48 VDC ± 12.5%	50%	0.05%/0.1%	
UPM-12/420-D5	+ 12 V	420 mA	5 VDC ± 10%	50%	0.05%/0.05%	
UPM-12/420-D24	+ 12 V	420 mA	24 VDC ± 10%	50%	0.05%/0.05%	
UPM-12/420-D28	+ 12 V	420 mA	28 VDC ± 10%	55%	0.05%/0.05%	
UPM-12/420-D48	+ 12 V	420 mA	48 VDC ± 12.5%	50%	0.05%/0.05%	
UPM-15/330-D5	+ 15 V	330 mA	5 VDC ± 10%	50%	0.05%/0.05%	
UPM-15/330-D12	+ 15 V	330 mA	12 VDC ± 10%	50%	0.05%/0.05%	
UPM-15/330-D24	+ 15 V	330 mA	24 VDC ± 10%	50%	0.05%/0.05%	
UPM-15/330-D28	+ 15 V	330 mA	28 VDC ± 10%	50%	0.05%/0.05%	
UPM-15/330-D48	+ 15 V	330 mA	48 VDC ± 12.5%	50%	0.05%/0.05%	
UPM-24/210-D5	+ 24 V	210 mA	5 VDC ± 10%	55%	0.05%/0.05%	
UPM-24/210-D12	+ 24 V	210 mA	12 VDC ± 10%	55%	0.05%/0.05%	
UPM-28/180-D5	+ 28 V	180 mA	5 VDC ± 10%	55%	0.05%/0.05%	
UPM-28/180-D12	+ 28 V	180 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/210-D5	± 12 V	210 mA	5 VDC ± 10%	50%	0.05%/0.05%	
BPM-12/210-D12	± 12 V	210 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/210-D24	± 12 V	210 mA	24 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/210-D28	± 12 V	210 mA	28 VDC ± 10%	55%	0.05%/0.05%	
BPM-12/210-D48	± 12 V	210 mA	48 VDC ± 12.5%	50%	0.05%/0.05%	
BPM-15/165-D5	± 15 V	165 mA	5 VDC ± 10%	50%	0.05%/0.05%	
BPM-15/165-D12	± 15 V	165 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-15/165-D24	± 15 V	165 mA	24 VDC ± 10%	55%	0.05%/0.05%	
BPM-15/165-D28	± 15 V	165 mA	28 VDC ± 10%	55%	0.05%/0.05%	
BPM-15/165-D48	± 15 V	165 mA	48 VDC ± 12.5%	50%	0.05%/0.05%	
BPM-18/140-D5	± 18 V	140 mA	5 VDC ± 10%	55%	0.05%/0.05%	
BPM-18/140-D12	± 18 V	140 mA	12 VDC ± 10%	55%	0.05%/0.05%	
BPM-18/140-D24	± 18 V	140 mA	24 VDC ± 10%	55%	0.05%/0.05%	
BPM-18/140-D28	± 18 V	140 mA	28 VDC ± 10%	55%	0.05%/0.05%	
BPM-18/140-D48	± 18 V	140 mA	48 VDC ± 12.5%	50%	0.05%/0.05%	

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DC-DC Converters

This comprehensive line of higher power DC-DC converters features 33 different models with both single and dual outputs. Input voltages are 5, 12, 24, 28 and 48 with single output voltages of 5, 12, 15, 24 and 28 and dual outputs of ±12, ±15 and ±18V. Output voltage accuracies are ±1% with 0.02%/°C temperature coefficients. Other features include low output ripple, 100 megohm isolation, and output current limiting protection.

10 watt series

MODEL NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	EFFIC. (FULL LOAD)	LINE/LOAD REGULATION	COMMENTS
UPM-5/2000-D5	+5 V	2.0 A	5 VDC ±10%	50%	0.05%/0.1%	10 watt series DC-DC converters. Case size is 3.5 x 2.5 x 0.875 (in.)
UPM-5/2000-D12	+5 V	2.0 A	12 VDC ±10%	50%	0.05%/0.1%	
UPM-5/2000-D24	+5 V	2.0 A	24 VDC ±10%	50%	0.05%/0.1%	
UPM-5/2000-D28	+5 V	2.0 A	28 VDC ±10%	50%	0.05%/0.1%	
UPM-5/2000-D48	+5 V	2.0 A	48 VDC ±12.5%	50%	0.05%/0.1%	
UPM-12/840-D5	+12 V	840 mA	5 VDC ±10%	50%	0.05%/0.05%	Tempcos are 0.02%/°C; output impedance is 0.005 Ω or 0.02 Ω, and output noise and ripple is 5 mV RMS (50mv P-P).
UPM-12/840-D24	+12 V	840 mA	24 VDC ±10%	50%	0.05%/0.05%	
UPM-12/840-D28	+12 V	840 mA	28 VDC ±10%	55%	0.05%/0.05%	
UPM-12/840-D48	+12 V	840 mA	48 VDC ±12.5%	50%	0.05%/0.05%	
UPM-15/660-D5	+15 V	660 mA	5 VDC ±10%	50%	0.05%/0.05%	Output voltage accuracy is within ±1% and the operating temperature range is −25°C to +71°C.
UPM-15/660-D12	+15 V	660 mA	12 VDC ±10%	50%	0.05%/0.05%	
UPM-15/660-D24	+15 V	660 mA	24 VDC ±10%	50%	0.05%/0.05%	
UPM-15/660-D28	+15 V	660 mA	28 VDC ±10%	50%	0.05%/0.05%	
UPM-15/660-D48	+15 V	660 mA	48 VDC ±12.5%	50%	0.05%/0.05%	
UPM-24/420-D5	+24 V	420 mA	5 VDC ±10%	55%	0.05%/0.05%	
UPM-24/420-D12	+24 V	420 mA	12 VDC ±10%	55%	0.05%/0.05%	
UPM-28/360-D5	+28 V	360 mA	5 VDC ±10%	55%	0.05%/0.05%	
UPM-28/360-D12	+28 V	360 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-12/420-D5	±12 V	420 mA	5 VDC ±10%	50%	0.05%/0.05%	
BPM-12/420-D12	±12 V	420 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-12/420-D24	±12 V	420 mA	24 VDC ±10%	55%	0.05%/0.05%	
BPM-12/420-D28	±12 V	420 mA	28 VDC ±10%	55%	0.05%/0.05%	
BPM-12/420-D48	±12 V	420 mA	48 VDC ±12.5%	50%	0.05%/0.05%	
BPM-15/330-D5	±15 V	330 mA	5 VDC ±10%	50%	0.05%/0.05%	
BPM-15/330-D12	±15 V	330 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-15/330-D24	±15 V	330 mA	24 VDC ±10%	55%	0.05%/0.05%	
BPM-15/330-D28	±15 V	330 mA	28 VDC ±10%	55%	0.05%/0.05%	
BPM-15/330-D48	±15 V	330 mA	48 VDC ±12.5%	50%	0.05%/0.05%	
BPM-18/280-D5	±18 V	280 mA	5 VDC ±10%	55%	0.05%/0.05%	
BPM-18/280-D12	±18 V	280 mA	12 VDC ±10%	55%	0.05%/0.05%	
BPM-18/280-D24	±18 V	280 mA	24 VDC ±10%	55%	0.05%/0.05%	
BPM-18/280-D28	±18 V	280 mA	28 VDC ±10%	55%	0.05%/0.05%	
BPM-18/280-D48	±18 V	280 mA	48 VDC ±12.5%	50%	0.05%/0.05%	

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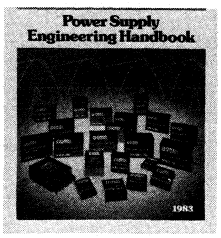
Literature Available From Datel-Intersil



NEW Power Supply Handbook

DATEL-INTERSIL's new 40 page POWER SUPPLY HANDBOOK is a complete reference guide to over 140 different power supplies. Included are 1, 3, 5 and 10 watt DC-DC converters, single, dual and triple output line operated modules, modular switching supplies, plug-in power adapters and high voltage power modules. All specifications are included to make a quick and accurate selection. FREE

Circle (1) on Data Inquiry Card

1982/1983 Short Form Catalog

Our standard SHORT FORM CATALOG provides an overview of DATEL-INTERSIL's entire product line. Data acquisition devices from monolithics to I/O boards as well as digital panel meters, panel mount thermal printers and special function products are included. For ease of selection, significant specifications are included. FREE

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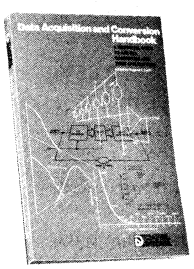

Data Acquisition and Conversion Handbook

DATEL-INTERSIL's DATA ACQUISITION AND CONVERSION HANDBOOK is an informative technical guide to data conversion techniques. Topics of discussion include the principles of data conversion, interfacing data conversion devices with microcomputer systems, designing-in sample-holds and the application of voltage-to-frequency converters in data acquisition systems. This book is required reading for those who are pursuing a better understanding of data conversion theory. $4.95

Circle (3) on Data Inquiry Card

Advanced Hybrid Technology: A Guide to Standard and Hi-Rel Hybrid Processing

This brochure provides an insightful look into DATEL-INTERSIL's hybrid processing facility. Detailed explanations of our manufacturing and testing processes are included for a better understanding of hybrid technology. For more information about the high reliability screening process, order the brochure below. FREE

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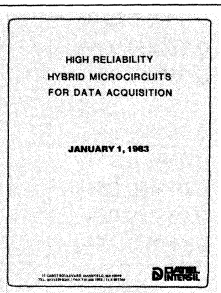

High Reliability Hybrid Microcircuits for Data Acquisition

This brochure delves into a detailed discussion of DATEL-INTERSIL's high reliability screening procedures, per MIL-STD-883 Level B requirements. An easy to follow flow chart is included to provide a better understanding of the HI-REL process. FREE

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Circle (6) on the Data Inquiry Card or call DATEL's Literature Hotline at 1-617-339-9341, ext. 100 to receive our soon-to-be-released catalogs of System Products.

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ORDERING GUIDE

THIS ORDERING GUIDE IS PRESENTED AS A PROCEDURAL GUIDE. FOR A FORMAL STATEMENT OF POLICIES REFER TO THE TERMS AND CONDITIONS OF SALE FOUND ON THE QUOTATION FORM OR ON THE CUSTOMER ACKNOWLEDGEMENT COPY OF THE SALES ORDER.

PLACING AN ORDER
When ordering a Datel-Intersil product, the complete model number, product description, and option description should be given. Orders may be placed with a Datel-Intersil field sales representative or with the factory by letter, telephone, TWX, or TELEX. **MINIMUM ORDER IS** $50.00.

OUTSIDE THE U.S.A. AND CANADA: Orders should be placed with a Datel-Intersil Sales Subsidiary (in West Germany, France, the United Kingdom, and Japan) or with a Datel-Intersil overseas sales representative. Orders received directly will be treated the same as if placed through our overseas sales representative. In countries without a Datel-Intersil representative, orders should be placed by TELEX and confirmed by air mail.

FIELD SALES REPRESENTATIVE
Datel-Intersil employs field sales representatives throughout the United States, Canada, Europe, and the Far East. In addition, it has direct Sales Offices in Santa Ana and Sunnyvale, California. Datel-Intersil also has Sales Subsidiaries in Munich, West Germany; Paris, France; London, England; and Tokyo and Osaka, Japan. These sales representatives are the only ones authorized by Datel-Intersil to solicit sales, and any information or data received by sources other than these authorized representatives or the Datel-Intersil factory cannot be considered binding.

PRICES
All prices are F.O.B., Mansfield, Massachusetts, U.S.A. in U.S. dollars. Applicable federal, state, and local taxes are extra and paid by buyer. Prices are subject to change without notice.

TERMS: Net 30 days.

DISCOUNTS
Quantity discounts are available when placed in a single order. OEM discounts are available on an order or contract basis; consult the factory for details.

QUOTATIONS
Price and delivery quotations made by Datel-Intersil or its authorized field sales representatives are valid for 60 days unless otherwise stated.

DELIVERY
Datel-Intersil uses an IBM System 4331, for efficient processing of orders. All orders placed with Datel-Intersil are acknowledged within a few days by an acknowledgement copy of our sales order form. This copy will indicate pertinent information including a formal statement of terms and conditions of sale and estimated delivery date. This date has preference over all other agreed upon dates unless otherwise specified.

All products are shipped in rugged commercial containers suitable for insuring safe delivery under normal shipping conditions. Unless shipping method is specified, the best available method will be used. UPS, UPS Blue Label, Parcel Post, and Air Parcel Post are among the methods normally used. Datel-Intersil recommends insurance on Parcel Post and Air Parcel Post shipments for tracing purposes. Shipping charges are normally prepaid and billed to the customer except for Air Freight charges which are sent collect. The appropriate data sheet and/or instruction is packed with each product shipped.

ORDER CANCELLATION
All orders entered with Datel-Intersil are binding and are subject to a cancellation charge if cancelled before or after the scheduled shipping date on the acknowledgement copy of the sales order form. The normal cancellation charge is 20% but may be higher depending on expenses already incurred and commitments made by Datel-Intersil.

WARRANTY
Datel-Intersil warrants that its products are free from defects in material and workmanship under normal use and service for a period of one year from date of shipment for any module, hybrid or monolithic product and printers and digital panel meters. For systems and subsystems products the applicable period is 90 days. Datel-Intersil's obligations under this warranty are limited to replacing or repairing, at its option, at its factory or facility, any of the products which shall within the applicable period after shipment be returned to Datel-Intersil's facility, transportation charges prepaid, and which are after examination disclosed to the satisfaction of Datel-Intersil to be thus defective. This warranty shall not apply to any such equipment which shall have been repaired or altered except by Datel-Intersil or which shall have been subjected to misuse, negligence, or accident. In no case shall Datel-Intersil's liability exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Datel-Intersil.

RETURNS
When returning products for any reason, contact the factory first for **return authorization number** and shipping instructions. Items should not be returned air freight collect as they cannot be accepted. It is absolutely necessary to return products in the manner stated here, otherwise considerable delay will result in processing the return.

RETURNS OUTSIDE THE U.S.A. AND CANADA: Contact the local sales representative or factory for authorization and shipping instructions first.

CERTIFICATE OF COMPLIANCE
Datel-Intersil will provide a standard Certificate of Compliance with all shipments when requested by the customer. This request must be specified on the purchase order.

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